Advance

64Mb Double Data Rate Synchronous DRAM

Special Features

- 125MHz max clock freq @ $\overline{\text{CAS}}$ Latency=2
- 133MHz max clock freq @ $\overline{\text{CAS}}$ Latency=2.5
- 143MHz max clock freq @ $\overline{\text{CAS}}$ Latency=3
- On-chip DLL to align output data with input clock
- DLL disable option via Extended Mode Register

Features

- Double Data Rate (DDR)
- Bidirectional Data Strobe with one clock cycle preamble and one-half clock postamble
- On-chip DLL
- Quad bank operation
- Fully synchronous
- Programmable burst type, burst length, and $\overline{\text{CAS}}$ latency
- Burst Read and Write operations
- Read termination by Burst Stop Command
- Auto Precharge and Auto Refresh modes
- 4K Refresh cycles/64ms
- SSTL_2 I/O for data I/O, data mask, data strobe
- LVTTL Inputs for address and control
- Differential clock inputs (SSTL_2)
- V_{DD} = 3.3V ±0.3V, V_{DDQ} = 2.5V ±0.2V
- 66-pin TSOP-II (0.65mm lead pitch)

Timing Options	Marking
83 MHz clock rate	-12
100 MHz clock rate	-10

Key Timing Parameters

Speed Grade @ $\overline{\text{CL}}$=2	Clock Frequency (MHz)	DQ Burst Frequency (MHz)
-12	83	166
-10	100	200

Description

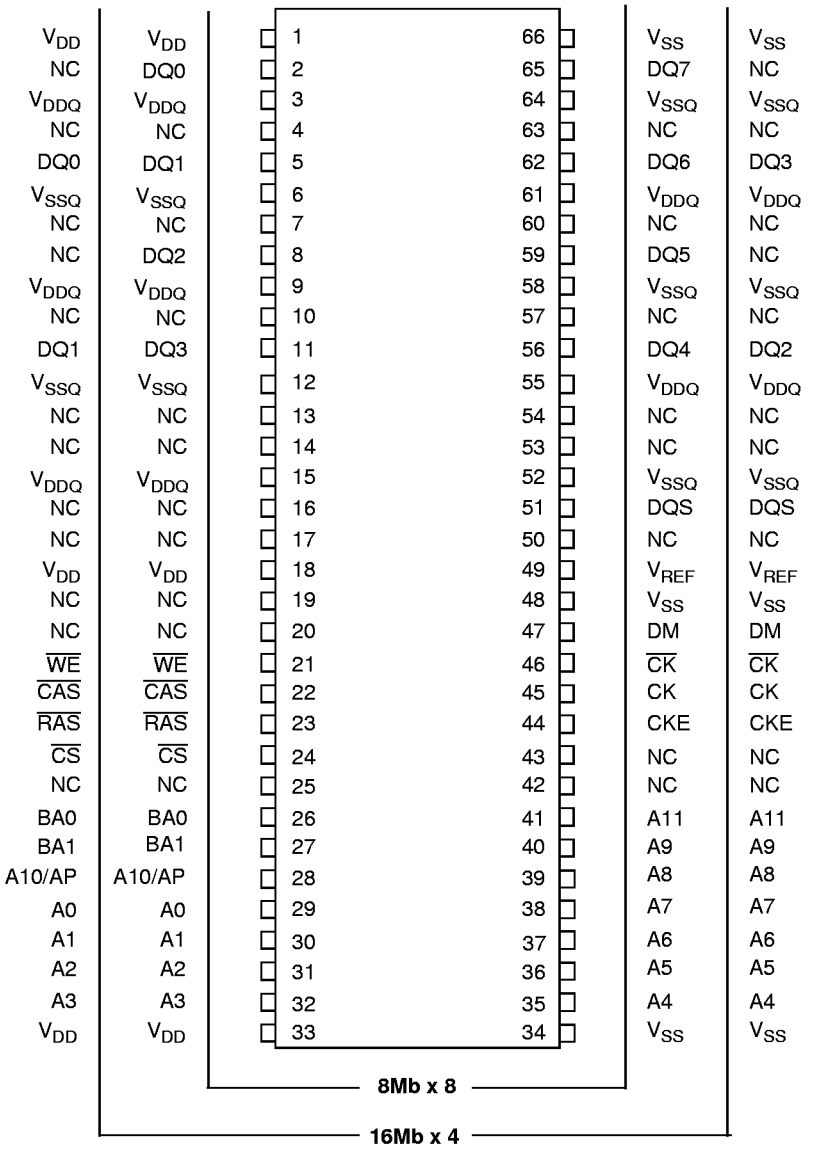
The IBM0664404ET3A and IBM0644804ET3A DDR SDRAMs are high speed CMOS 64Mb Double Data Rate (DDR) Synchronous DRAM devices, organized as x4 and x8, respectively. These devices are four (4) bank SDRAMs, but unlike preceding SDRAMs, these devices incorporate an additional bi-directional data strobe pin (DQS) to allow high speed read and write operations on both edges of the system clock. During Read operation, the DRAM drives a data strobe off chip along with the output data. Here, the data strobe is aligned with the leading edge of the valid output data window. During Write operation, input data, data mask, and a data strobe are supplied to the DRAM by a memory controller. The data strobe generated by the controller should be nominally centered within the valid data-input window. Unlike previous generation SDRAMs, DDR SDRAM devices require a write latency of one clock cycle for input data and mask data with respect to the Write command. This latency reduces chip power dissipation by allowing data input receivers to remain powered down until Write commands are registered by the device.

DDR devices also integrate an on-chip DLL (Delay Locked Loop) circuit to shift the output data in time such that the output data is nominally aligned with the input clock of the DRAM (CK). The DLL will stay locked to the input clock as long as the input clock frequency remains within the valid operating range for DLL operation. The DLL is only used to shift the output data with respect to the input clock and can be disabled through a mode register set command to save power or when it is desired to slow the clock frequency beyond the minimum specified range for proper DLL operation.

An Auto Precharge function can be enabled to provide a self-timed precharge at the end of the burst read or write operation. Once an Auto Precharge command is issued, it is forbidden to issue a new command to terminate or interrupt the operation. An Auto Refresh mode is provided in addition to a power saving Power Down mode.

The DDR devices use a 2-bit prefetch internal pipelined architecture to achieve high speed operation, which allows the column address to be changed every clock cycle (1N rule). Interleaved bank operation can hide precharge cycles and provide seamless high speed random operation within the device. The part is designed to operate with a 3.3V power supply.

Pin Configuration



Pin Description

Symbol	Function	Symbol	Function
CK, $\overline{CK}$[1]	Differential System Clock Inputs	A_0-A_8	Column Address Inputs (x8)
CKE	Clock Enable	DQS	Bidirectional Data Strobe
$\overline{CS}$	Chip Select	DM	Data Input Mask
$\overline{RAS}$	Row Address Strobe	DQ_0-DQ_7	Data Inputs/Outputs (DDR)
$\overline{CAS}$	Column Address Strobe	NC	No Connection (Chip to pin)
$\overline{WE}$	Write Enable	V_{DD}	Supply Voltage
BA_0, BA_1	Bank Selects (4 Bank)	V_{SS}	Ground
A_0-A_{11}	Row Address Inputs	V_{DDQ}	Supply Voltage for DQs
A_{10}/AP	Auto Precharge	V_{SSQ}	Ground for DQs
A_0-A_9	Column Address Inputs (x4)	V_{REF}	Ref. Voltage for SSTL inputs

1. CK and CK must cross each other during transition and the timing reference point for the differential clock pair is at the intersection of CK anc CK. It is permisable to use a single ended CK input to time the DDR device so long as the CK input is connected to V_{REF}.

Input/Output Functional Description

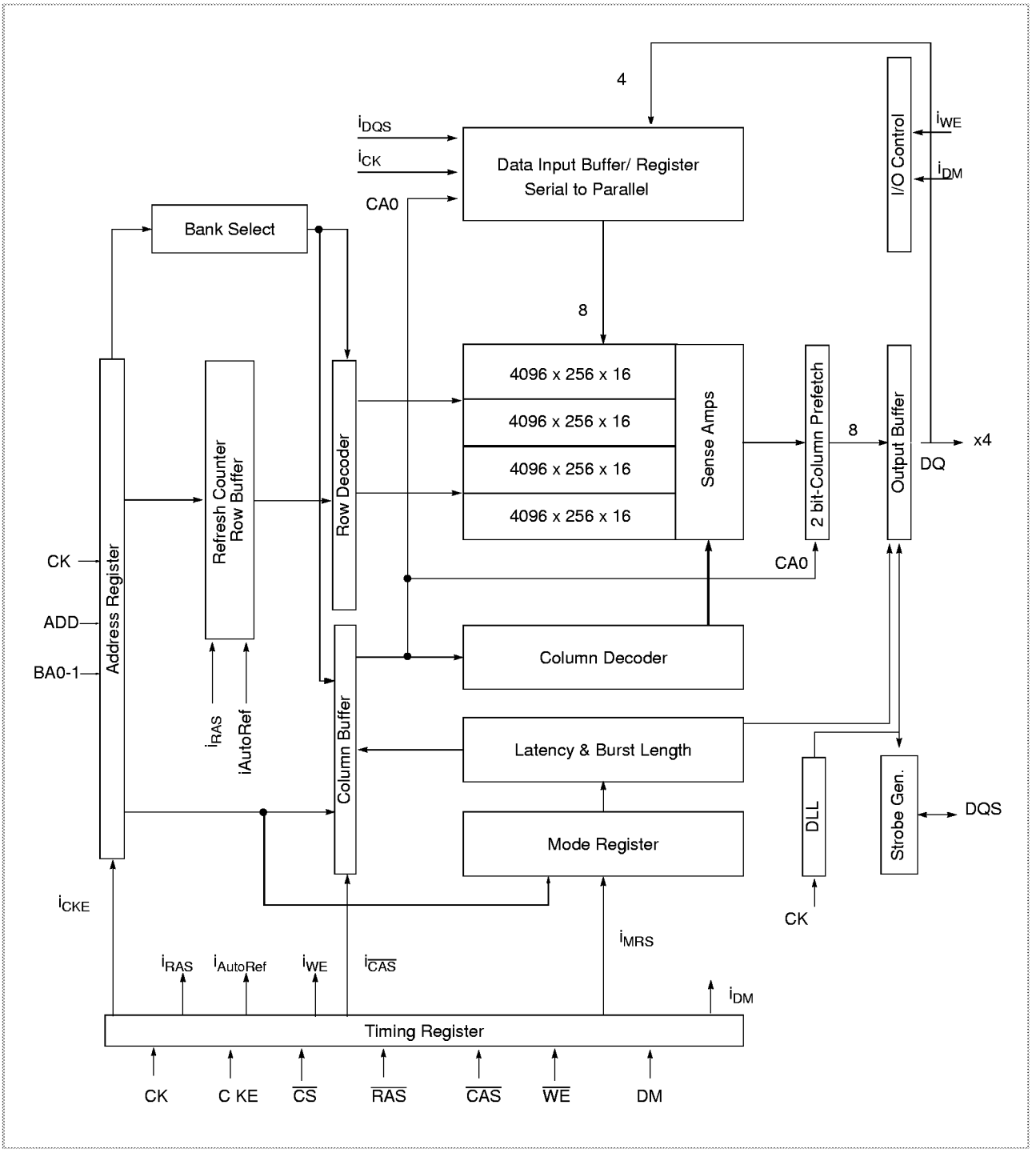
Symbol	Type	Function
CK, $\overline{CK}$	Input (SSTL)	The differential system clock inputs. All of the SDRAM inputs are sampled on the rising edge of the clock except DQs and DMs which are sampled on both edges of the DQS.
CKE	Input (SSTL)	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low indicates the Power Down mode or the Self Refresh mode.
$\overline{CS}$	Input (SSTL)	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input (SSTL)	Control inputs that are issued to the command decoder. See the Operative Command Table (Part 1 of 6) beginning on page 34 for details.
$\overline{CAS}$	Input (SSTL)	
$\overline{WE}$	Input (SSTL)	
DQS	Input/Output (SSTL)	Data Strobe for input and output data, active on both edges.
DM	Input (SSTL)	Masks Write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the Write command is registered into the SDRAM.
DQ_0 - DQ_7	Input/Output (SSTL)	Data Inputs/Outputs are multiplexed on the same pins.
BA_0, BA_1	Input (SSTL)	Selects which bank is to be active.
A_0 - A_{11}	Input (SSTL)	Row/Column addresses are multiplexed on the same pins. Row addresses: RA_0-RA_{11}; Column addresses: CA_0-CA_9. Address A_{10} issued at Column time is used to invoke or disable Auto Precharge.
V_{DD}, V_{SS}	Supply	Power and ground for the input buffers and the core logic.
V_{DDQ}, V_{SSQ}	Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Supply	Reference voltage for SSTL inputs.

Ordering Information

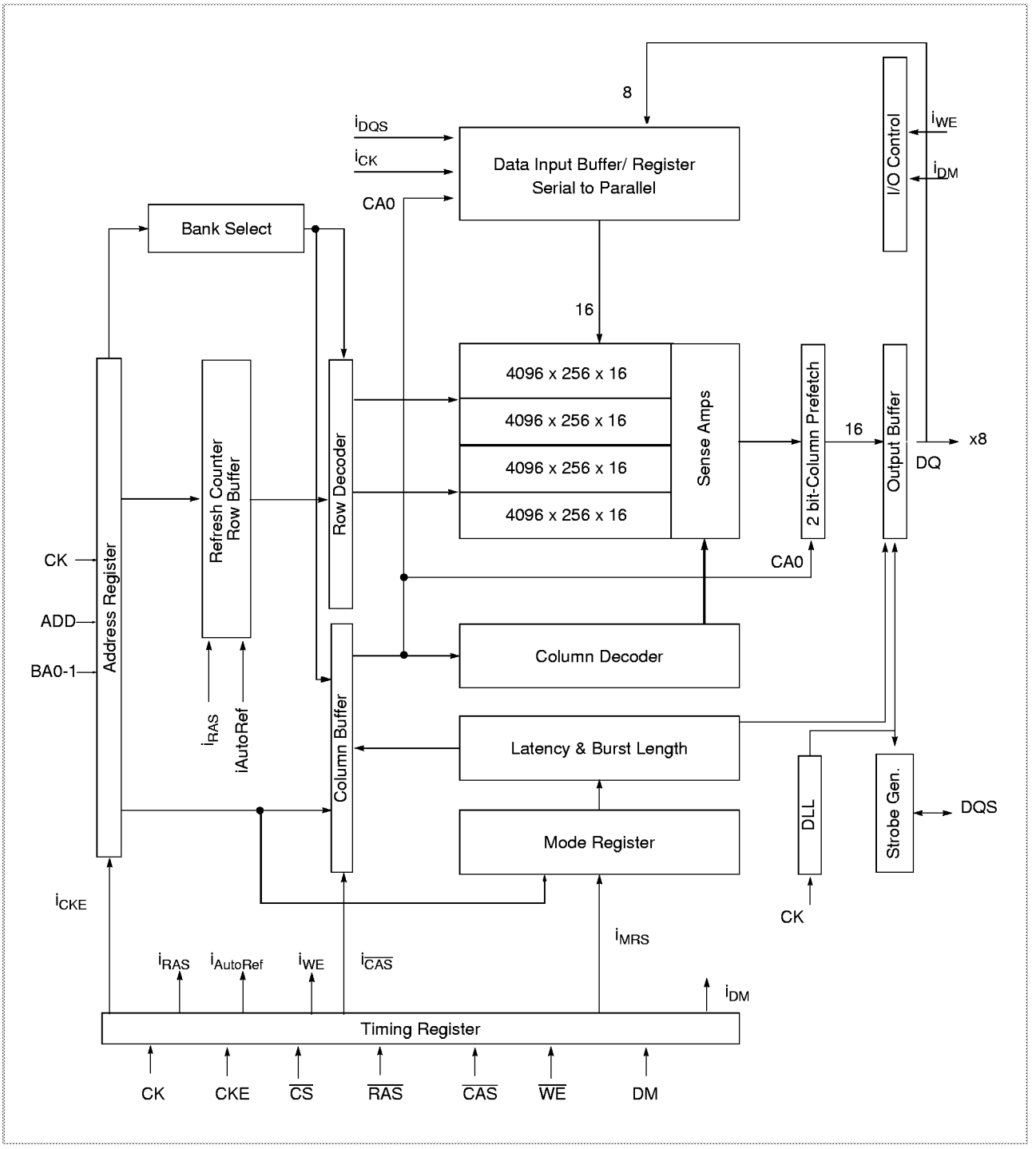
Part Number	Power	Self Refresh	Power Supply	Speed	Package	Notes
IBM0664404ET3A-10	SP	Y	3.3V	100	66 pin TSOP-II	1
IBM0664404ET3A-12				83		
IBM0664804ET3A-10	SP	Y	3.3V	100	66 pin TSOP-II	1
IBM0664804ET3A-12				83		

1. SP = Standard Power.

16Mb x 4 Block Diagram



8Mb x 8 Block Diagram



Power-Up Sequence to Enable and Reset (Lock) the DLL

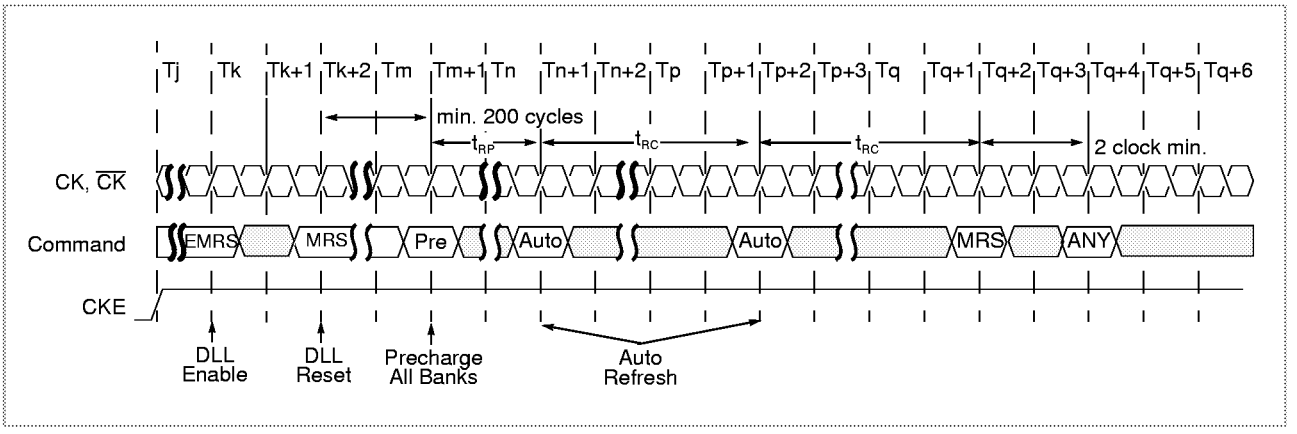
Description

The following sequence is recommended for Power-Up.

1. Apply power and attempt to maintain CKE below 0.8V. Apply VDD before or coincidentally with VDDQ. Apply VDDQ before or coincidentally with VTT and V_{REF}
2. Start the clocks (CK and $\overline{CK}$).
3. Maintain stable power, stable clock and a NOP condition at the inputs for a minimum of 200µs.
4. Take the CKE pin above 2.0V.
5. Issue the Extended Mode Register Set command for “DLL Enable”. Issue a Mode Register Set command for “DLL Reset”. Wait an additional 200 clock cycles to lock the DLL.
6. Issue a Precharge command for all banks of the device.
7. Issue two or more Auto Refresh commands.
8. Issue a Mode Register Set command to initialize the device for the desired operating mode.

Note: Steps 7 and 8 can be reversed (the order is irrelevant).

Power-Up Command Sequence



Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of the DDR SDRAM. It is used to program $\overline{CAS}$ latency, addressing mode, burst length, test mode, DLL reset, and various other specific options to make the DDR SDRAM useful for a variety of applications. The default value of the mode register is not specified at Power-Up, therefore the mode register must be written after Power-Up to select the operating mode of the device. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The DDR SDRAM should be in an idle state (non-power down mode) with CKE already high prior to programming the mode register. The address pins (A_0-A_{11} and BA_0-BA) must be defined during the same cycle when the mode register set command is issued. Two clock cycles are required to complete the write operation in the mode register. The mode register contents can be changed via the MRS command when all banks are in the idle state.

The mode register is divided into various fields depending on functionality. The burst length uses A_0-A_2, burst type uses A_3, and $\overline{CAS}$ latency (read latency from column address) uses A_4-A_6. A_7-A_8 is used to define test mode, DLL Reset, or normal operation. BA_0 and BA_1 must be set to low to enable the normal mode register functions. Refer to the Extended Mode Register Functions table for additional DDR programmable modes.

Mode Register Functions

BA_1	BA_0	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address Key
0	0	RFU			Mode		$\overline{CAS}$ Latency			BT	Burst Length			Mode Register

A_8	A_7	Operating Mode
Ø	Ø	Normal
1	Ø	Reset DLL
1	1	Test Mode

A_3	Burst Type
Ø	Sequential
1	Interleave

$\overline{CAS}$ Latency

A_6	A_5	A_4	Latency
Ø	Ø	Ø	Reserved
Ø	Ø	1	Reserved
Ø	1	Ø	2
Ø	1	1	3
1	Ø	Ø	Reserved
1	Ø	1	Reserved (1.5)
1	1	Ø	2.5
1	1	1	Reserved (3.5)

Burst Length

A_2	A_1	A_0	Sequential	Interleave
Ø	Ø	Ø	Reserved	Reserved
Ø	Ø	1	2	2
Ø	1	Ø	4	4
Ø	1	1	8	8
1	Ø	Ø	Reserved	Reserved
1	Ø	1	Reserved	Reserved
1	1	Ø	Reserved	Reserved
1	1	1	Reserved	Reserved

* RFU (Reserved for future use)
should stay "0" during MRS cycle.

Extended Mode Register Set (EMRS)

The extended mode register provides extended address space for additional JEDEC approved DDR operating modes. This extended address space is accessible by driving Bank Address BA_0 high when the mode register set command is issued. Address bit A_0 defines whether the DLL is enabled or disabled. Address bits A_{1-11} are reserved at this time.

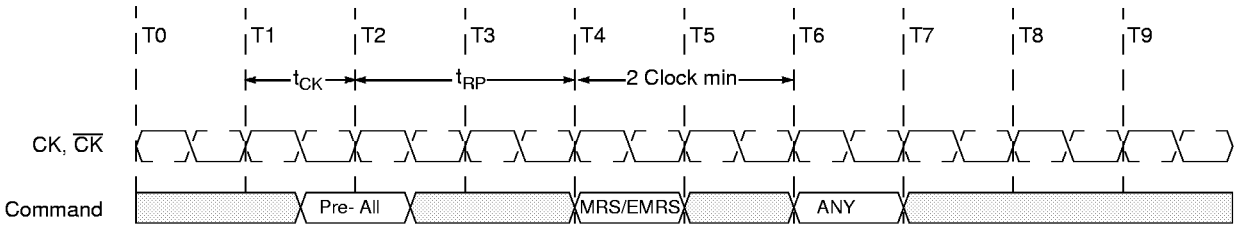
Extended Mode Register Functions

BA_1	BA_0	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address Key
0	1	RFU											DLL	Extended Mode Register

A_0	DLL
Ø	Enable
1	Disable

* RFU (Reserved for future use)
should stay "0" during MRS cycle.

Mode Register / Extended Mode Register Set Timing



Mode Register set (MRS) or Extended Mode Register Set (EMRS) can be issued only when all banks are in the idle state.

If a MRS command is issued to reset the DLL, then an additional 200 clocks must occur prior to issuing any new command to allow time for the DLL to lock onto the clock.

Burst Operation

Burst operation is used to provide a constant flow of data to memory locations (Write cycle) or from memory locations (Read cycle). Two parameters define how the burst mode will operate: burst sequence and burst length. These parameters are programmable and are determined by address bits A_0-A_3 during the Mode Register Set command. Burst type defines the sequence in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequence are supported: sequential and interleave. The burst length controls the number of bits that will be output after a Read command, or the number of bits to be input after a Write command. The burst length can be programmed to have values of 2, 4, or 8. See the Burst Length and Sequence table below for programming information.

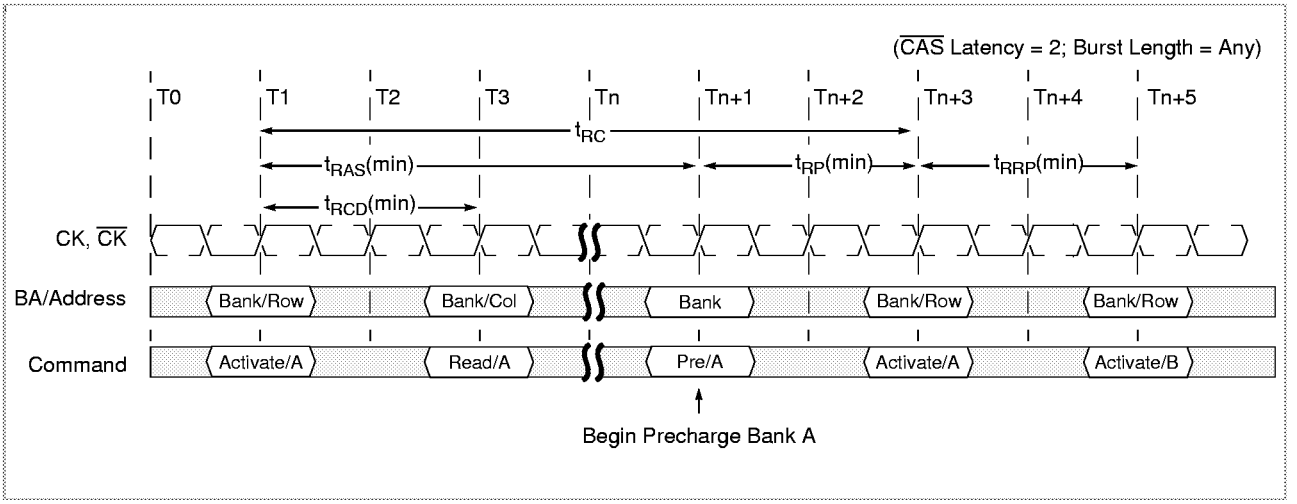
Burst Length and Sequence

Burst Length	Starting Address (A_2, A_1, A_0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The DDR SDRAM has four independent banks, so two Bank Select addresses (BA_0 and BA_1) are supported. The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from the Bank Activate command to the first Read or Write command must meet or exceed the minimum $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD}(min)). Once a bank has been activated, it must meet the Bank Active minimum time (t_{RAS} min) before the bank can be closed. The precharge time must be satisfied (t_{RP}(min)) before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD}(min)).

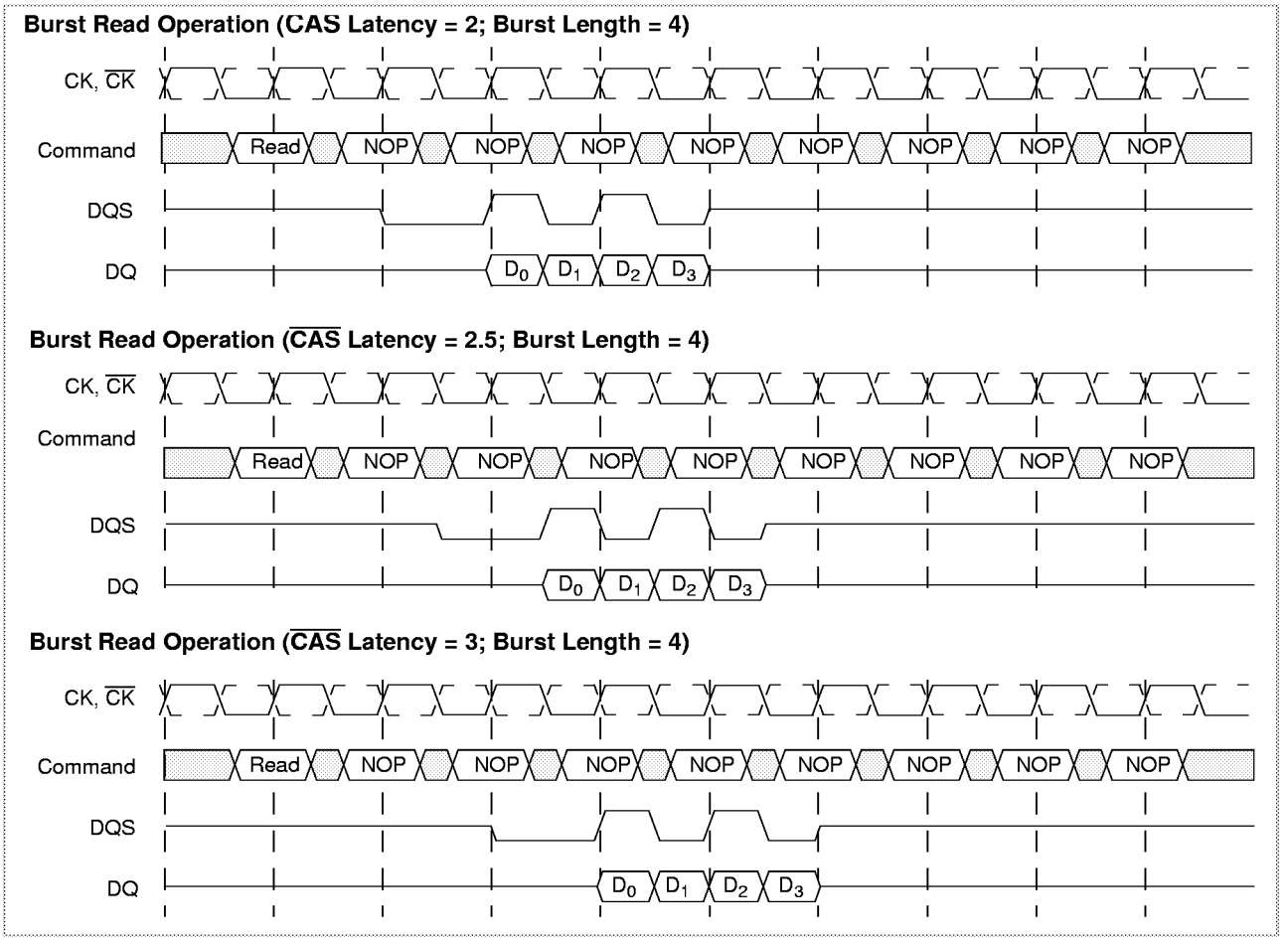
Bank Activation Timing



Burst Read Operation

The Burst Read command in DDR SDRAM, as in traditional SDRAMs, is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock after t_{RCD} from the Bank Activate command. The address inputs determine the starting address of the burst. The Mode Register sets the type of burst (sequential or interleave) and the burst length (2, 4, or 8). The first output data is available after the $\overline{CAS}$ latency from the Read command followed by consecutive data on both the rising and falling edges of the clock (CK) and output data strobe (DQS) until the burst length is completed.

Data Strobe (DQS) and Data (DQ) as a Function of $\overline{CAS}$ Latency for Burst Read Operation



The edges of the output data (DQ) are nominally coincident with the edges of the output data strobe. The output data drivers and output data strobe are driven by the same internal clock phase thus minimizing the skew between DQS and DQ.

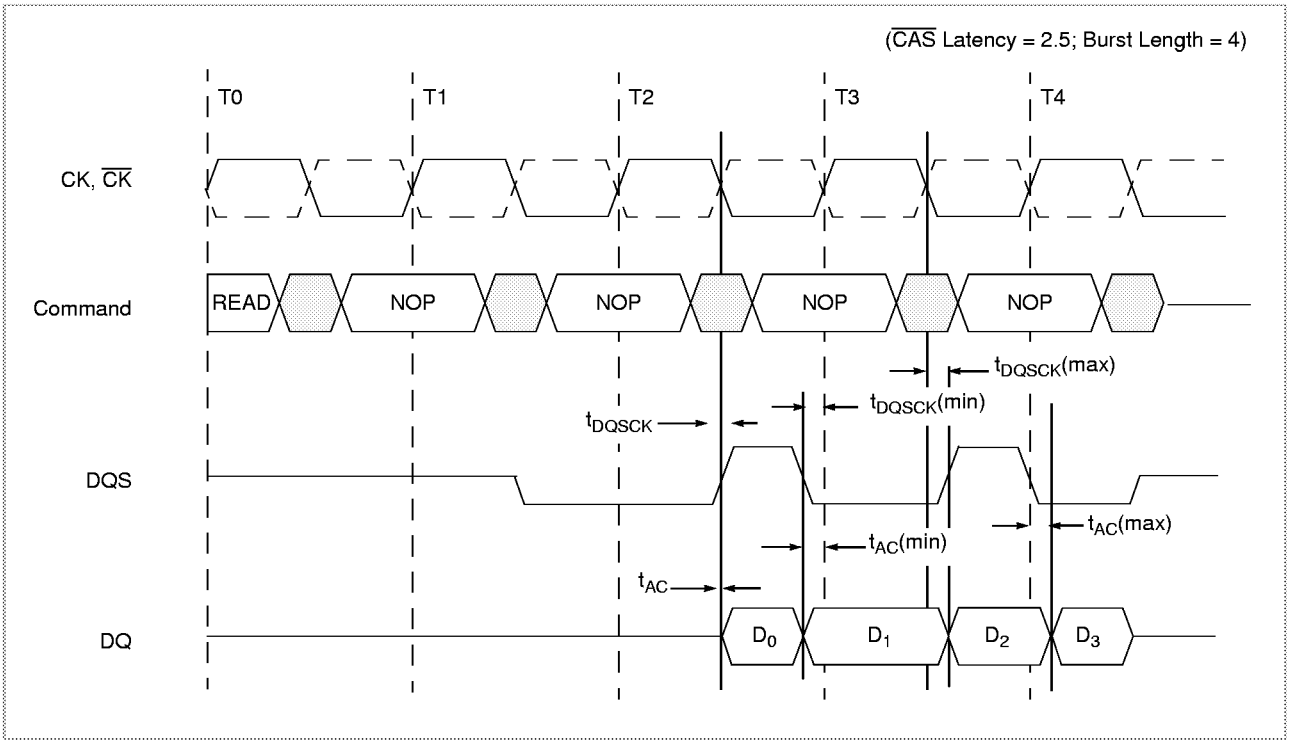
The edges of the output data (DQ) are also nominally coincident with the edges of the input clock (CK) when the DLL is enabled. If the DLL is disabled through the Extended Mode Register command or if the clock frequency falls below the minimum clock frequency required to keep the DLL locked to the input clock, then the output data will no longer track the system clock. The output data will, however, continue to track the data output strobe (DQS) signal.

With the DLL enabled, all devices operating at the same frequency within a system are ensured to have the same timing relationship between DQ and DQS relative to the CK input regardless of device density, process variation, or technology generation.

The data strobe signal (DQS) is driven off chip simultaneously with the output data (DQ) during each read cycle. The same internal clock phase is used to drive both the output data and data strobe signal off chip to minimize skew between data strobe and output data. This internal clock phase is nominally aligned to the input clock (CK) by the on-chip DLL. Therefore, when the DLL is enabled and the clock frequency is within the specified range for proper DLL operation, the data strobe (DQS), output data (DQ), and the system clock (CK) are all nominally aligned.

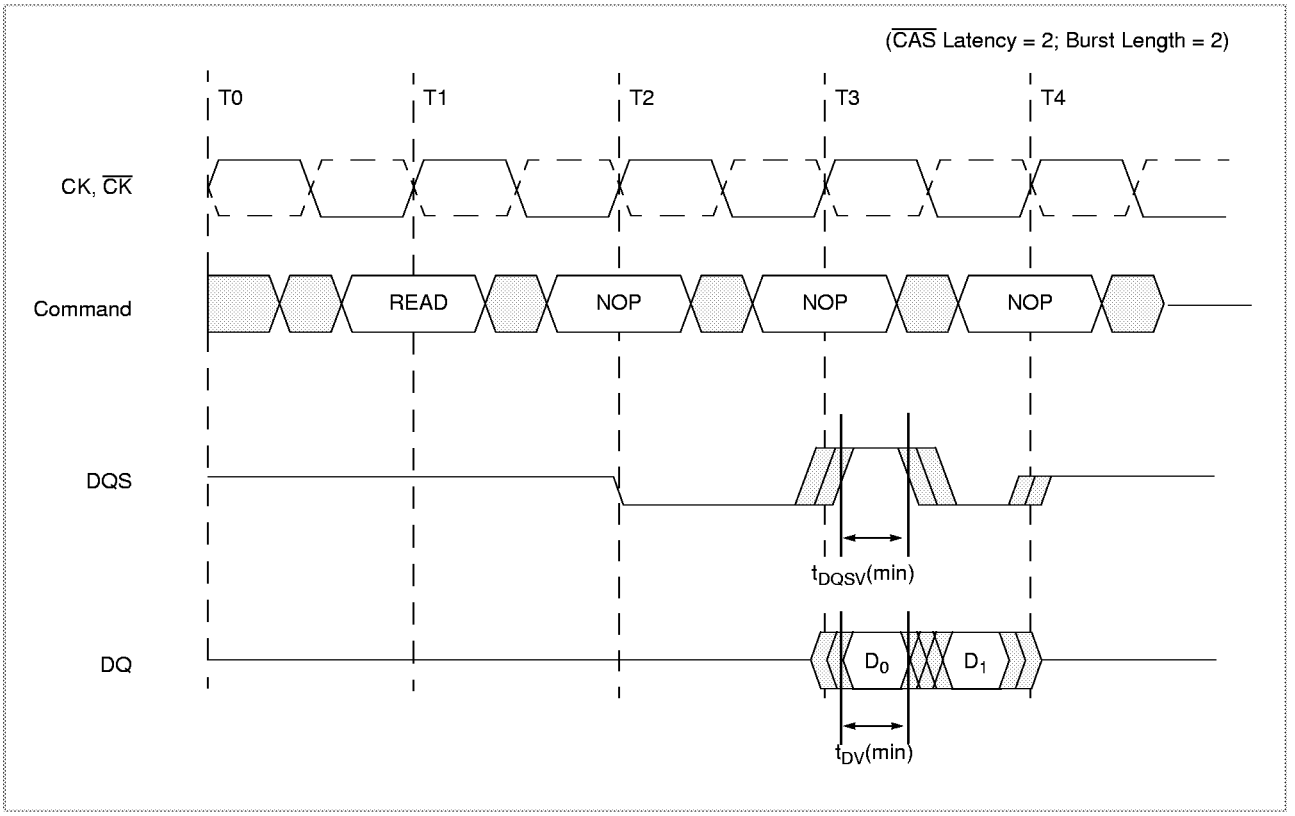
Since the data strobe and output data are tightly coupled in the system, the data strobe signal may be delayed and used to latch the output data into the receiving device. The tolerance for skew between DQS and DQ (t_{DQSQ}) is tighter than that possible for CK to DQ (t_{AC}) or DQS to CK (t_{DQSCK}).

Output Data (DQ) and Data Strobe (DQS) Timing Relative to the Clock (CK) During Read Cycles



The minimum time during which the output data (DQ) is valid is critical for the receiving device (i.e., a memory controller device). This also applies to the data strobe during the read cycle since it is tightly coupled to the output data. The minimum data output valid time (t_{DV}) and minimum data strobe valid time (t_{DQSV}) are derived from the minimum clock high/low time minus a margin for variation in data access and hold time due to DLL jitter and power supply noise.

Output Data and Data Strobe Valid Window for DDR Read Cycles



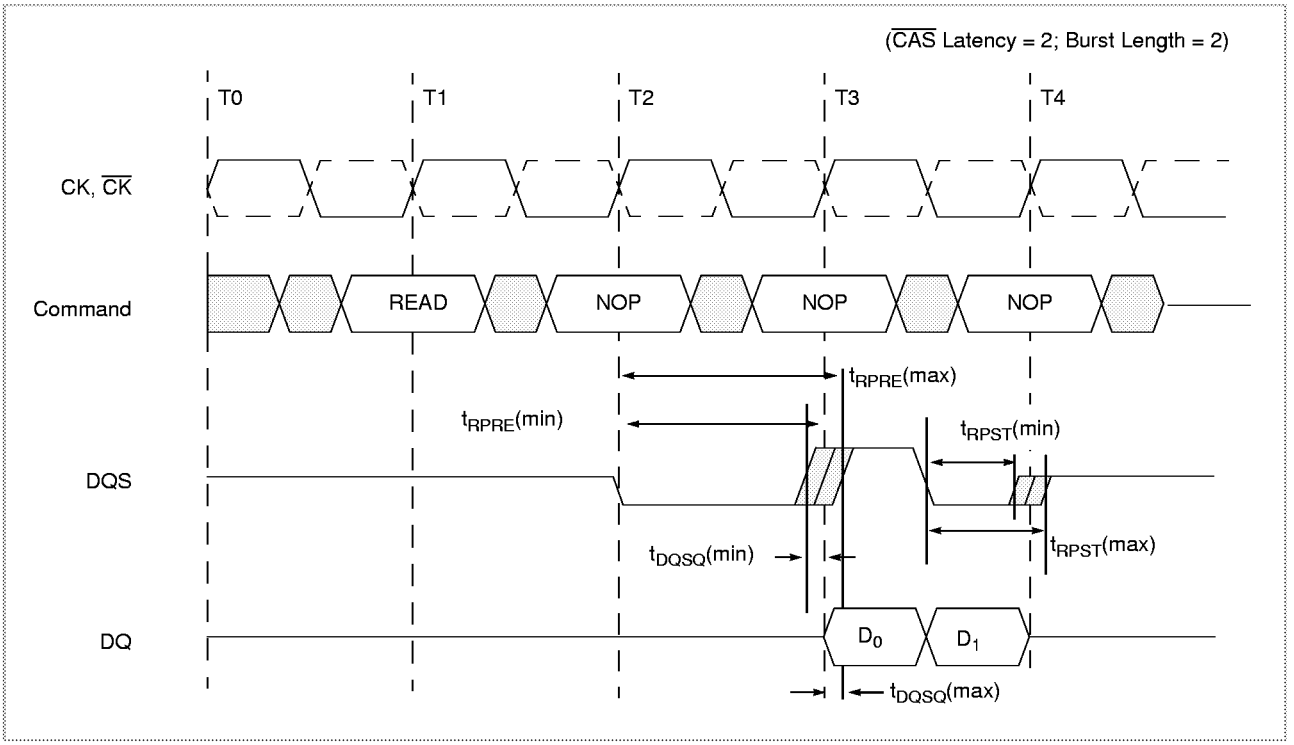
Read Preamble and Postamble Operation

Prior to a burst of read data and given that the controller is not currently in burst read mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. The is referred to as the data strobe “read preamble” (t_{RPRE}). This transition from Hi-Z to logic low nominally happens one clock cycle prior to the first edge of valid data.

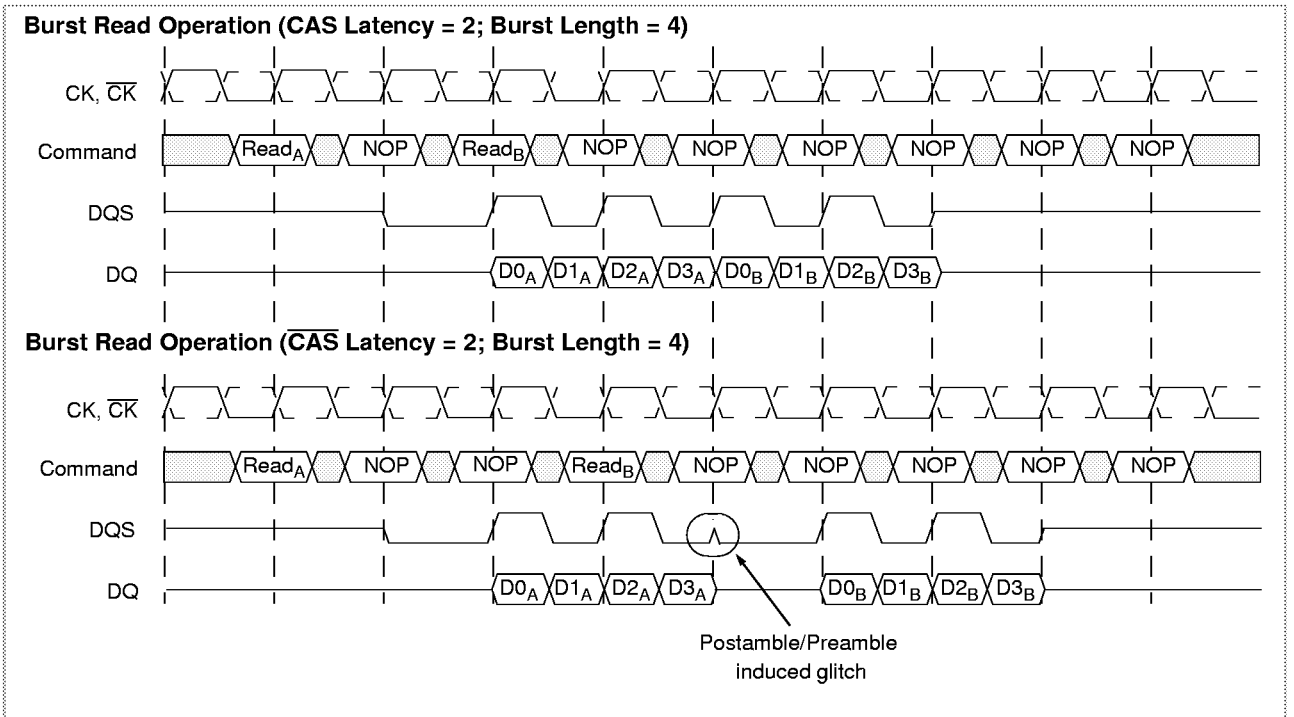
Once the burst of read data is concluded and given that no subsequent burst read operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “read postamble” (t_{RPST}). This transition happens nominally one-half clock period after the last edge of valid data.

Consecutive or “gapless” burst read operations are possible from the same DDR SDRAM device with no requirement for a data strobe “read” preamble or postamble in between the groups of burst data. The data strobe read preamble is required before the DDR device drives the first output data off chip. Similarly, the data strobe postamble is initiated when the device stops driving DQ data at then end or termination of read burst cycles.

Data Strobe Preamble and Postamble Timings for DDR Read Cycles



Consecutive Burst Read Operation and Effects on the Data Strobe Preamble and Postamble

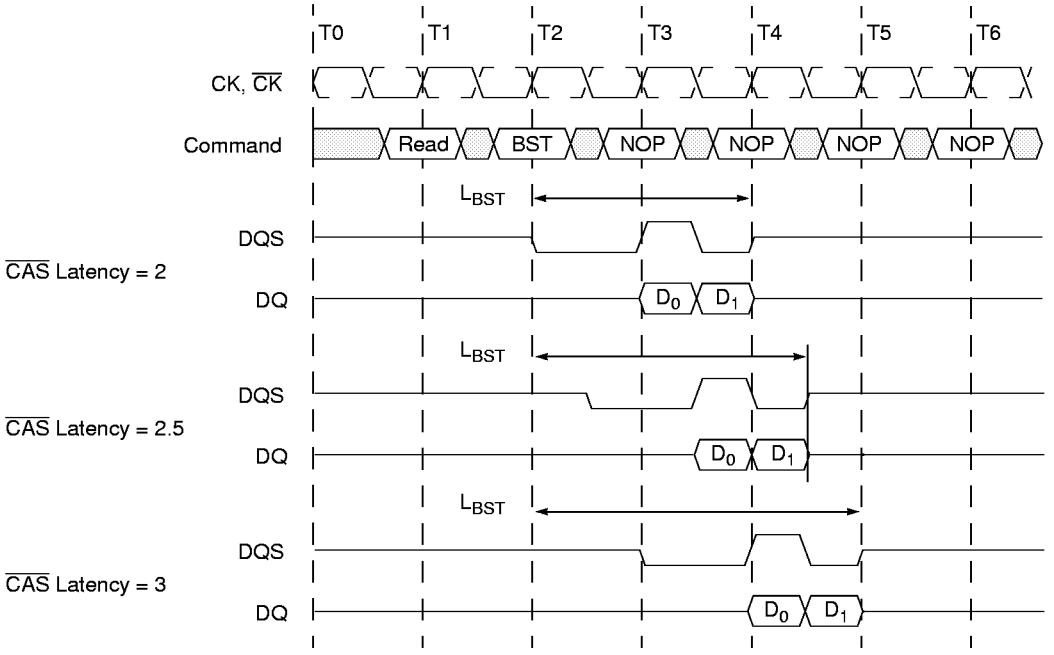


Burst Stop Command

The Burst Stop command is valid only during burst read cycles and is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. When the Burst Stop command is issued during a burst Read cycle, both the output data (DQ) and data strobe (DQS) go to a high impedance state after a delay (L_{BST}) equal to the $\overline{CAS}$ latency programmed into the device. If the Burst Stop command is issued during a burst Write cycle, the command will be treated as a NOP command.

Read Terminated by Burst Stop Command Timing

($\overline{CAS}$ Latency = 2, 2.5, 3; Burst Length = 4)



Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. The memory controller is required to provide an input data strobe (DQS) to the DDR SDRAM to strobe or latch the input data (DQ) and data mask (DM) into the device. During Write cycles, the data strobe applied to the DDR SDRAM is required to be nominally centered within the data (DQ) and data mask (DM) valid windows. The data strobe must be driven high nominally one clock after the write command has been registered. Timing parameters t_{DQSS}(min) and t_{DQSS}(max) define the allowable window when the data strobe must be driven high.

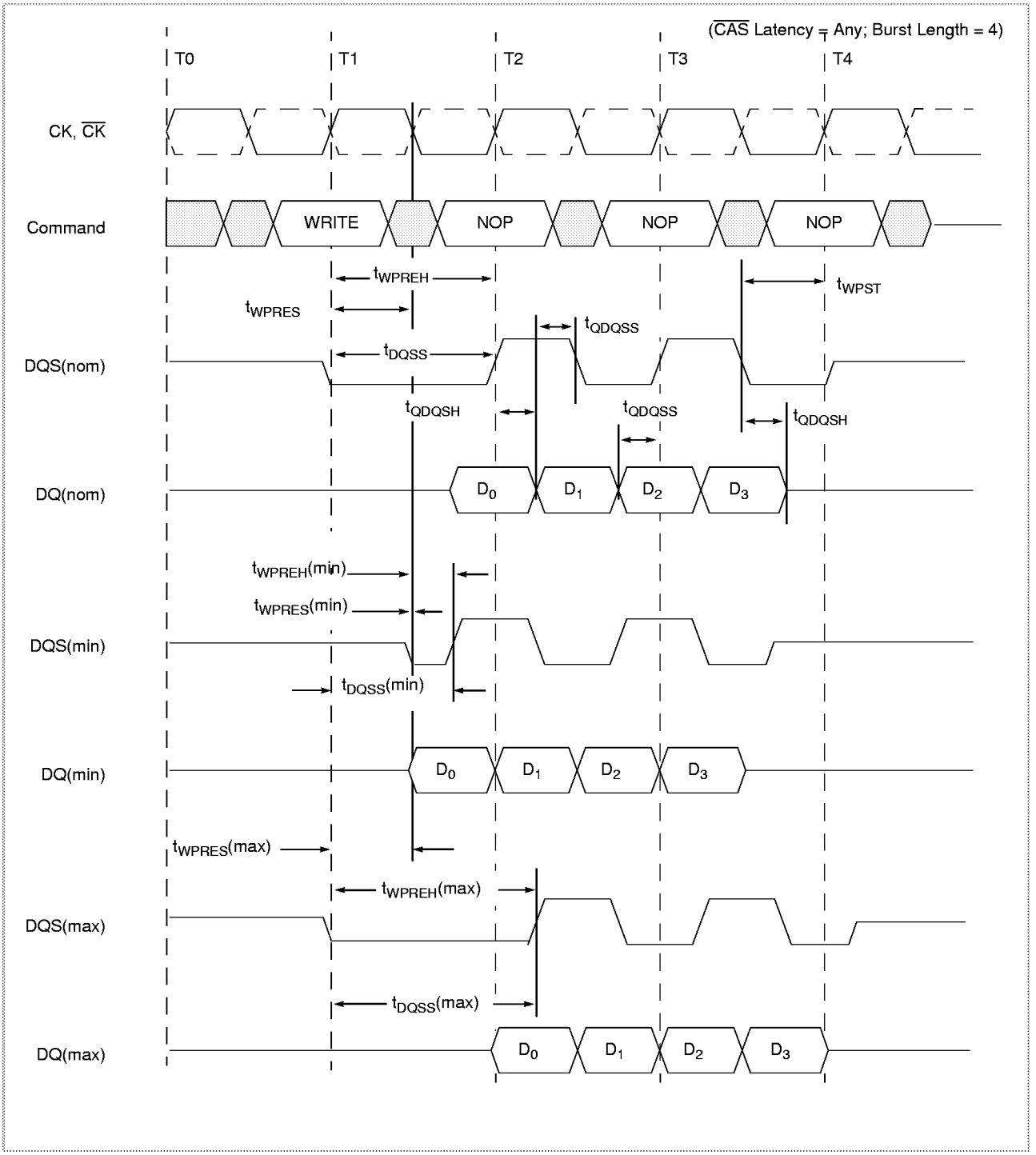
Input data for the first Burst Write cycle must be applied one clock cycle after the Write command is registered into the device (WL=1). The input data valid window is nominally centered around the midpoint of the data strobe signal. The data window is defined by DQ to DQS setup time (t_{QDQSS}) and DQ to DQS hold time (t_{QDQSH}). All data inputs must be supplied on each rising and falling edge of the data strobe until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

Write Preamble and Postamble Operation

Prior to a burst of write data and given that the controller is not currently in burst write mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. This is referred to as the data strobe “write preamble”. This transition from Hi-Z to logic low nominally happens on the falling edge of the clock after the write command has been registered by the device. The preamble is explicitly defined by a setup time (t_{WPRES}(min)) and hold time (t_{WPREH}(min)) referenced to the first falling edge of CK after the write command.

Once the burst of write data is concluded and given that no subsequent burst write operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “write postamble”. This transition happens nominally one-half clock period after the last data of the burst cycle is latched into the device.

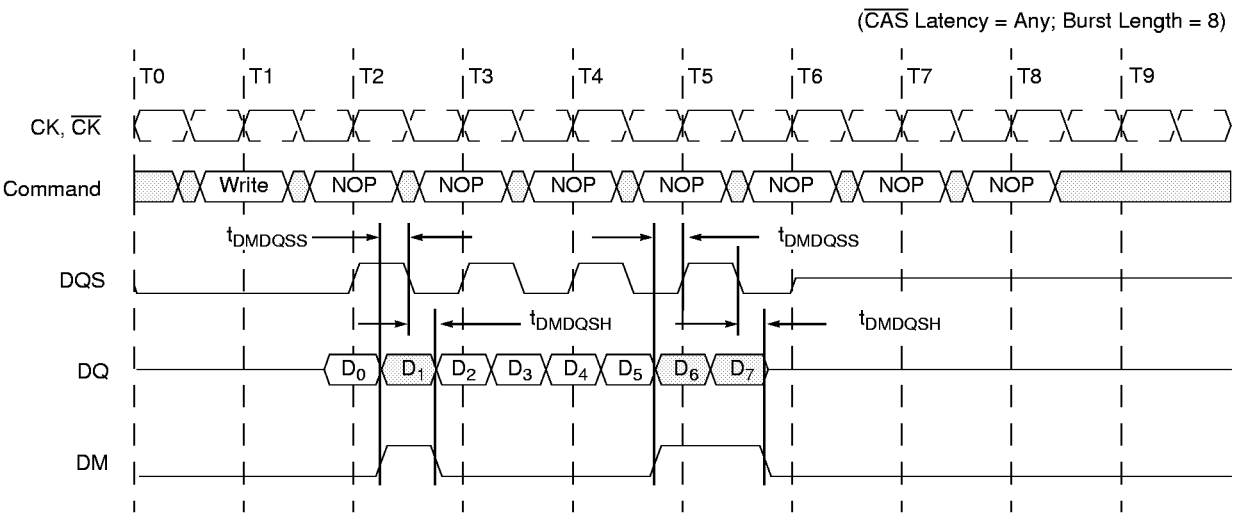
Burst Write Timing (Assumes DM is Low)



Data Mask Function

The DDR SDRAM has data mask capability that can be used to mask the input data during burst write cycles. The data mask has no effect during burst read cycles. The data mask (DM) is applied coincidentally with the input data and must satisfy setup and hold conditions referenced to the data strobe (DQS). The data mask is sampled on each edge of the data strobe during write cycles. When the data mask is activated (DM high) during a Write operation, the Write is blocked to all data inputs associated with the controlling data mask pin for that edge of the data strobe (Mask to Data Latency = 0).

Data Mask Timing



Precharge Command

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is issued when $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. This command can be used to precharge each bank independently or all banks simultaneously. The Bank Select addresses (BA_0, BA_1) are used to define which bank is precharged when the command is initiated. After a specified delay (t_{RP}) from the precharge, a Bank Activate command to the same bank can be initiated.

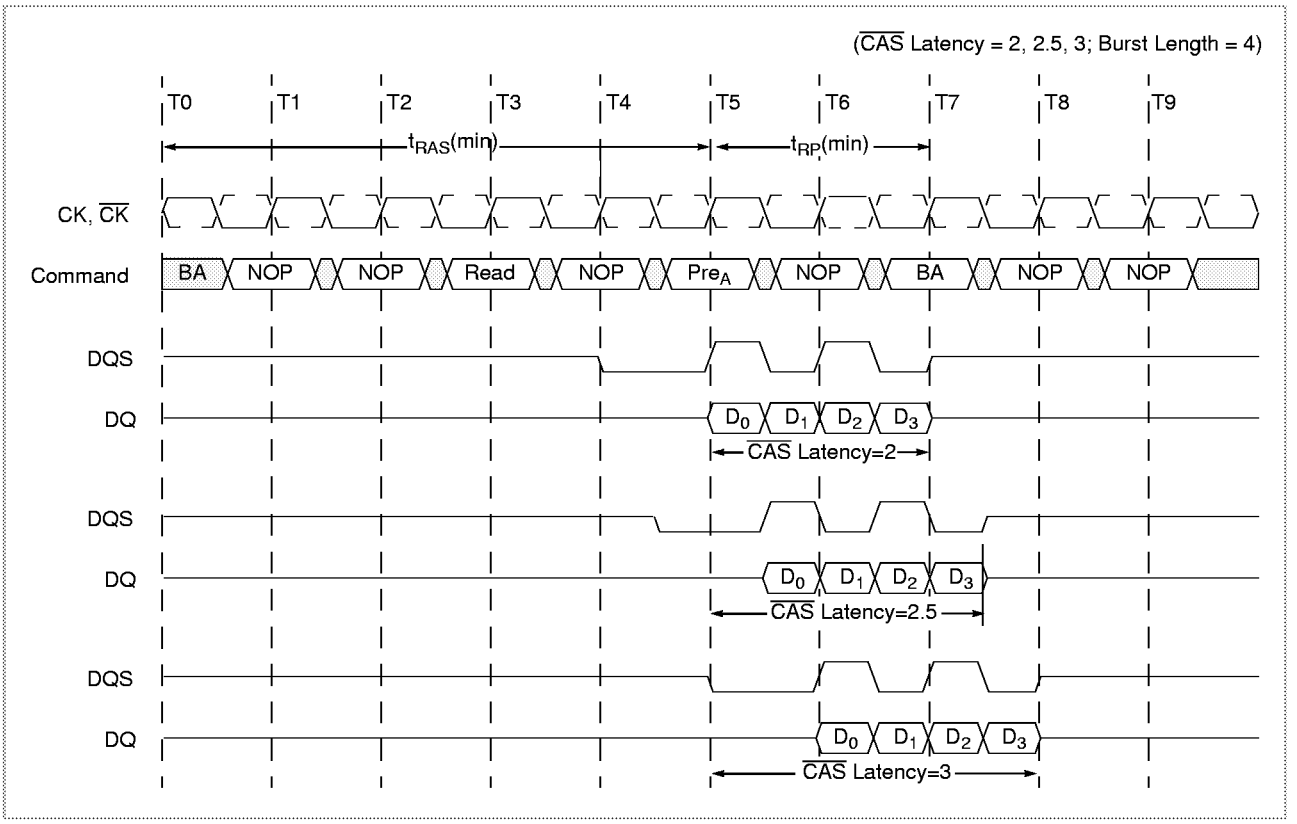
Bank Select for Precharge by Bank Address Bits

A_{10}/AP	BA_1	BA_0	Precharge
0	0	0	Bank A only
0	0	1	Bank B only
0	1	0	Bank C only
0	1	1	Bank D only
1	X	X	All banks

Precharge Timing During Read Operation

For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be issued on the rising clock edge which is $\overline{CAS}$ latency (CL) clock cycles before the end of the Read burst. A new Bank Activate (BA) command may be issued to the same bank after the $\overline{RAS}$ precharge time (t_{RP}). A Precharge command can not be issued until t_{RAS}(min) is satisfied

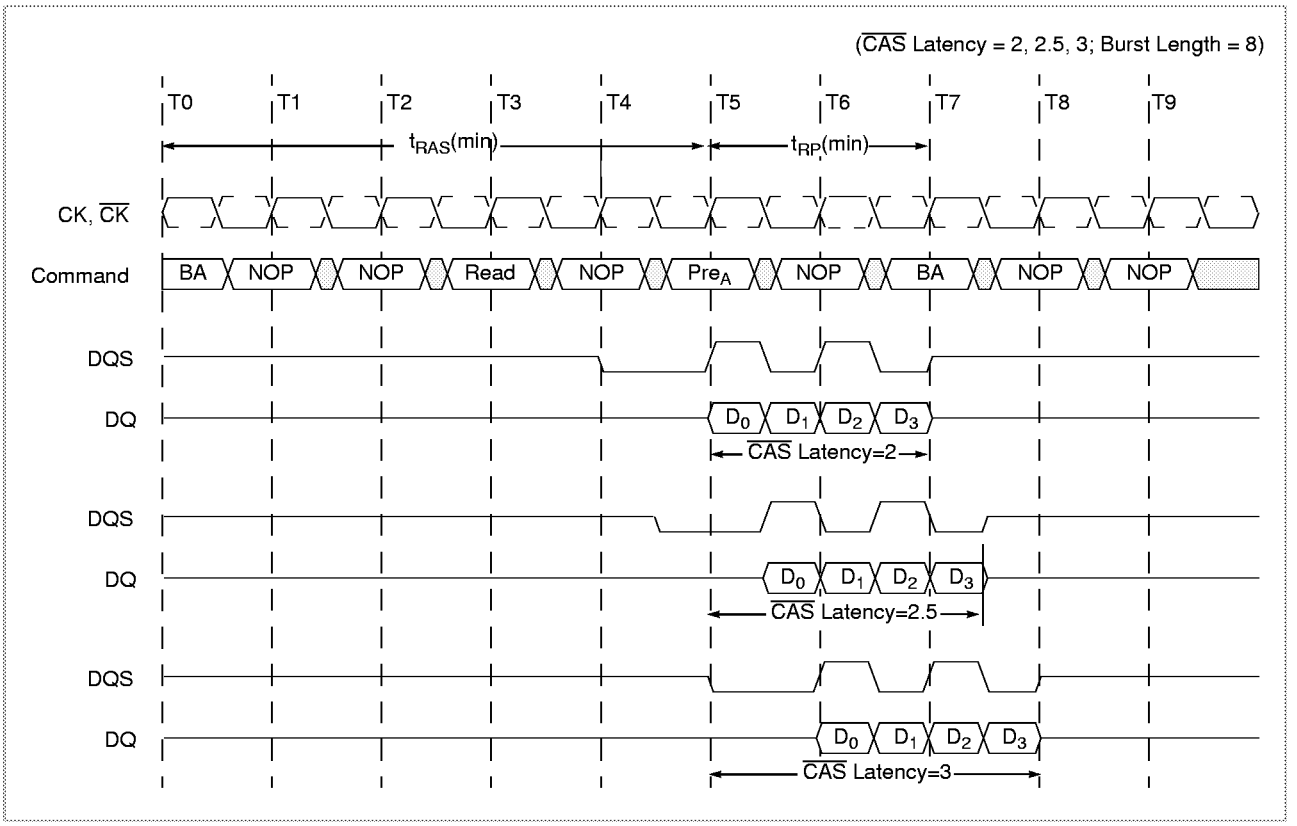
Read with Precharge Timing as a Function of $\overline{CAS}$ Latency



Read Terminated with Precharge Command

A Precharge command can interrupt and terminate a Read burst operation. The Precharge command may be issued on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after the precharge delay is satisfied.

Read Terminated with Precharge Command Timing as a Function of $\overline{CAS}$ Latency



Precharge Timing During Write Operation

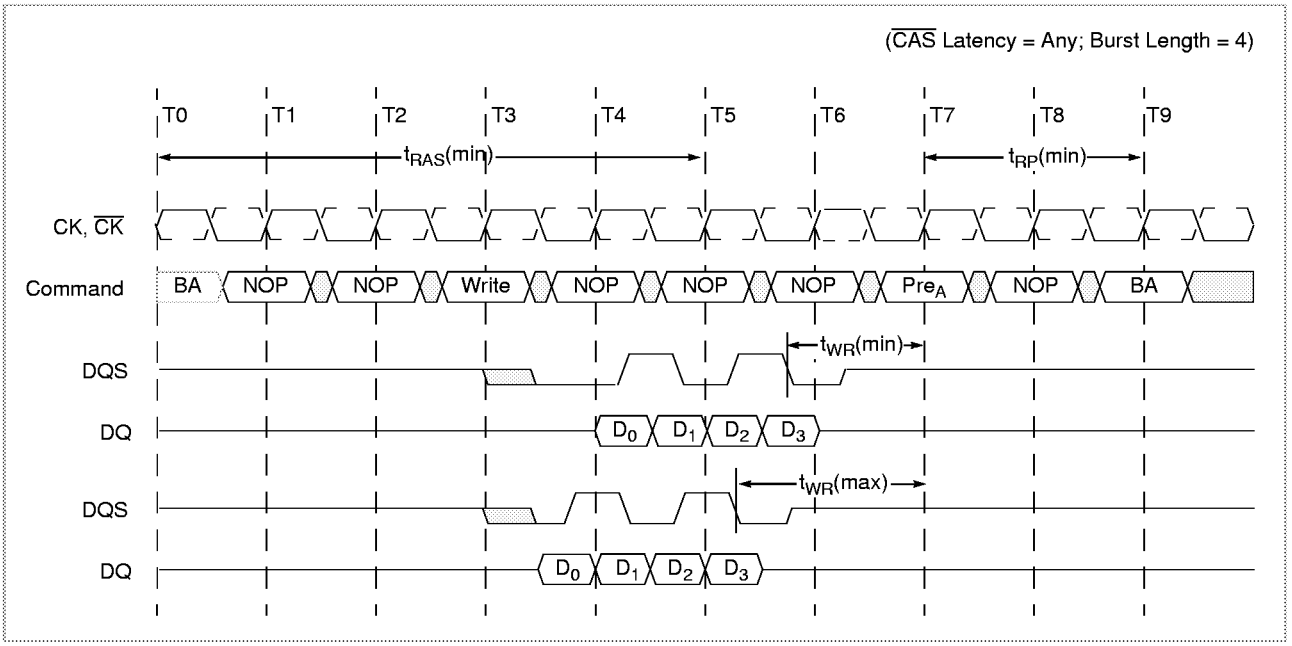
Precharge timing for Write operations in DRAM's requires enough time to allow the "write recovery" to occur. This is the time required by a DRAM sense amp to fully store or "0" or "1" level before isolating the array cell from the bit line. For DDR SDRAMs, a timing parameter (t_{WR}) is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for write operation is a complex function for DDR devices since the write data is latched into the chip by the data strobe and the address is driven or incremented in the chip by the clock input. Inside the device, the data path is eventually synchronized with the address path by switching clock domains from the data strobe domain to the input clock domain. This complicates the definition of when a precharge operation can begin after a write cycle since the "write recovery" period must reference only the clock domain to time the internal write operation.

The "write recovery" operation begins on the rising clock edge after the last DQS edge that is used to strobe in the last valid write data. "Write recovery" is complete on the next rising clock edge that is used to strobe in the Precharge command.

For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for "write recovery" is 1.25 clock cycles. Maximum "write recovery" time is 1.75 clock cycles.

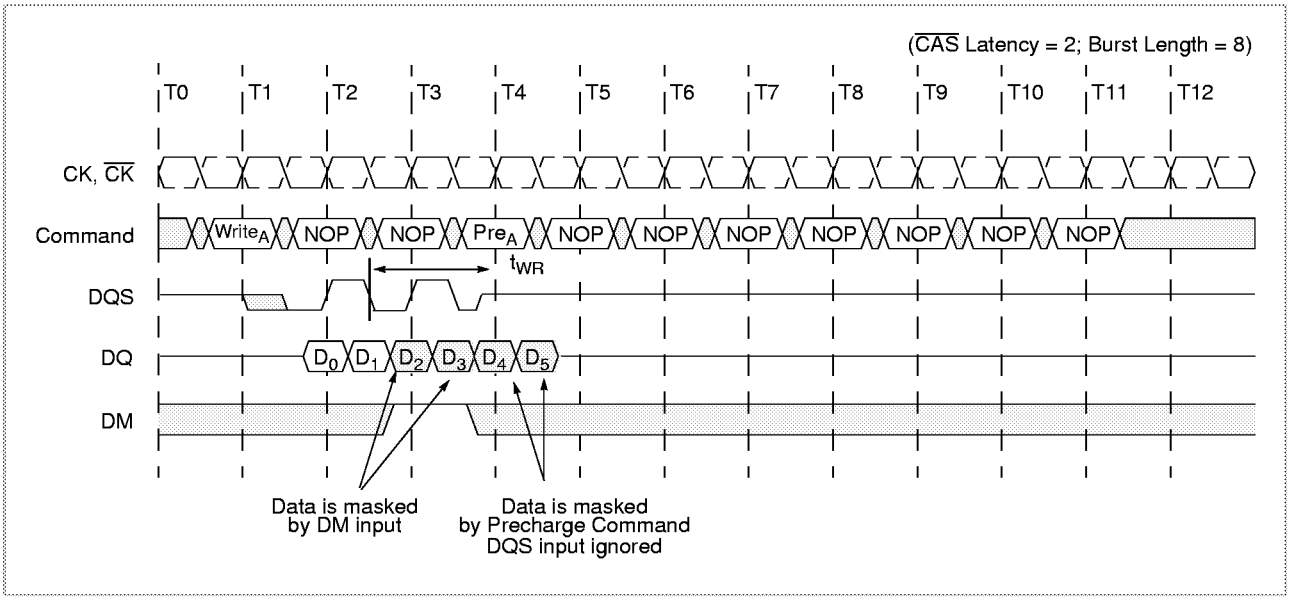
Write with Precharge Timing



Write Terminated with Precharge Command

A Burst Write operation can be interrupted and terminated by a precharge to the same bank. When a precharge command interrupts a Write burst operation, the data mask (DM) input pin is used to mask input data (DQ) during the time between the last valid write data and the rising clock edge on which the Precharge command is issued. During this time, the DQS input is still required to strobe in the state of DM. Any data that is present on the DQ pins coincident with or following the Precharge command will be masked off by the Precharge command and will not be written to the array. The minimum time for write recovery is defined by tWR. It is illegal to interrupt a Write with autoprecharge command with a Precharge command.

Write Terminated with Precharge Command Timing



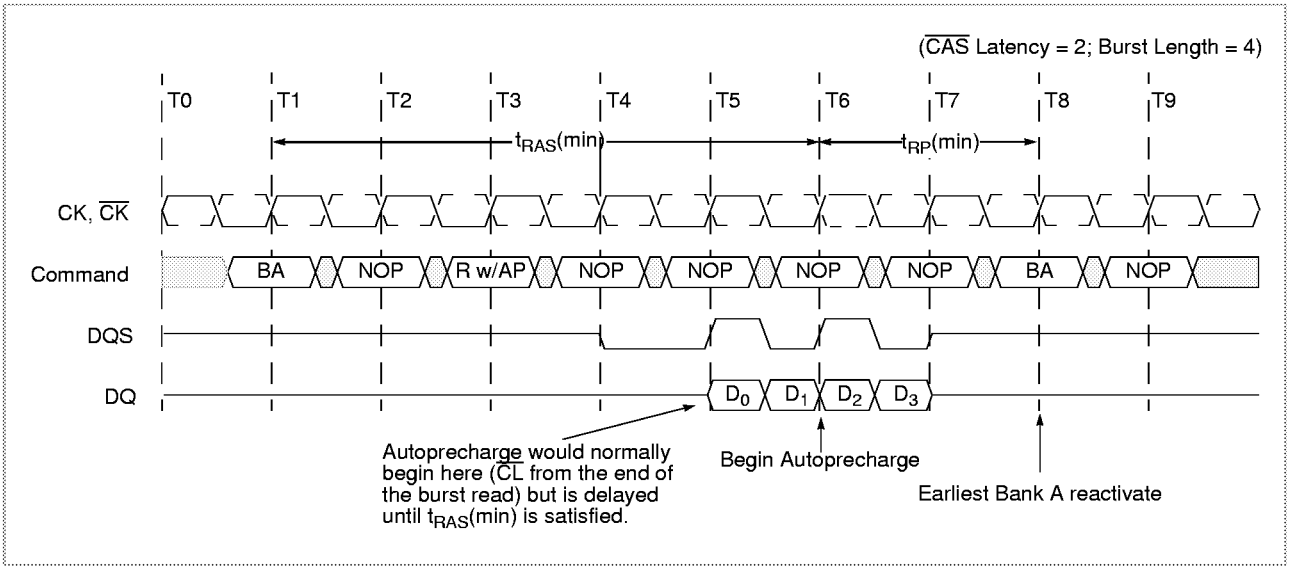
Auto Precharge Operation

The Auto Precharge operation can be issued by having column address A_{10} high when a Read or Write command is asserted. If A_{10} is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle once t_{RAS}(min) is satisfied.

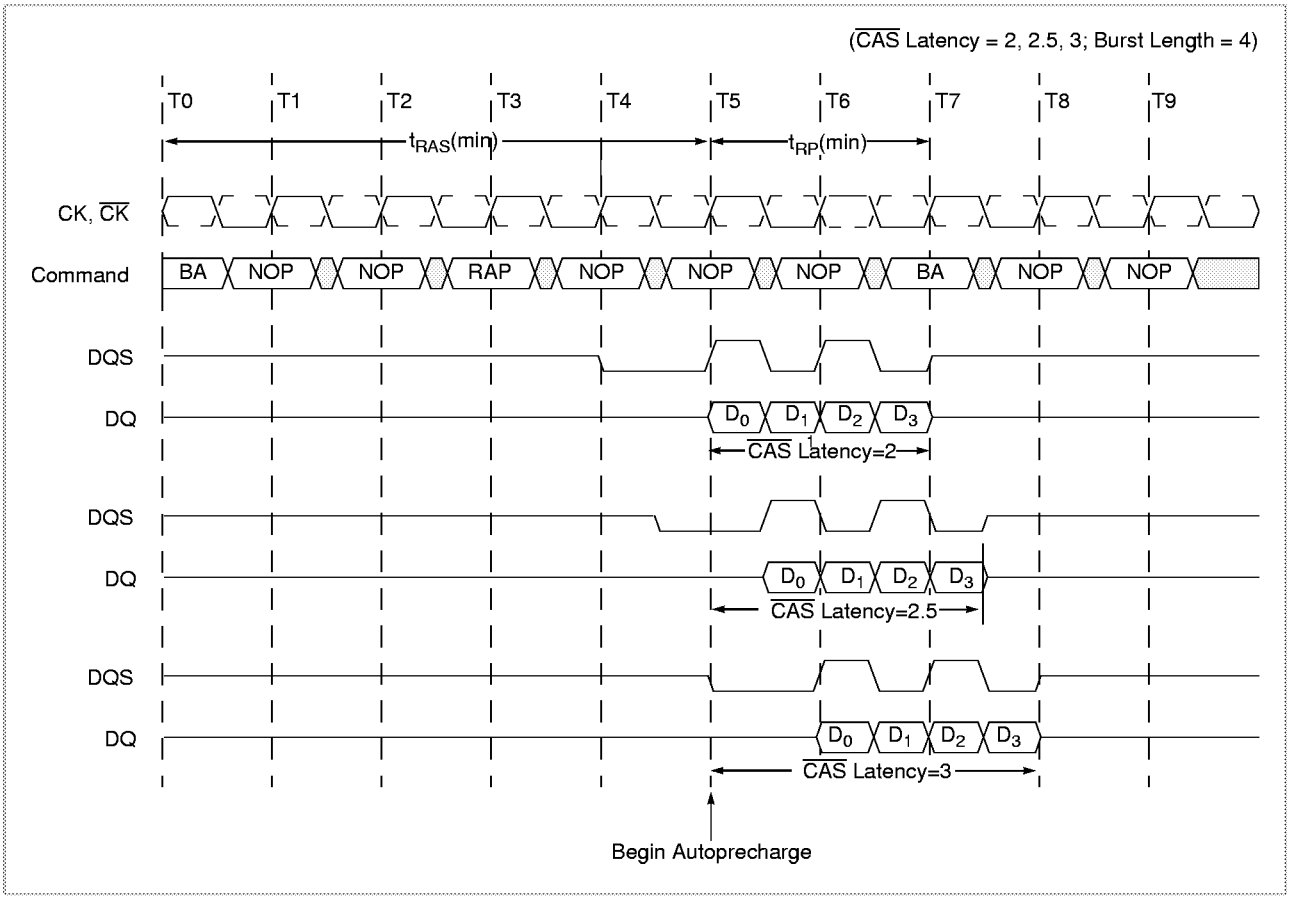
Read with Auto Precharge

If a Read with Auto Precharge command is initiated, the DDR SDRAM will enter the precharge operation N-clock cycles measured from the last data of the burst read cycle where N is equal to the $\overline{CAS}$ latency programmed into the device. If a Read with autoprecharge command is issued before t_{RAS}(min) is satisfied, the precharge operation will be delayed until that time when t_{RAS}(min) is met. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time (t_{RP}) has been satisfied.

Read with Autoprecharge Timing



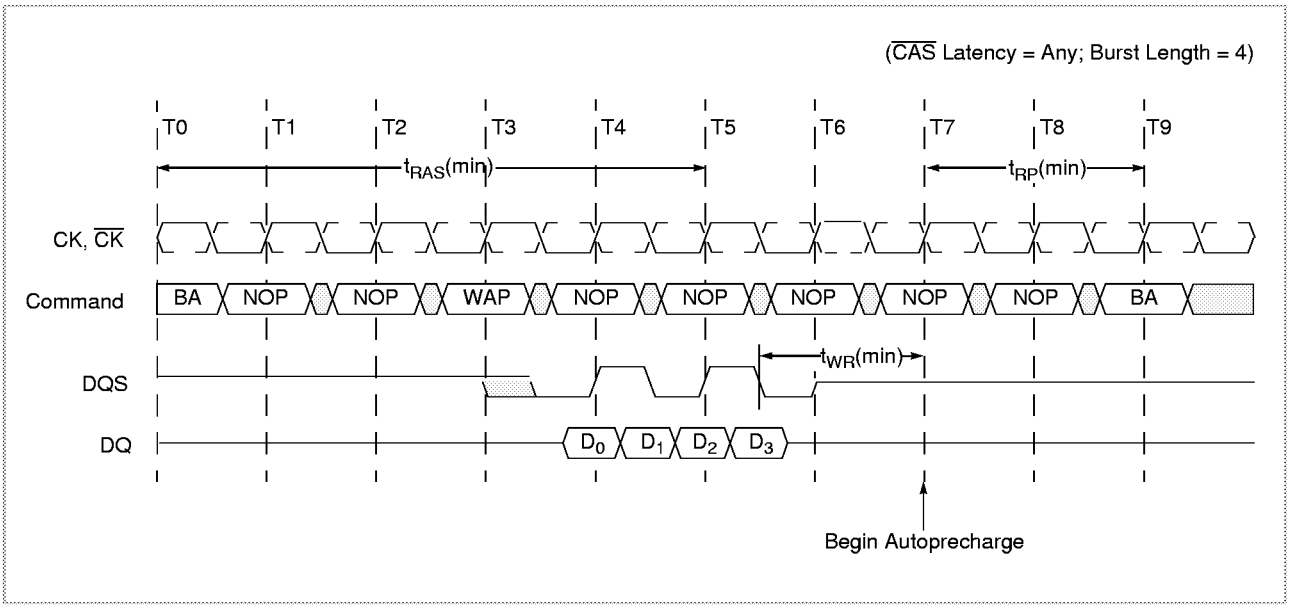
Read with Autoprecharge Timing as a Function of $\overline{CAS}$ Latency



Write with Autoprecharge

If a Write with Autoprecharge command is initiated, the DDR SDRAM will enter the precharge operation a delay (t_{WR}(min)) after the final burst write cycle. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time (t_{RP}) has been satisfied.

Write with Autoprecharge Timing

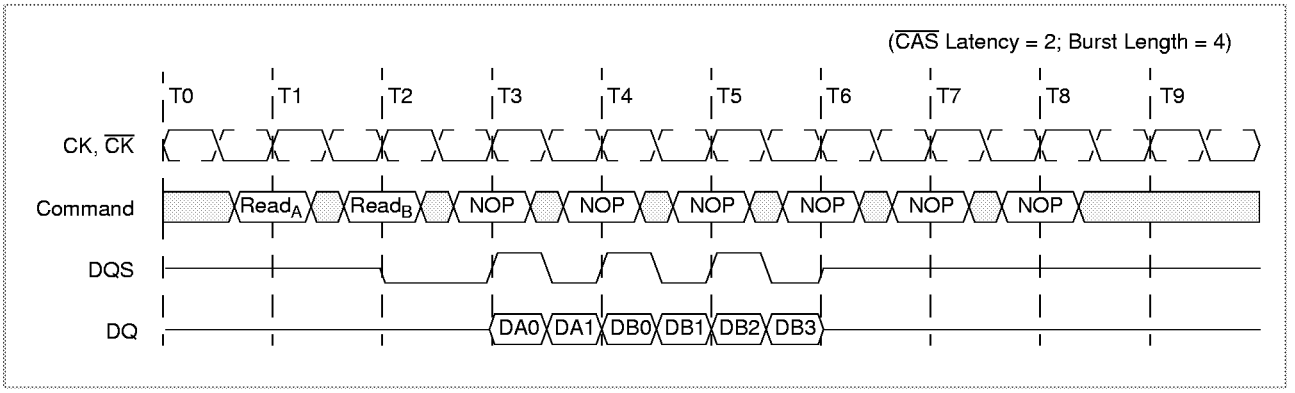


Burst Interruption

Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by issuing a new Read command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears on the bus. Read commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Read with autoprecharge command with a Read command.

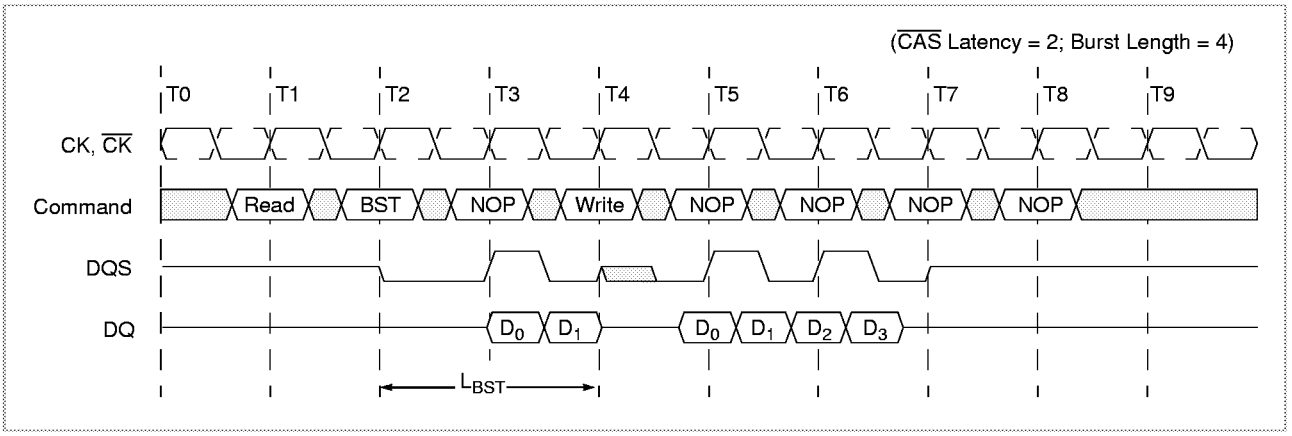
Read Interrupted by a Read Command Timing



Read Interrupted by a Write

To interrupt a Burst Read with a Write command, a Burst Stop command must be asserted to stop the burst read operation and tristate the DQ bus. Additionally, control of the DQS bus must be turned around to allow the memory controller to drive the data strobe signal (DQS) into the DDR SDRAM for the write cycles. Once the Burst Stop command has been issued, a Write command can not be issued until a minimum delay or latency (L_{BST}) has been satisfied. This latency is measured from the Burst Stop command and is equivalent to the $\overline{CAS}$ latency programmed into the mode register. In instances where $\overline{CAS}$ latency is measured in half clock cycles, the minimum delay (L_{BST}) is rounded up to the next full clock cycle (i.e., if CL=2 then L_{BST}=2, if CL=2.5 then L_{BST}=3). It is illegal to interrupt a Read with autoprecharge command with a Write command.

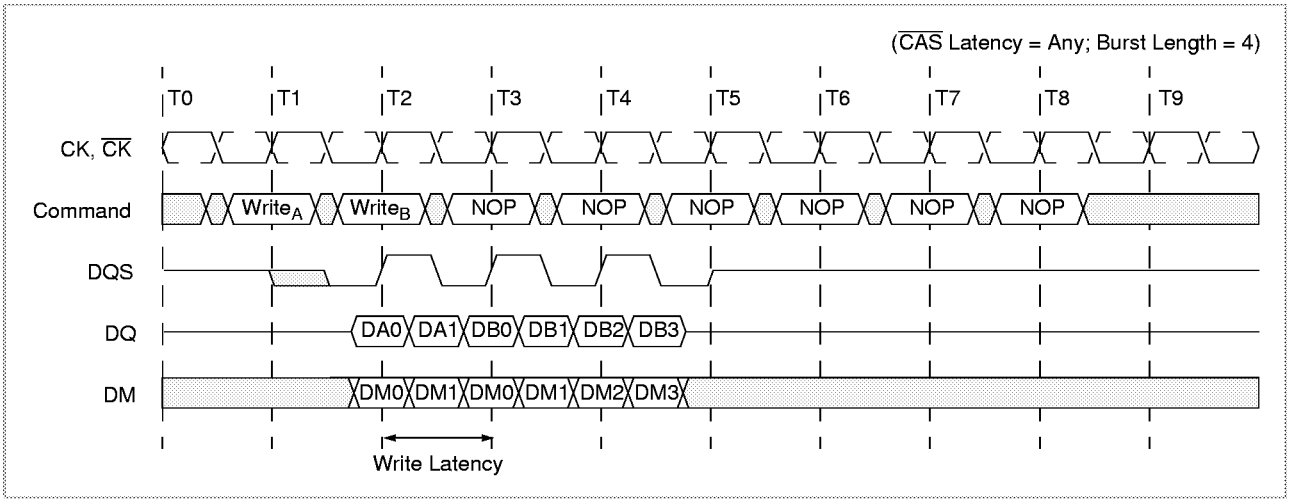
Read Interrupted by Burst Stop Command Followed by a Write Command Timing



Write Interrupted by a Write

A Burst Write can be interrupted before completion by a new Write command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Write command continues to be input into the device until the Write Latency of the interrupting Write command is satisfied (WL=1) At this point, the data from the interrupting Write command is input into the device. Write commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Write with autoprecharge command with a Write command.

Write Interrupted by a Write Command Timing

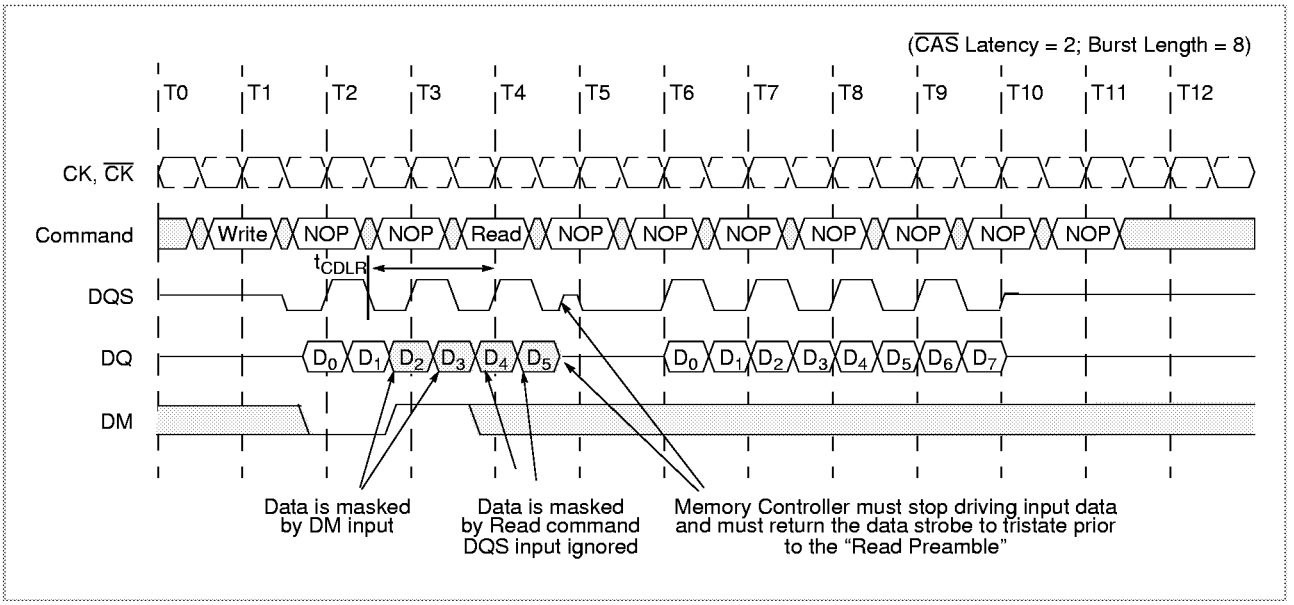


Write Interrupted by a Read

A Burst Write can be interrupted by a Read command to any bank. If a burst write operation is interrupted prior to the end of the burst operation, then the last two pieces of input data prior to the Read command must be masked off with the data mask (DM) input pin to prevent invalid data from being written into the memory array. Any data that is present on the DQ pins coincident with or following the Read command will be masked off by the Read command and will not be written to the array. The memory controller must give up control of both the DQ bus and the DQS bus at least one clock cycle before the read data appears on the outputs in order to avoid contention. In order to avoid data contention within the device, a delay is required (t_{CDLR}) from the last valid data input before a Read command can be issued to the device.

It is illegal to interrupt a Write with autoprecharge command with a Read command.

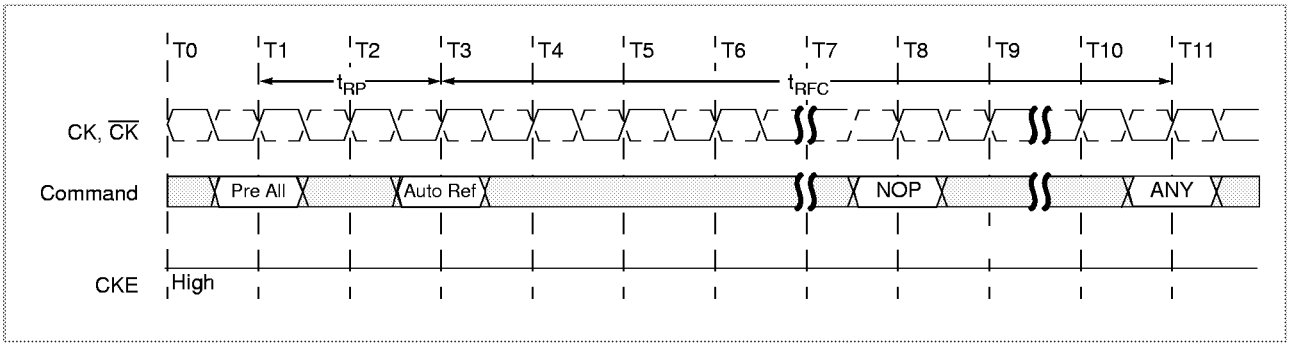
Write Interrupted by a Read Command Timing



Auto Refresh

The Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$, and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock. All banks must be precharged and idle for a t_{RP}(min) before the Auto Refresh command is applied. No control of the address pins is required once this cycle has started because of the internal address counter. When the Auto Refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate command or subsequent Auto Refresh command must be greater than or equal to the t_{RFC}(min). Commands may not be issued to the device once an AutoRefresh cycle has begun. $\overline{CS}$ input must remain high during the refresh period or NOP commands must be registered on each rising edge of the CK input until the refresh period is satisfied.

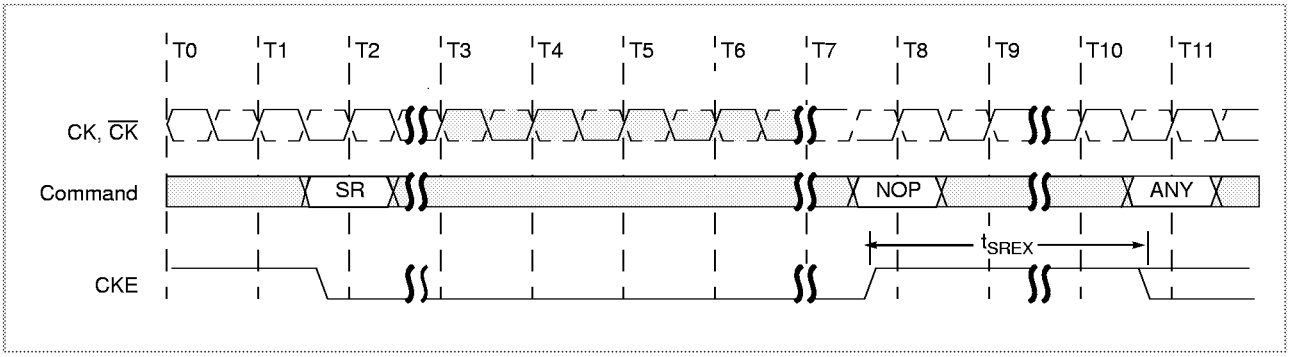
Auto Refresh Timing



Self Refresh

The Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the Self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. During the Self Refresh mode, all of the external control signals are disabled except CKE. The DLL is internally disabled during Self Refresh operation and the clock receiver is disabled to reduce power. To exit the Self Refresh mode, supply a stable clock input before returning CKE high. Issue a NOP command, and assert CKE high until t_{SREX} is met in order to lock DLL on to the system clock.

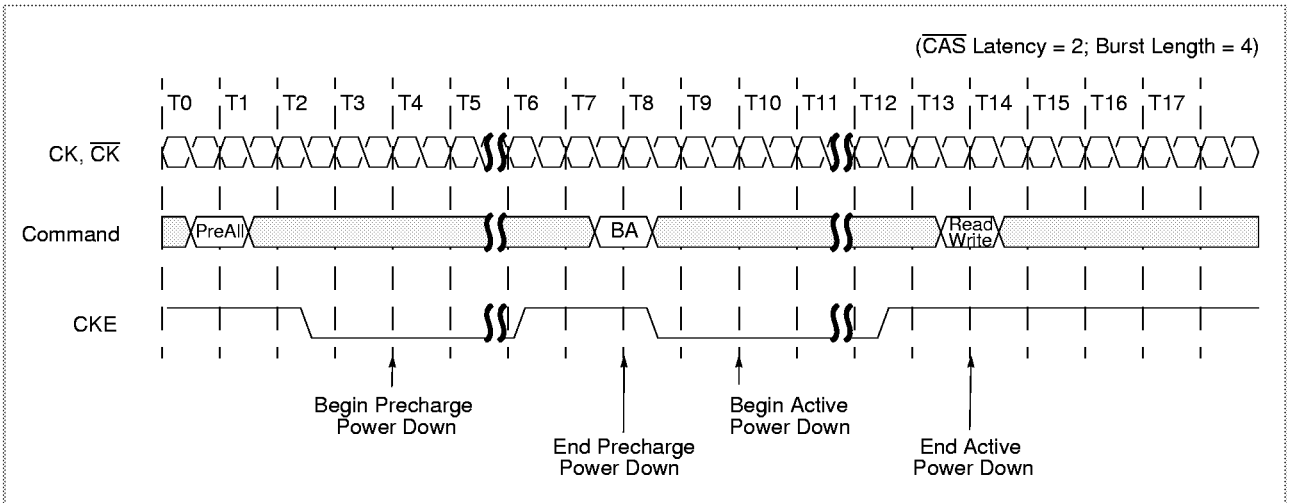
Self Refresh Timing



Power Down Mode

The Power Down mode is initiated by dropping CKE low and is exited by returning CKE high. Once Power Down mode has begun, all of the receiver circuits (except CK, $\overline{CK}$, CKE) and the DLL circuitry are gated off to reduce power consumption. Banks can be activated or precharged when Power Down Mode is entered, however, all banks must be in an idle state. Power Down mode can not be entered while burst read or write operations are being performed. Power Down mode will begin one clock cycle after CKE is registered low and, conversely, will end one clock cycle after CKE is registered high. The device cannot remain in Power Down mode longer than the refresh period (t_{REF}) of the device.

Power Down Mode Timing



Operative Command Table (Part 1 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	Address	Command	Action	Notes
Idle	H	X	X	X	X	X	INHBT	NOP	3
	L	H	H	X	X	X	NOP or BST	NOP	3
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	1
	L	L	H	H	X	BA, RA	ACT	Bank Activate	
	L	L	H	L	X	BA, PA	PRE/PREALL	NOP	
	L	L	L	H	X	X	REF/SR	AutoRefresh or Self Refresh	4
	L	L	L	L	X	Op-Code	MRS/EMRS	Mode Reg Set or Extended Mode Reg Set	
Row Active	H	X	X	X	X	X	INHBT	NOP	
	L	H	H	X	X	X	NOP or BST	NOP	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Begin Read: Determine AP	9
	L	H	L	L	V	BA, CA, AP	WR/WRA	Begin Write: Determine AP	9
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1, 5
	L	L	H	L	X	BA, PA	PRE/PREALL	Precharge	6
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input.

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down mode. All input buffers except CKE, CK, and $\overline{CK}$ will be disabled.
4. If both banks are idle, and CKE is deactivated (Low level) coincidentally with an AutoRefresh command, the device will enter Self Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask two preceding data bits with the DM pin.
9. Illegal if t_{RCD} is not satisfied.
10. Illegal if t_{WR} is not satisfied.
11. Illegal if t_{RC} is not satisfied.

RA = Row Address (A_0 - A_{11}) BA = Bank Address (BA_0-BA_1) PA = Precharge All (A_{10})
NOP = No Operation Command CA = Column Address (A_0 - A_9) AP = Auto Precharge (A_{10})

Operative Command Table (Part 2 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	Address	Command	Action	Notes
Read	H	X	X	X	X	X	INHBT	Continue Burst to End → Row Active	
	L	H	H	X	X	X	NOP	Continue Burst to End → Row Active	
	L	H	H	L	X	X	BST	Burst Stop → Row Active	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Term Burst, New Read: Determine AP	7
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	2, 7
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREALL	Term Burst, Precharge	
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	X	INHBT	Continue Burst to End → Row Active	
	L	H	H	X	X	X	NOP	Continue Burst to End → Row Active	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Term Burst, New Read: Determine AP	7, 8
	L	H	L	L	V	BA, CA, AP	WR/WRA	Term Burst, Start Write: Determine AP	2, 7
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREALL	Term Burst, Precharging	8
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input.

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down mode. All input buffers except CKE, CK, and $\overline{CK}$ will be disabled.
4. If both banks are idle, and CKE is deactivated (Low level) coincidentally with an AutoRefresh command, the device will enter Self Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask two preceding data bits with the DM pin.
9. Illegal if t_{RCD} is not satisfied.
10. Illegal if t_{WR} is not satisfied.
11. Illegal if t_{RC} is not satisfied.

RA = Row Address (A_0 - A_{11}) BA = Bank Address (BA_0-BA_1) PA = Precharge All (A_{10})
NOP = No Operation Command CA = Column Address (A_0 - A_9) AP = Auto Precharge (A_{10})

Operative Command Table (Part 3 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	Address	Command	Action	Notes
Read with Auto Precharge	H	X	X	X	X	X	INHBT	Continue Burst to End → Precharge	
	L	H	H	X	X	X	NOP	Continue Burst to End → Precharge	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREALL	ILLEGAL	1
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	INHBT	Continue Burst to End → Precharge	
	L	H	H	X	X	X	NOP	Continue Burst to End → Precharge	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREALL	ILLEGAL	1
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input.

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down mode. All input buffers except CKE, CK, and $\overline{CK}$ will be disabled.
4. If both banks are idle, and CKE is deactivated (Low level) coincidentally with an AutoRefresh command, the device will enter Self Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask two preceding data bits with the DM pin.
9. Illegal if t_{RCD} is not satisfied.
10. Illegal if t_{WR} is not satisfied.
11. Illegal if t_{RC} is not satisfied.

RA = Row Address (A_0 - A_{11}) BA = Bank Address (BA_0-BA_1) PA = Precharge All (A_{10})
NOP = No Operation Command CA = Column Address (A_0 - A_9) AP = Auto Precharge (A_{10})

Operative Command Table (Part 4 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	Address	Command	Action	Notes
Precharging	H	X	X	X	X	X	INHBT	NOP → Enter idle after t_{RP}	
	L	H	H	X	X	X	NOP	NOP → Enter idle after t_{RP}	
	L	H	H	L	X	X	BST	NOP → Enter idle after t_{RP}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	1
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREALL	NOP → Enter Idle after t_{RP}	1
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	
Bank Activating	H	X	X	X	X	X	INHBT	NOP → Enter Row Active after t_{RCD}	
	L	H	H	X	X	X	NOP	NOP → Enter Row Active after t_{RCD}	
	L	H	H	L	X	X	BST	NOP → Enter Row Active after t_{RCD}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1, 9
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	1, 9
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1, 5
	L	L	H	L	X	BA, PA	PRE/PREALL	ILLEGAL	1, 6
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input.

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down mode. All input buffers except CKE, CK, and $\overline{CK}$ will be disabled.
4. If both banks are idle, and CKE is deactivated (Low level) coincidentally with an AutoRefresh command, the device will enter Self Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask two preceding data bits with the DM pin.
9. Illegal if t_{RCD} is not satisfied.
10. Illegal if t_{WR} is not satisfied.
11. Illegal if t_{RC} is not satisfied.

RA = Row Address (A_0 - A_{11}) BA = Bank Address (BA_0-BA_1) PA = Precharge All (A_{10})
NOP = No Operation Command CA = Column Address (A_0 - A_9) AP = Auto Precharge (A_{10})

Operative Command Table (Part 5 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	Address	Command	Action	Notes
Write Recovering	H	X	X	X	X	X	INHBT	NOP → Enter Row Active after t_{WR}	
	L	H	H	X	X	X	NOP	NOP → Enter Row Active after t_{WR}	
	L	H	H	L	X	X	BST	NOP → Enter Row Active after t_{WR}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Start Read, Determine AP	2
	L	H	L	L	V	BA, CA, AP	WR/WRA	New Write, Determine AP	
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREALL	ILLEGAL	1,10
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	
Write Recovering with Auto Precharge	H	X	X	X	X	X	INHBT	NOP → Enter Precharge after t_{WR}	
	L	H	H	X	X	X	NOP	NOP → Enter Precharge after t_{WR}	
	L	H	H	L	X	X	BST	NOP → Enter Precharge after t_{WR}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1, 2
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	1
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREALL	ILLEGAL	1
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input.

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down mode. All input buffers except CKE, CK, and $\overline{CK}$ will be disabled.
4. If both banks are idle, and CKE is deactivated (Low level) coincidentally with an AutoRefresh command, the device will enter Self Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask two preceding data bits with the DM pin.
9. Illegal if t_{RCD} is not satisfied.
10. Illegal if t_{WR} is not satisfied.
11. Illegal if t_{RC} is not satisfied.

RA = Row Address (A_0 - A_{11}) BA = Bank Address (BA_0-BA_1) PA = Precharge All (A_{10})
NOP = No Operation Command CA = Column Address (A_0 - A_9) AP = Auto Precharge (A_{10})

Operative Command Table (Part 6 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	Address	Command	Action	Notes
Refreshing	H	X	X	X	X	X	INHBT	NOP → Enter idle after t_{RC}	
	L	H	H	X	X	X	NOP	NOP → Enter idle after t_{RC}	
	L	H	H	L	X	X	BST	NOP → Enter idle after t_{RC}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	11
	L	L	H	L	X	BA, PA	PRE/PREALL	ILLEGAL	
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	
Mode Register or Extended Mode Register Accessing	H	X	X	X	X	X	INHBT	NOP → Enter idle after two clocks	
	L	H	H	X	X	X	NOP	NOP → Enter idle after two clocks	
	L	H	H	L	X	X	BST	NOP → Enter idle after two clocks	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	X	BA, CA, AP	WR/WRA	ILLEGAL	
	L	L	H	H	X	BA, RA	ACT	ILLEGAL	
	L	L	H	L	X	BA, PA	PRE/PREALL	ILLEGAL	
	L	L	L	H	X	X	REF/SR	ILLEGAL	
	L	L	L	L	X	Op-Code	MRS/EMRS	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input.

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down mode. All input buffers except CKE, CK, and $\overline{CK}$ will be disabled.
4. If both banks are idle, and CKE is deactivated (Low level) coincidentally with an AutoRefresh command, the device will enter Self Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask two preceding data bits with the DM pin.
9. Illegal if t_{RCD} is not satisfied.
10. Illegal if t_{WR} is not satisfied.
11. Illegal if t_{RC} is not satisfied.

RA = Row Address (A_0 - A_{11}) BA = Bank Address (BA_0-BA_1) PA = Precharge All (A_{10})
NOP = No Operation Command CA = Column Address (A_0 - A_9) AP = Auto Precharge (A_{10})

Function Truth Table

All inputs are latched on the rising edge of the clock, except the DQs and DMs which are latched at rising and falling edges of DQS.

Operation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA_0, BA_1	A_{10}	A_0-A_9	MNE	Notes
	n-1	n										
Device Deselect	H	X	H	X	X	X	X	X	X	X	INHBT	
No Operation	H	X	L	H	H	H	X	X	X	X	NOP	
Load Mode Register Mode or Extended Mode Register	H	X	L	L	L	L	X	OP CODE			MRS/EMRS	1
Row Activate	H	X	L	L	H	H	X	BS	Row Address		ACT	2
Read	H	X	L	H	L	H	X	BS	L	Col.	RD	3
Read w/ Auto Precharge	H	X	L	H	L	H	X	BS	H	Col.	RDA	3
Write	H	X	L	H	L	L	V	BS	L	Col.	WR	3, 4
Write w/ Auto Precharge	H	X	L	H	L	L	V	BS	H	Col.	WRA	3, 4
Burst Stop	H	X	L	H	H	L	X	X	X	X	BST	5
Precharge Single Bank	H	X	L	L	H	L	X	BS	L	X	PRE	
Precharge All Banks	H	X	L	L	H	L	X	X	H	X	PREALL	
Auto Refresh	H	H	L	L	L	H	X	X	X	X	REF	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	SR(ENTRY)	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	SR(EXIT)	
	L	H	L	H	H	H	X	X	X	X		
Power Down Mode (entry)	H	L	H	X	X	X	X	X	X	X	PDN(ENTRY)	
	H	L	L	H	H	H	X	X	X	X		
Power Down Mode (exit)	L	H	X	X	X	X	X	X	X	X	PDN(EXIT)	

1. Should be issued only after both banks are deactivated (PREALL command).
2. Should be issued only after the corresponding bank has been deactivated (PRE command).
3. Should be issued after the corresponding bank has been activated (ACT command).
4. Any valid Write cycles applied to the selected bank/row will be masked according to the DM.
5. Should be issued only during Read burst cycles.

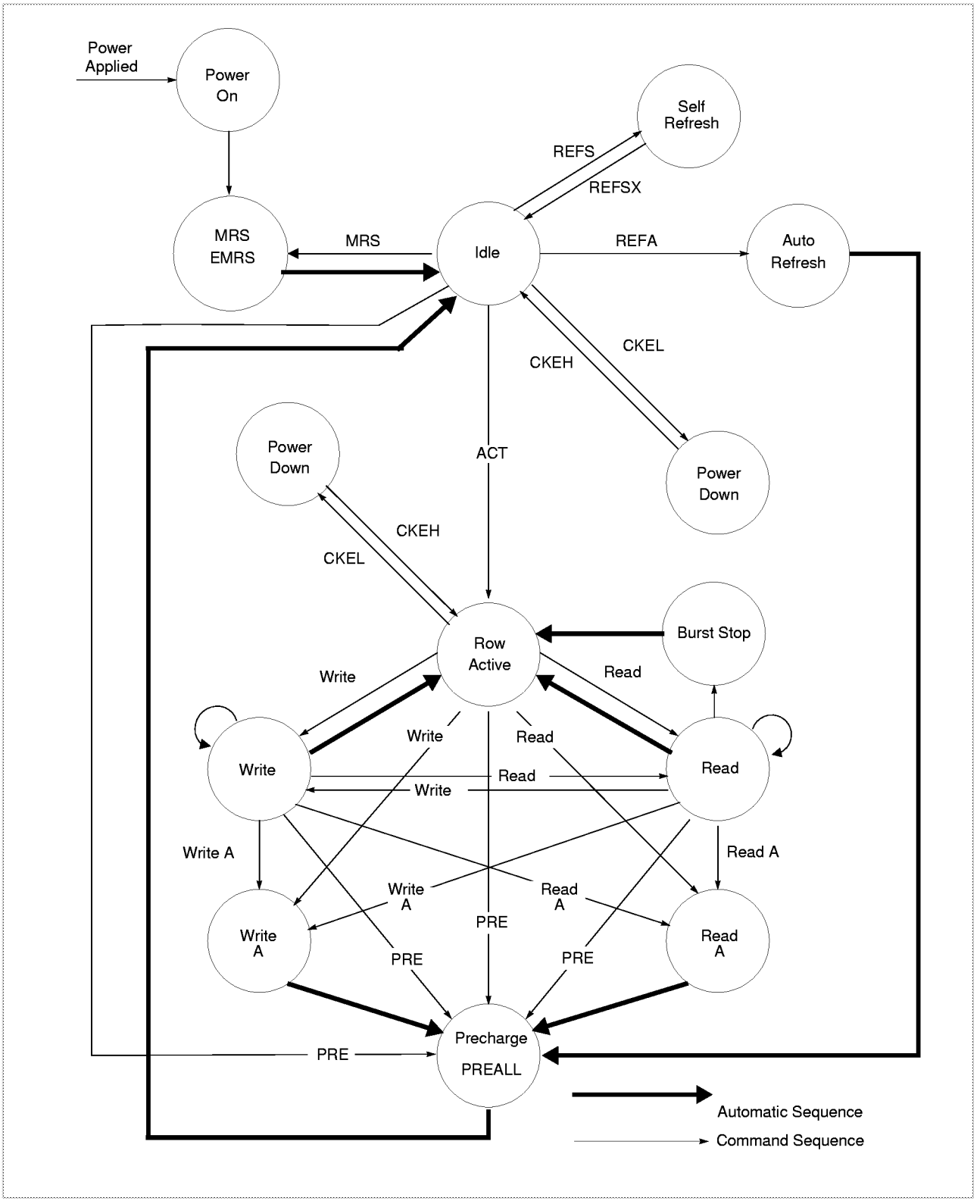
Function Truth Table for CKE

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self Refreshing	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self Refresh (idle after t_{SREX})	1
	L	H	L	H	H	H	X	Exit Self Refresh (idle after t_{SREX})	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	L	X	X	ILLEGAL	1
	L	H	L	L	X	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (maintain Self Refresh)	1
Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit power down (idle after t_{PDEX})	1
	L	L	X	X	X	X	X	NOP (maintain power down)	
All Banks Idle	H	H	X	X	X	X	X	Refer to the Function Truth Table on page 40.	2
	H	L	L	L	L	H	X	Enter Self Refresh	3
	H	L	H	X	X	X	X	Enter Power Down	2
	H	L	L	H	H	H	X	Enter Power Down	2
	H	L	L	H	H	L	X	ILLEGAL	2
	H	L	L	H	L	X	X	ILLEGAL	2
	H	L	L	L	X	X	X	ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Power Down in this table	
Any state other than listed above	H	H	X	X	X	X	X	Refer to the Function Truth Table on page 40.	

ABBREVIATIONS: H=High Level; L=Low Level; X=Don't Care.

1. CKE low-to-high transition re-enables inputs asynchronously. A minimum setup time to CK must be satisfied before any commands other than EXIT are executed.
2. Power Down can be entered when all banks are idle (banks can be active or precharged).
3. Self Refresh can be entered only from the Precharge/Idle state.

Simplified State Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-1.0 to 4.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	-1.0 to 4.6	V
V_{DDQ}	Voltage on V_{DD} supply relative to V_{SS}	-1.0 to 3.7	V
T_{STG}	Storage Temperature	-55 to +150	°C
P_D	Power Dissipation	1.5	W
I_{OUT}	Short Circuit Current	50	mA

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Supply Voltage Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Device Supply Voltage	3.0	3.3	3.6	V	
V_{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V	1
V_{REF}	Input Reference Voltage	1.15	1.25	1.35	V	2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.
3. V_{TT} of the transmitting device must track V_{REF} of the receiving device.

Stub Series Terminated Logic (SSTL_2)

DC Input Levels

SSTL_2 DC input levels reduce the effects of ringing and define the final logic state unambiguously. Once a receiver input has crossed a DC level, it will change to and maintain the new state.

DC Operating Conditions (SSTL_2 Inputs) (V_{DDQ}=2.5V, Tamb=70C, Voltage Referenced to V_{SS})

Symbol	Parameter	Min	Max	Units	Notes
V_{IH} (DC)	DC Input Logic High	V_{REF}+0.18	V_{DDQ}+0.3	V	1
V_{IL} (DC)	DC Input Logic Low	-0.30	V_{REF}-0.18	V	
I_{IL}	Input Leakage Current	-5	5	uA	2
I_{OL}	Output Leakage Current	-5	5	uA	3

1. The relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of V_{IH} (max) (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0V (High corner V_{DDQ}+300mV).
2. For any pin under test input of 0V ≤ Vin ≤ V_{DDQ} + 0.3V.
3. Any valid Write cycles applied to the selected bank/row will be masked according to the DM.

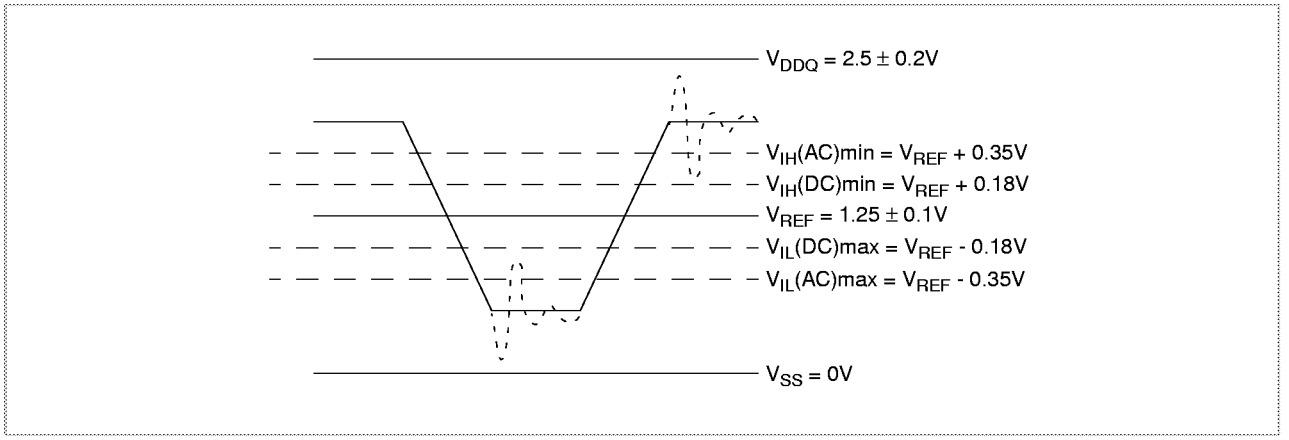
AC Input Levels

SSTL_2 AC input levels must be met for the receiver to meet the timing specifications.

SSTL_2 Input AC Logic Levels

Symbol	Parameter	Min	Max	Units	Notes
V_{IH} (AC)	AC Input Logic High	V_{REF}+0.35	—	V	
V_{IL} (AC)	AC Input Logic Low	—	V_{REF}-0.35	V	

SSTL_2 Input Levels (V_{DDQ}=2.5V)



SSTL_2 Output Buffer Characteristics

Symbol	Parameter	Class II	Units	Notes
V_{REF}	Reference Voltage	$0.5 \bullet V_{DDQ}$	V	1
V_{TT}	Termination Voltage	V_{REF} +/- 0.04	V	
V_{OH}	Output Logic High Voltage	V_{TT} + 0.76	V	
V_{OL}	Output Logic Low Voltage	V_{TT} – 0.76	V	
I_{OH}	Output Minimum Source DC Current	-15.2	mA	
I_{OL}	Output Minimum Sink DC Current	15.2	mA	
RT	Termination Resistor	25	Ω	
RS	Series Resistor	25	Ω	

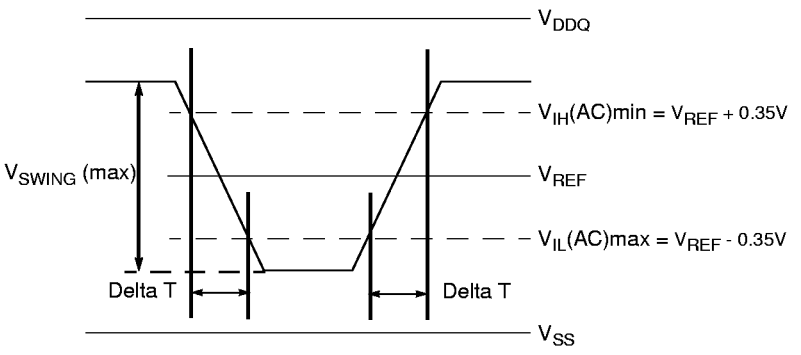
1. The V_{DDQ} of the device under test is referenced.

SSTL_2 AC Test Conditions

Symbol	Parameter	Value	Units	Notes
V_{REF}	Input Timing Measurement Reference Voltage for SSTL Inputs	$0.5 \bullet V_{DDQ}$	V	1
V_{SWING}(max)	Input Signal Maximum Swing (Peak to Peak)	1.5	V	1, 2
V_{IH}/V_{IL}	SSTL Input Levels (CK, $\overline{CK}$, DQ, DQS, DM)	V_{REF} +/- 0.35		
SLEW(min)	Input Signal Minimum Slew Rate	1.0	V/ns	3
Output Load Condition	See Output Load for AC Timing Parameters			
V_{TT}	Output Timing Measurement Reference Level	V_{REF} +/- 0.04	V	

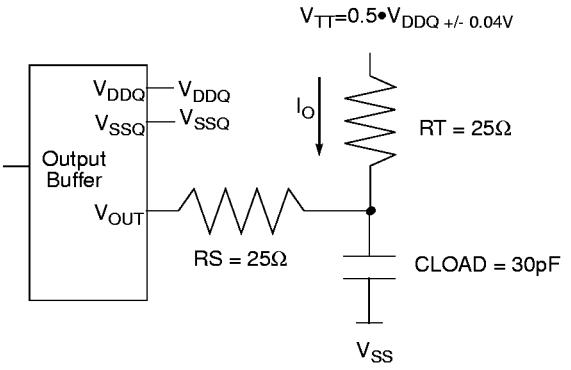
1. Input waveform timing is referenced to the input signal crossing the V_{REF} level applied to the device.
2. Compliant devices must still meet the V_{IH} (AC) and V_{IL} (AC) specifications under actual use conditions.
3. The 1V/ns input signal minimum slew rate is to be maintained in the V_{IL} max (AC) to V_{IL} min (AC) range of the input signal swing.

SSTL_2 AC Input Test Signal Waveform



Slew Rate = {V_{IH}(AC)min - V_{IL}(AC)max} / Delta T

Output Load for AC Timing Parameters not Involving Entry or Exit for Hi-Z or Hold Times



Capacitance (V_{DD}=3.3V ± 0.3V, T_A = 0 to +70°C)

Parameter	Symbol	Min.	Max.	Units
Input Capacitance (A_0-A11, BA_0-BA_1)	C_{IN1}	2.5	4	pF
Input Capacitance (CK, $\overline{CK}$, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	2.5	4	pF
Input Capacitance (DM)	C_{IN3}	4	6.5	pF
Data Strobe & DQs Input/Output Capacitance	C_{OUT}	4	6.5	pF

Operating, Standby and Refresh Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	Speed		Units	Notes
			-10	-12		
Operating Current t_{RC} = t_{RC}(min), t_{CK} = min Active-Precharge command without burst operation	I_{CC1}	1 bank operation $\overline{CAS}$ Latency = 2	90	70	mA	1, 2, 3
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{CS}$ =V_{IH}(min)	20	20	mA	1
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH}(min)	45	40	mA	1, 3
No Operating Current (Active state: 4 bank)	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = min	30	30	mA	1
	I_{CC3N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH}(min)	60	55	mA	1, 3
Operating Current (Burst Mode)	I_{CC4}	t_{CK} = min, Read/ Write command cycling, Multiple banks active, gapless data, BL=4	100	80	mA	1, 2, 3
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min, t_{RC} = t_{RFC}(min) CBR command cycling	135	110	mA	1, 4, 5
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	1	1	mA	1, 4

1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}.
2. The specified values are obtained with the output open.
3. Input signals are changed once during three clock cycles.
4. Refresh period is 64ms.
5. Minimum cycle time during Autorefresh operation (t_{REF}) is greater than minimum cycle time for Read/Write operation.

AC Characteristics (Part 1 of 2) (T_A=0 to +70°C, V_{CC}=3.3 0.3V)

Symbol	Parameter		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.		
t_{CK}	Clock Period	CL=2	10	20	12	24	ns	1
		CL=2.5	7.5	20	10	24	ns	
		CL=3	7	20	8	24	ns	
t_{RC}	Row Cycle Time	R/W Operation	90		90		ns	
t_{RFC}		Auto Refresh	90		90		ns	2
t_{RAS}	Row Active Time		50	100K	60	100K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay		20		24			
t_{RP}	Row Precharge Time		20		24		ns	
t_{RRD}	Row Activate to Row Activate Delay		1		1		CK	
t_{WR}	Last Data in to Row Precharge		10	14	10	16	ns	
t_{CDLR}	Last Data in to Read Command Delay		1.25	1.75	1.25	1.75	CK	
t_{CCD}	Col. Address to Col. Address Delay		1		1		CK	
t_{CH}	CK High Level Width		0.45•t_{CK}		0.45•t_{CK}		ns	
t_{CL}	CK Low Level Width		0.45•t_{CK}		0.45•t_{CK}		ns	
t_{AC}	Output Data Edge to Clock Edge		-0.1•t_{CK}	0.1•t_{CK}	-0.1•t_{CK}	0.1•t_{CK}	ns	
t_{DQSCK}	Data Strobe Edge to Clock Edge		-0.1•t_{CK}	0.1•t_{CK}	-0.1•t_{CK}	0.1•t_{CK}	ns	
t_{DQSQ}	Data Strobe Edge to Output Data Edge		-0.075•t_{CK}	0.075•t_{CK}	-0.075•t_{CK}	0.075•t_{CK}	ns	
t_{DV}	Output Data Valid Window		0.3•t_{CK}		0.3•t_{CK}		ns	
t_{DQSV}	Data Strobe Valid Window		0.3•t_{CK}		0.3•t_{CK}		ns	
t_{RPRE}	DQS Entry to Low-Z to First Rising Edge Delay (DQS Read Preamble)		0.9•t_{CK}	1.1•t_{CK}	0.9•t_{CK}	1.1•t_{CK}	ns	
t_{RPST}	DQS Last Falling Edge to Entry to Hi-Z Delay (DQS Read Postamble)		0.4•t_{CK}	0.6•t_{CK}	0.4•t_{CK}	0.6•t_{CK}	ns	
t_{QDQSS}	Data Input to Data Strobe Setup Time		0.075•t_{CK}		0.075•t_{CK}		ns	
t_{QDQSH}	Data Input to Data Strobe Hold Time		0.075•t_{CK}		0.075•t_{CK}		ns	
t_{DMDSQS}	Data Mask to Data Strobe Setup Time		0.075•t_{CK}		0.075•t_{CK}		ns	
t_{DMDQSH}	Data Mask to Data Strobe Hold Time		0.075•t_{CK}		0.075•t_{CK}		ns	
t_{WPRES}	Clock to DQS Write Preamble Setup Time		0	0.5•t_{CK}	0	0.5•t_{CK}	ns	
t_{WPREH}	Clock to DQS Write Preamble Hold Time		0.25•t_{CK}	1.25•t_{CK}	0.25•t_{CK}	1.25•t_{CK}	ns	
t_{WPST}	DQS Last Falling Edge to Entry to Hi-Z Delay (DQS Read Postamble)		0.4•t_{CK}	0.6•t_{CK}	0.4•t_{CK}	0.6•t_{CK}	ns	
t_{DQSS}	Clock to First Rising Edge of DQS Delay		0.75•t_{CK}	1.25•t_{CK}	0.75•t_{CK}	1.25•t_{CK}	ns	
t_{IS}	Input Setup Time (LVTTL inputs)		0.15•t_{CK}		0.15•t_{CK}		ns	
t_{IH}	Input Hold Time (LVTTL inputs)		0.15•t_{CK}		0.15•t_{CK}		ns	
t_{MRSD}	Mode Register / Extended Mode Register Set Cycle Time		2		2		CK	
t_{PDENT}	Power Down Entry Time		t_{IS} + 1 CK	2 CK + t_{IS}	t_{IS} + 1 CK	2 CK + t_{IS}	ns	

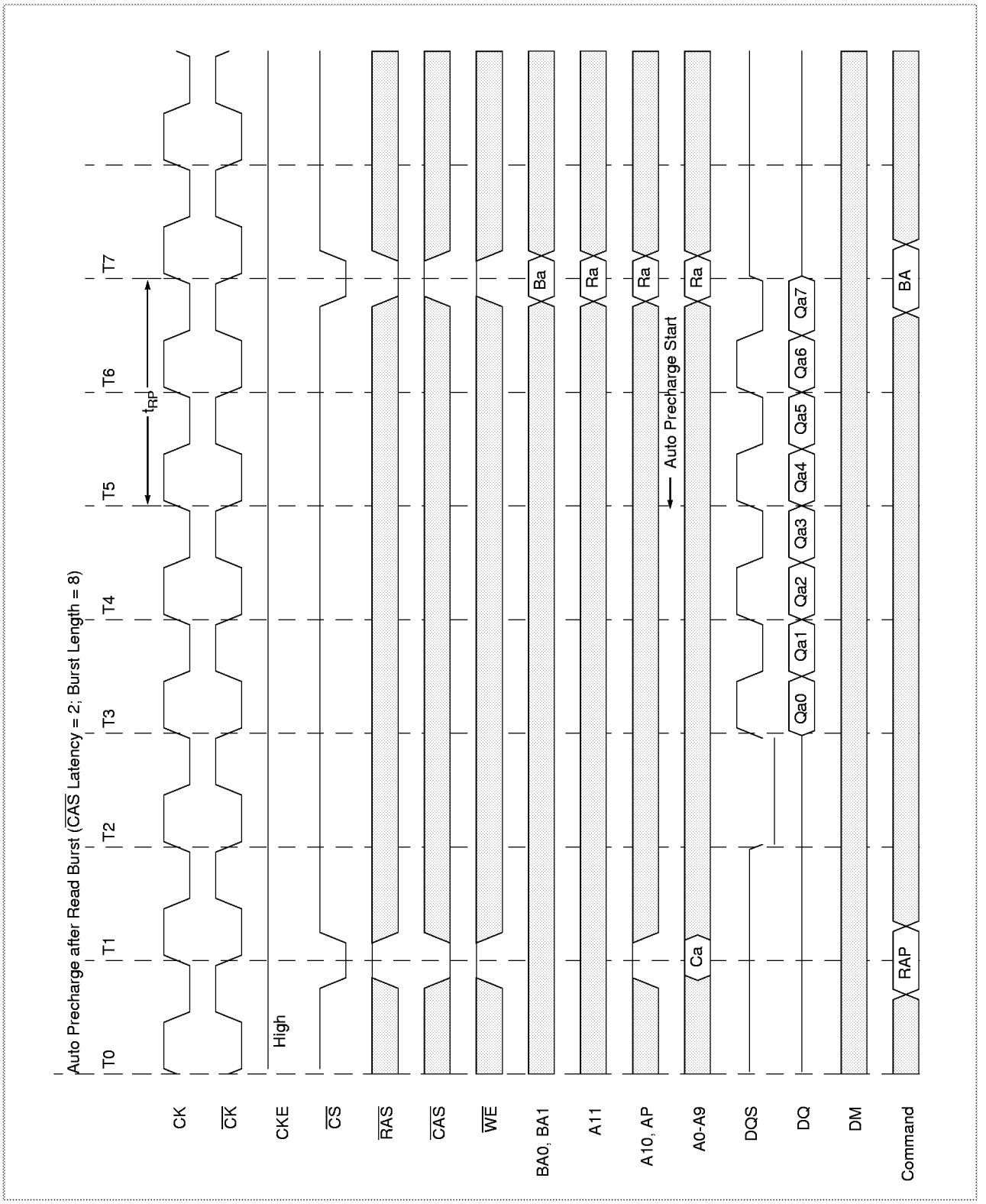
1. Maximum clock cycle may exceed the specification, however, the DLL is not guaranteed to operate when the maximum clock cycle is exceeded. It is recommended to turn off the DLL via the Extended Mode Register if t_{CK}(max) is exceeded. DQS and output data (DQ) will continue to track together, however, DQS and DQ will no longer track with CK.
2. Minimum AutoRefresh cycle time is greater than minimum cycle time during normal read or write operation.

AC Characteristics (Part 2 of 2) (T_A=0 to +70°C, V_{CC}=3.3 0.3V)

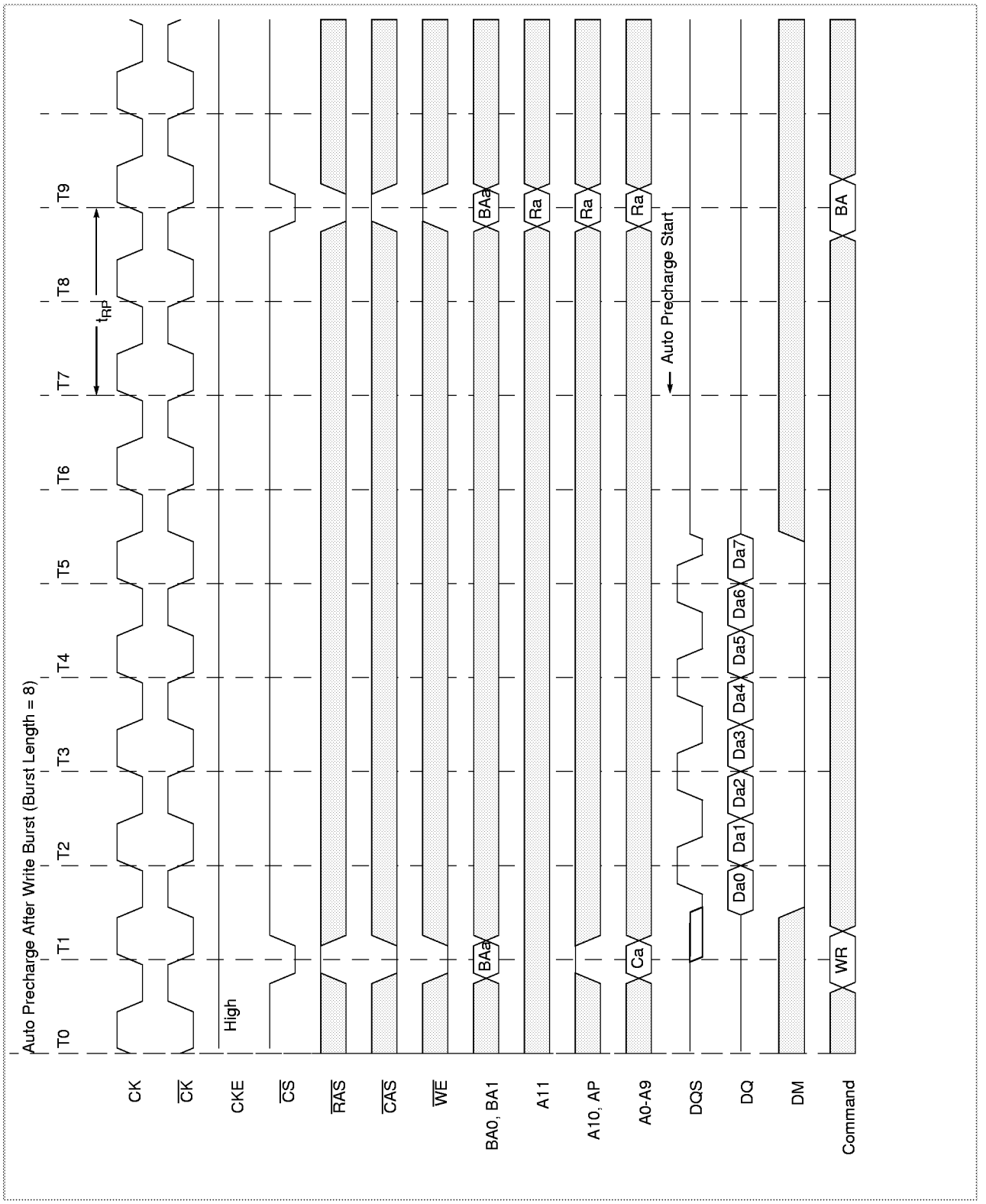
Symbol	Parameter	-10		-12		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{PDEX}	Power Down Exit TimeCK	t_{IS} + 1 CK	2 CK + t_{IS}	t_{IS} + 1 CK	2 CK + t_{IS}	ns	
t_{SREX}	Self Refresh Exit Time	200		200		Cycles	
t_T	CK Transition Time	0.5		0.5		ns	

1. Maximum clock cycle may exceed the specification, however, the DLL is not guaranteed to operate when the maximum clock cycle is exceeded. It is recommended to turn off the DLL via the Extended Mode Register if t_{CK}(max) is exceeded. DQS and output data (DQ) will continue to track together, however, DQS and DQ will no longer track with CK.
2. Minimum AutoRefresh cycle time is greater than minimum cycle time during normal read or write operation.

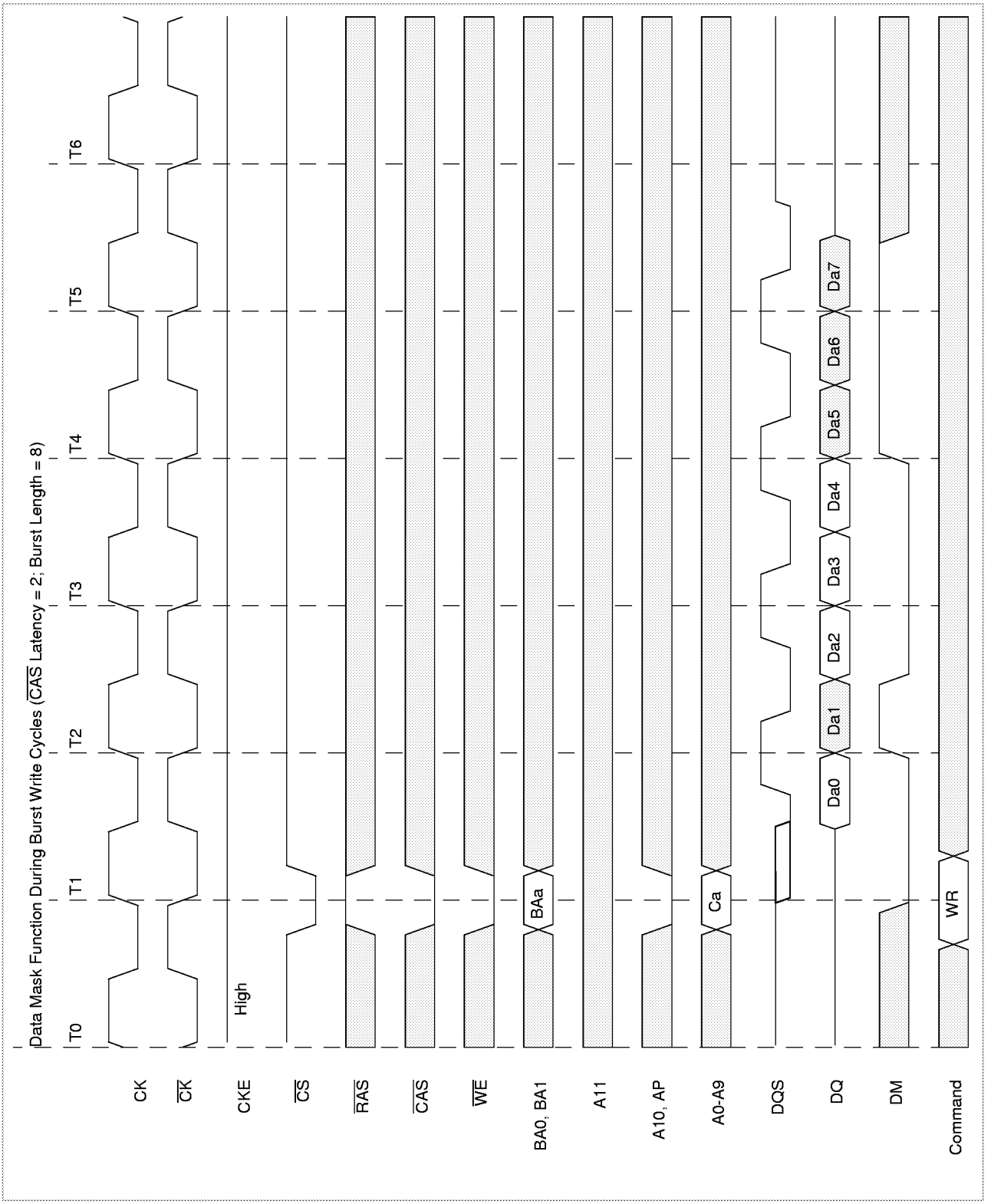
Auto Precharge After Read Burst



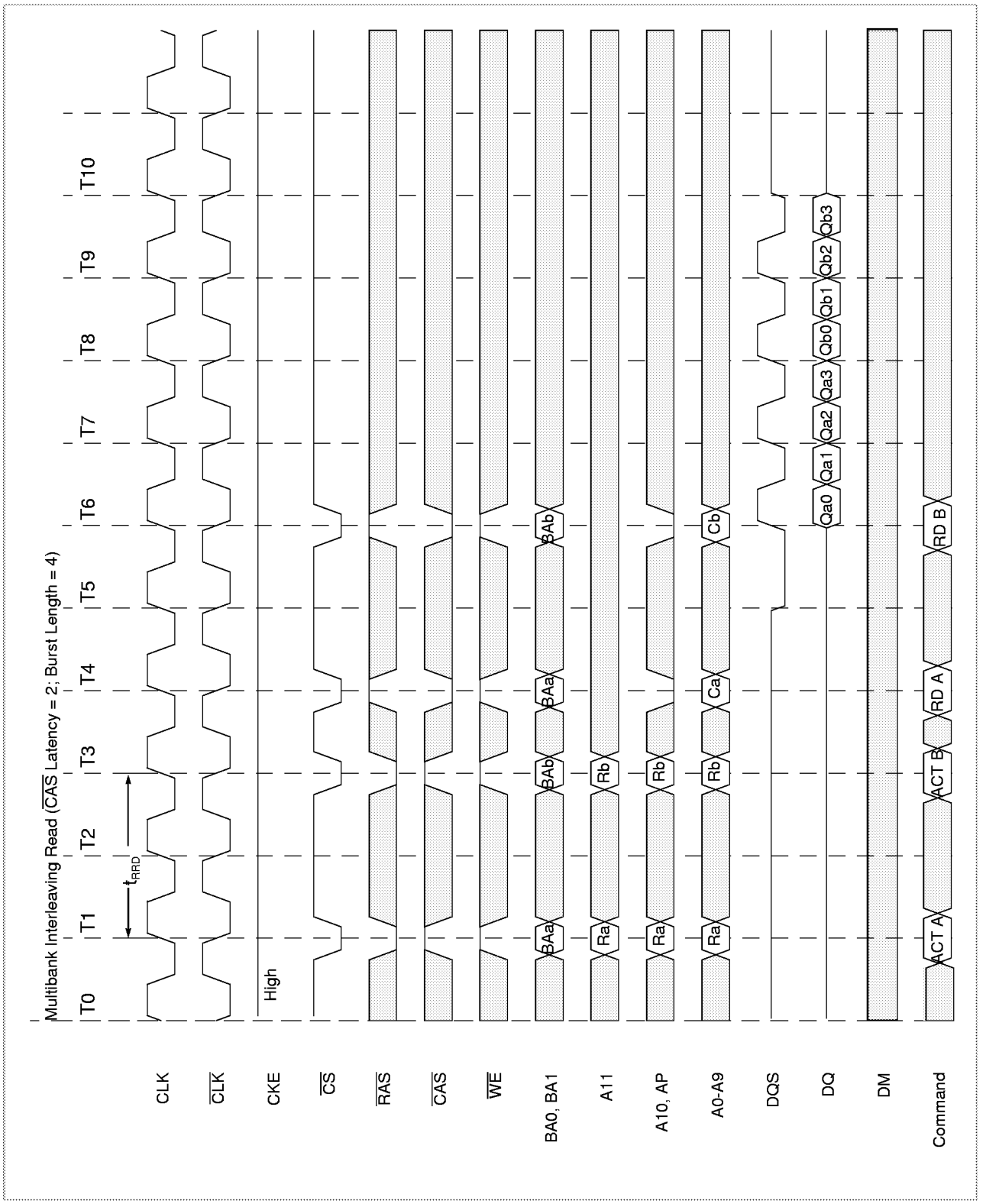
Auto Precharge After Write Burst



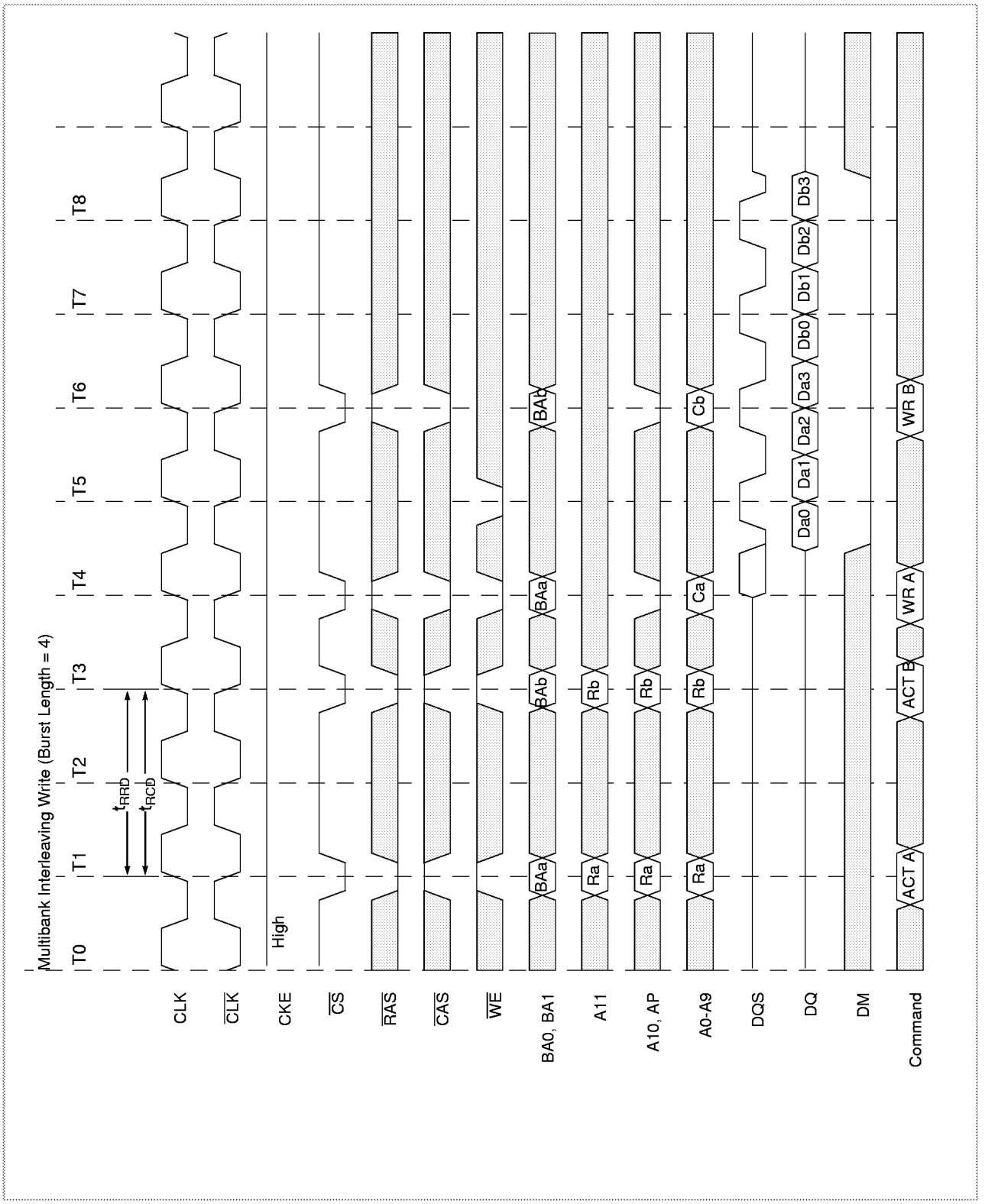
Data Mask Function Only for Write



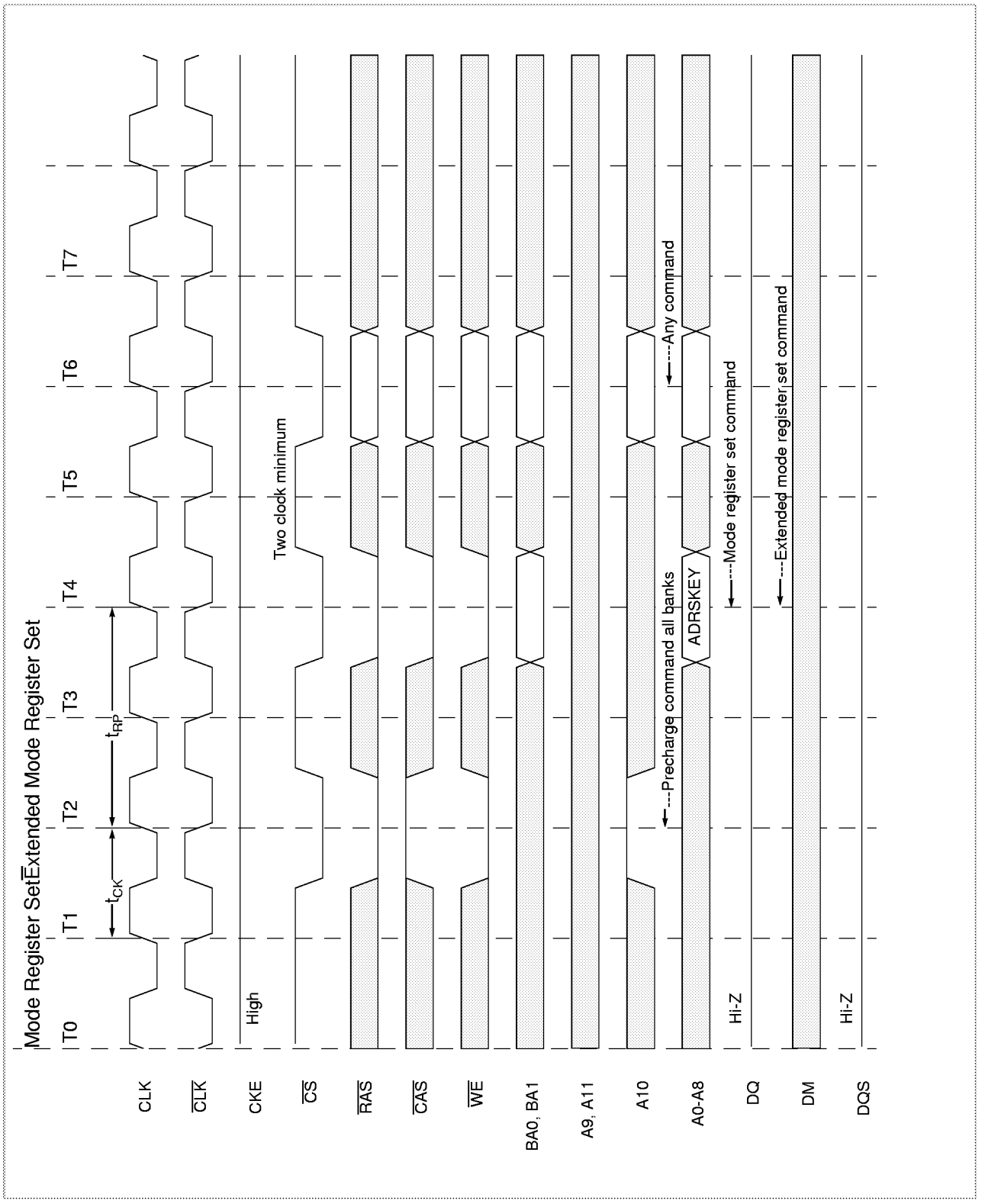
Multibank Interleaving Read



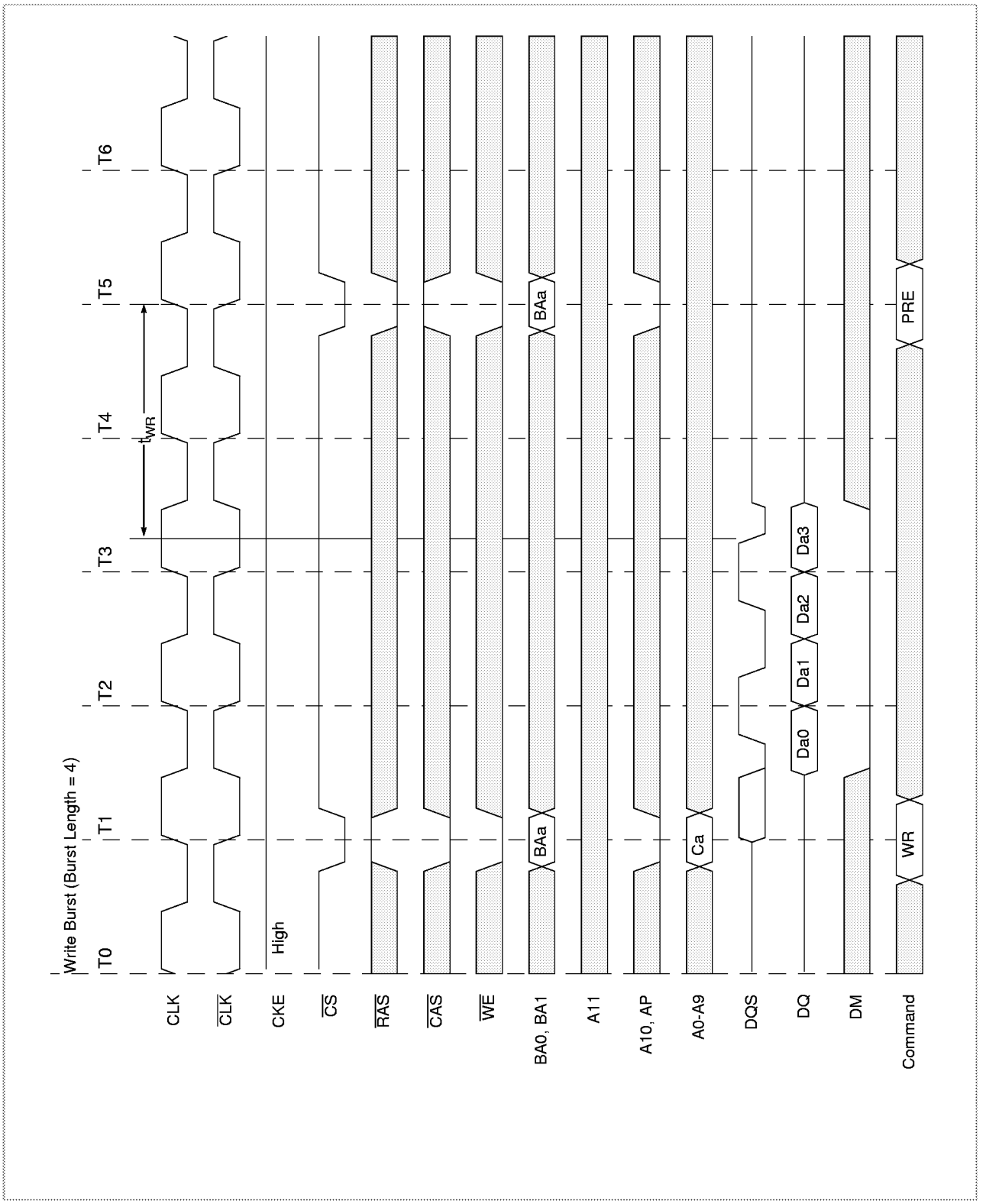
Multibank Interleaving Write



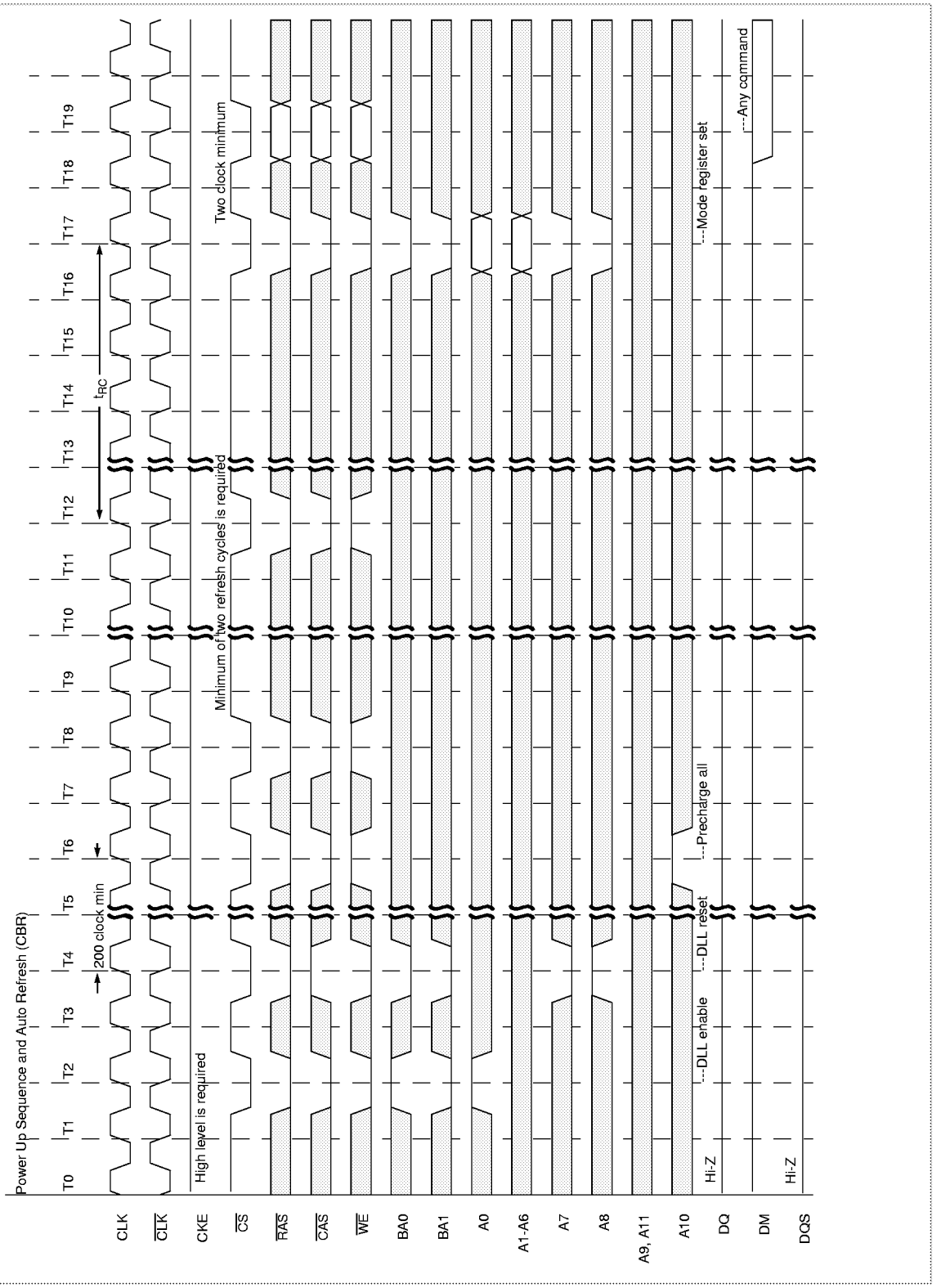
Mode Register / Extended Mode Register Set



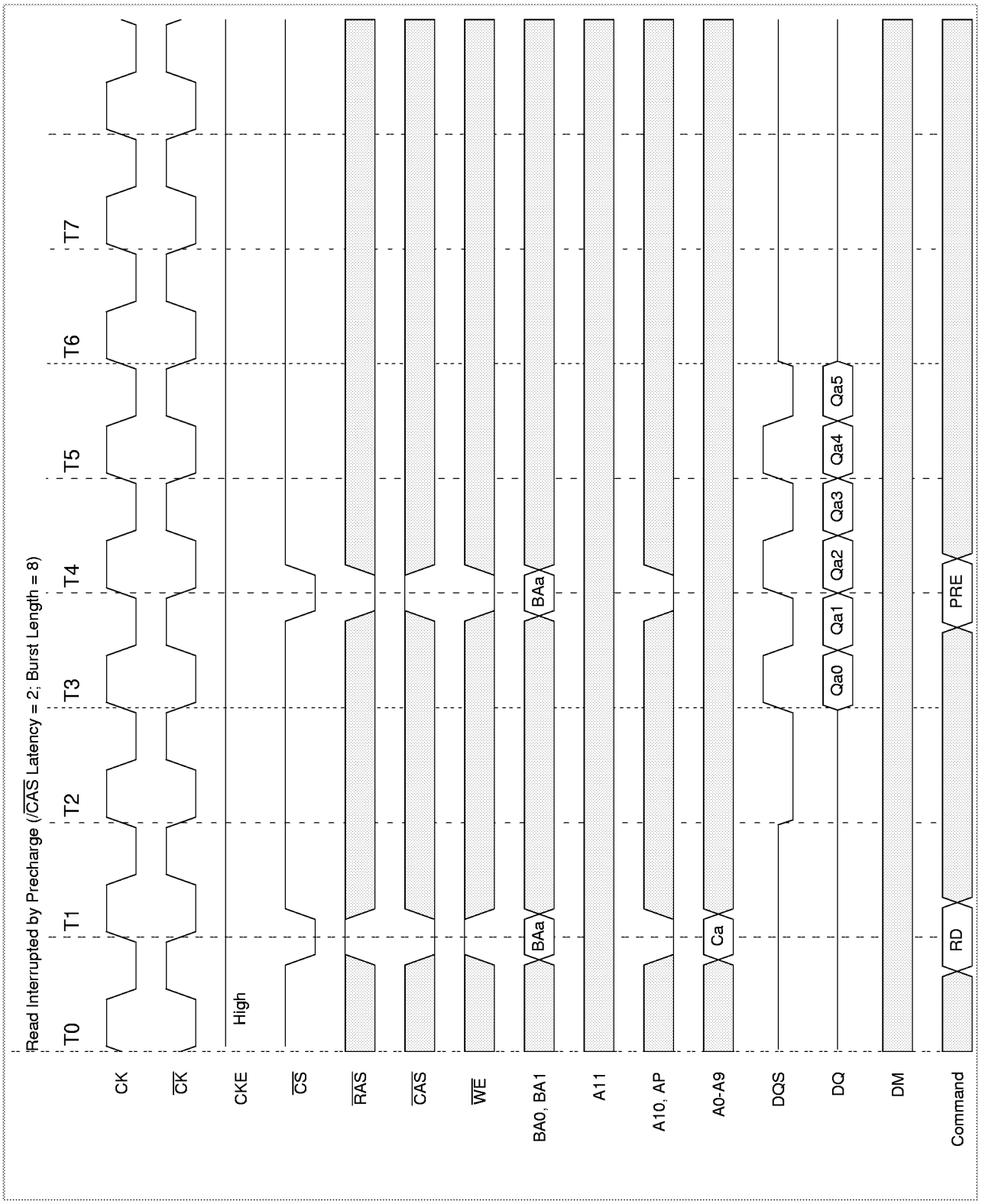
Write Burst



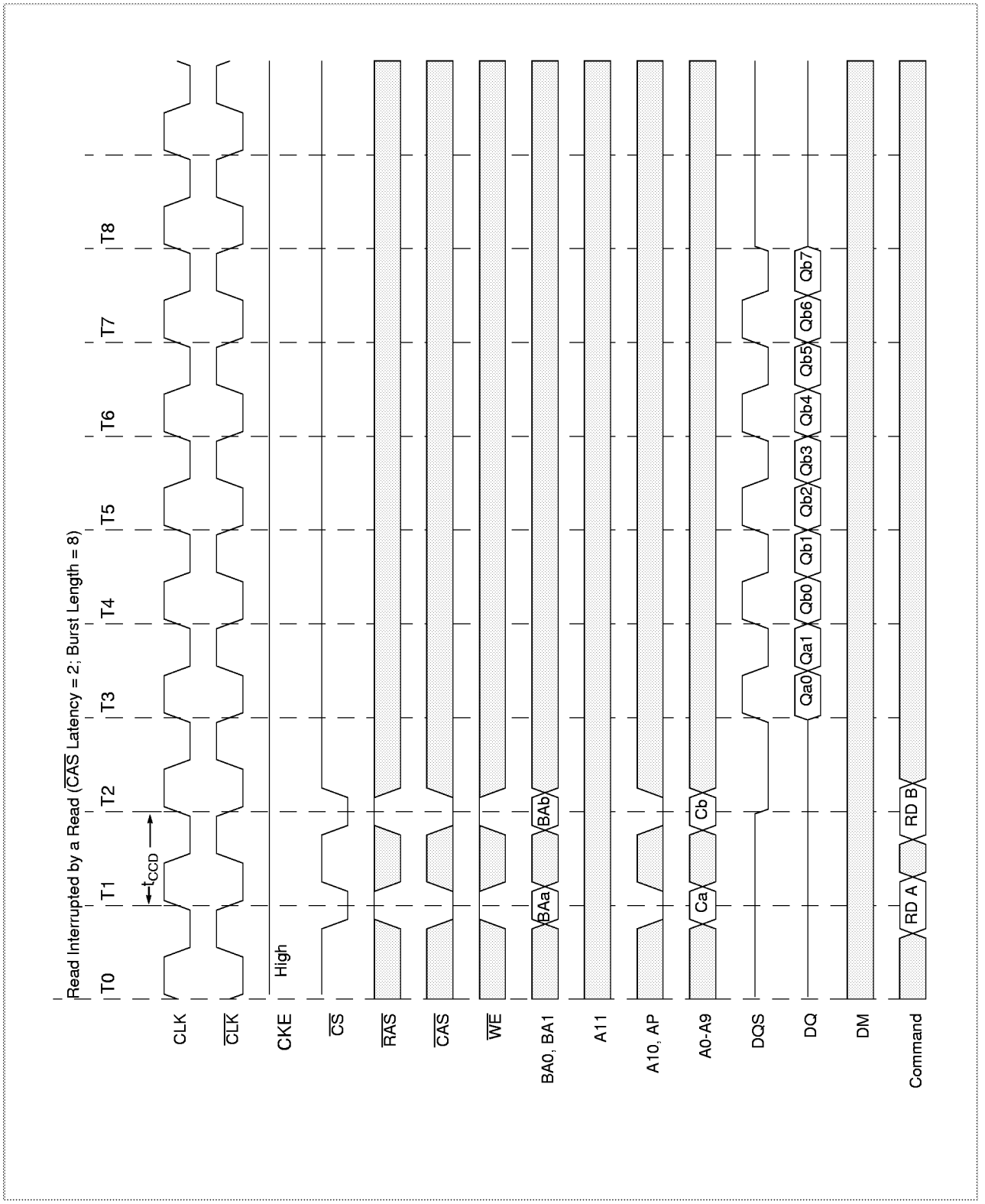
Power Up Sequence and Auto Refresh (CBR)



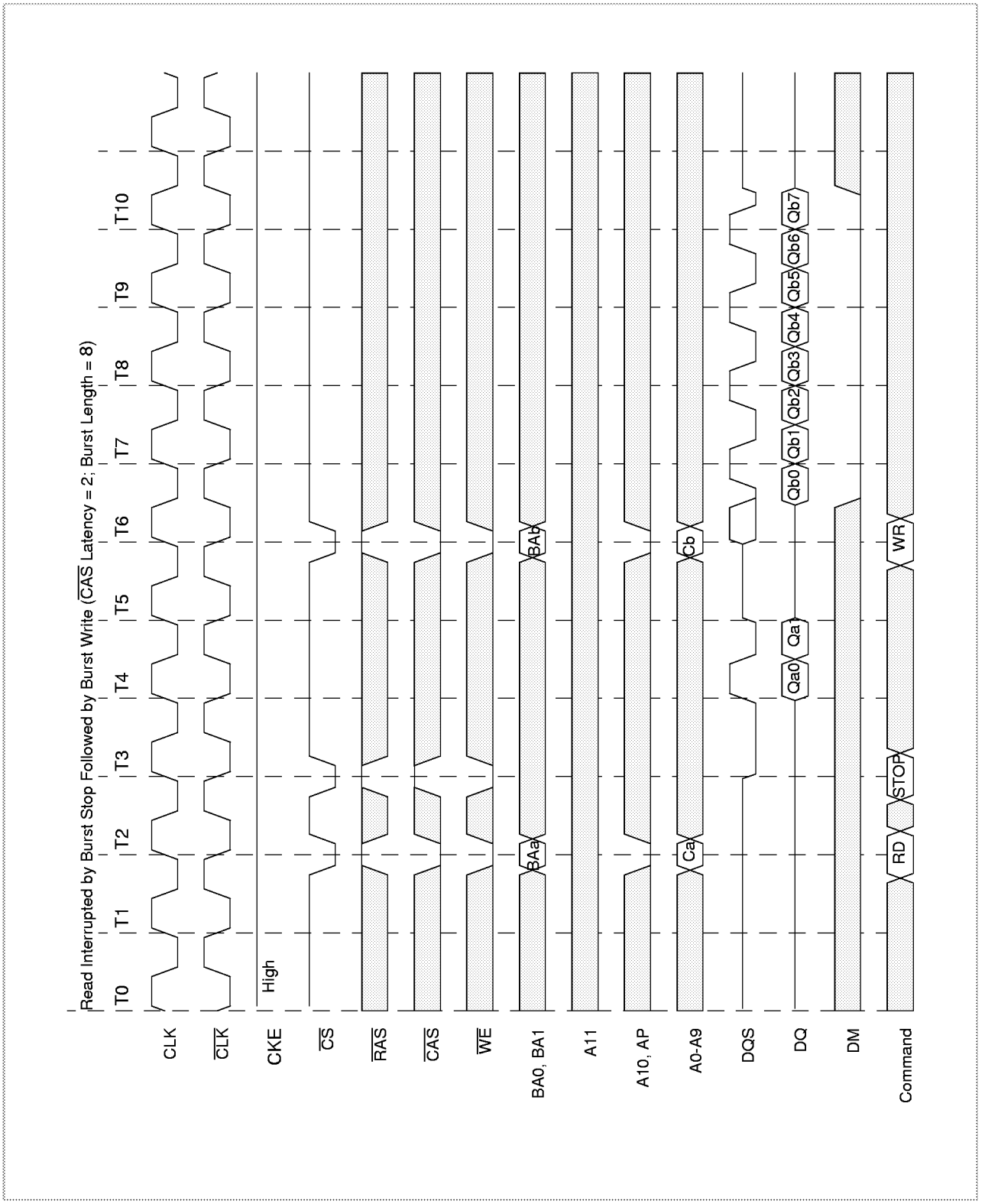
Read Interrupted by a Precharge



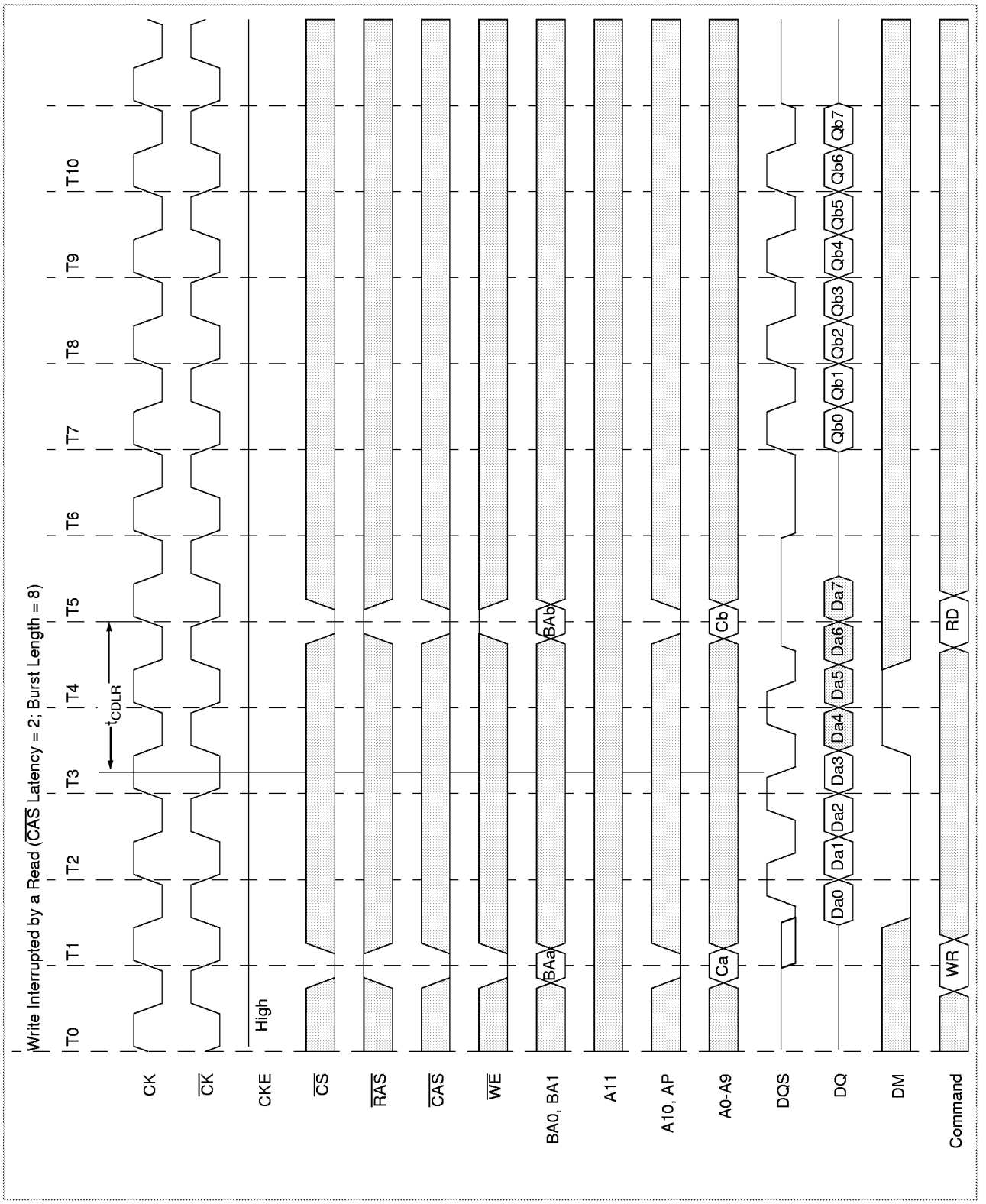
Read Interrupted by a Read



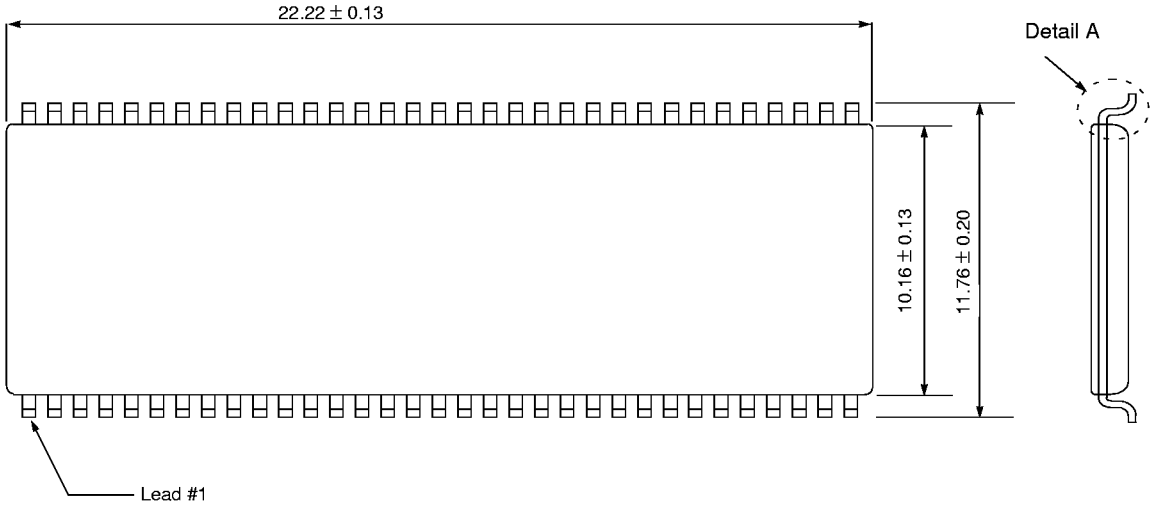
Read Interrupted by a Write and Burst Stop

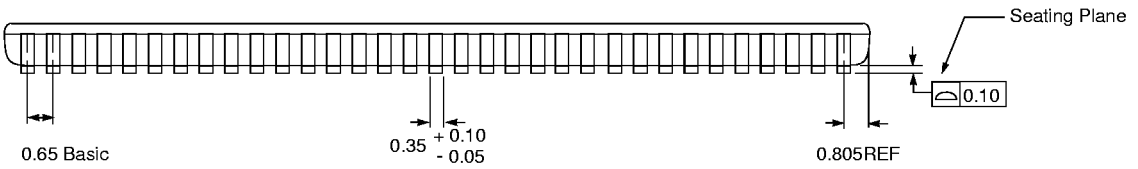


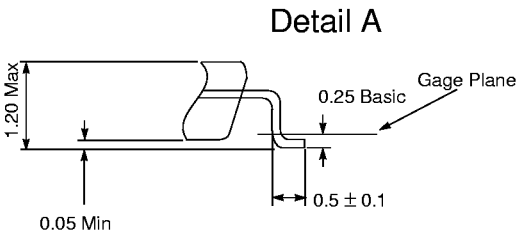
Write Interrupted by a Read



Package Dimensions (400mil; 66 lead; Thin Small Outline Package)







Revision Log

Revision	Contents of Modification
8/98	Initial release

For more information contact your IBM Microelectronics sales representative or
visit us on World Wide Web at http://www.chips.ibm.com

IBM Microelectronics manufacturing is ISO 9000 compliant.