L64550
MIL-STD-1750A
MBU Peripheral Device
Preliminary

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Unit
005790

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LSL

Description

LSI Logic Corporation's L64550 is a monolithic 1.5-micron drawn HCMOS chip designed to support the L64500 CPU (MIL-STD-1750A ISA). The L64550 contains a number of MIL-STD-1750A support options including; the Memory Management Unit (MMU) with mapping RAM, Block Protect Unit (BPU) with protection RAM, Memory Fault Status Register (MFSR), Watch-Dog timer and start-up ROM interface. In addition, the L64550 contains other options such as; a Bus Arbitrator with up to 6 bus masters, extended addressing capability to 8 M words, discrete I/O port, sophisticated CPU/MBU handshake to increase performance and bus time-out timer.

The MMU allows addressing of up to 1 M word of memory. In applications not requiring adherence to the standard, addressing can be extended to 8 M words. The MMU performs the logical-to-physical address translation and protection of logical space.

The BPU provides write protection in 1 K page granularity for up to 1 M word of physical memory for both L64500 CPU and DMA access.

If it is desired, the MMU and the BPU can be individually disabled.

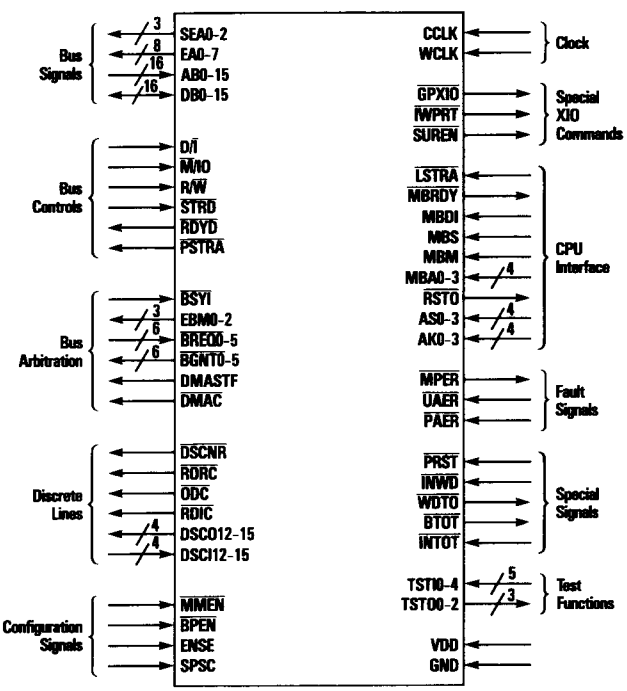
The L64550 MBU and L64500 CPU are included in LDS®, LSI Logic's Design System, as ASIC library elements. These elements can be used as Gigacells™ when combined with gate arrays or standard cells, or they can be used in multi-chip system simulations when adding new ASIC chips to the system.

The L64550 is available in several speed grades from 15 MHz to 25 MHz over the full military temperature range of −55°C to 125°C.

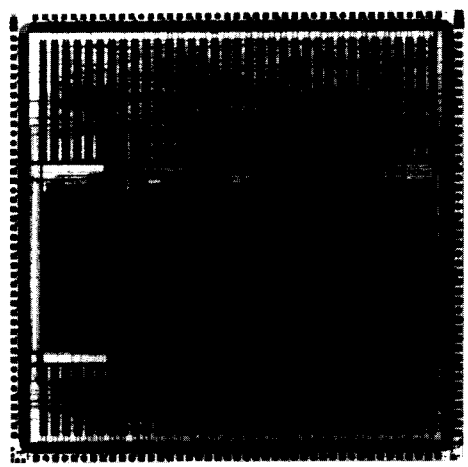
Features

- 1.5-micron drawn HCMOS technology
- 25 MHz operation over full military range
- Power dissipation < 1W
- Memory Management Unit (MMU) with 512×16 cache RAM
- Block Protect Unit (BPU) with 128×16 cache RAM
- Hit/miss mechanism
- Discrete I/O ports
- Extended addressing to 8 M words
- Bus Arbitration Unit with up to 6 bus masters
- Memory Fault Status Register (MFSR)
- Start-up ROM interface
- Bus interface time-out timer
- Watch-Dog timer
- TTL compatible interface
- Flexible packaging capability
- Available as ASIC Gigacell library element

Logic Symbol and Chip Layout

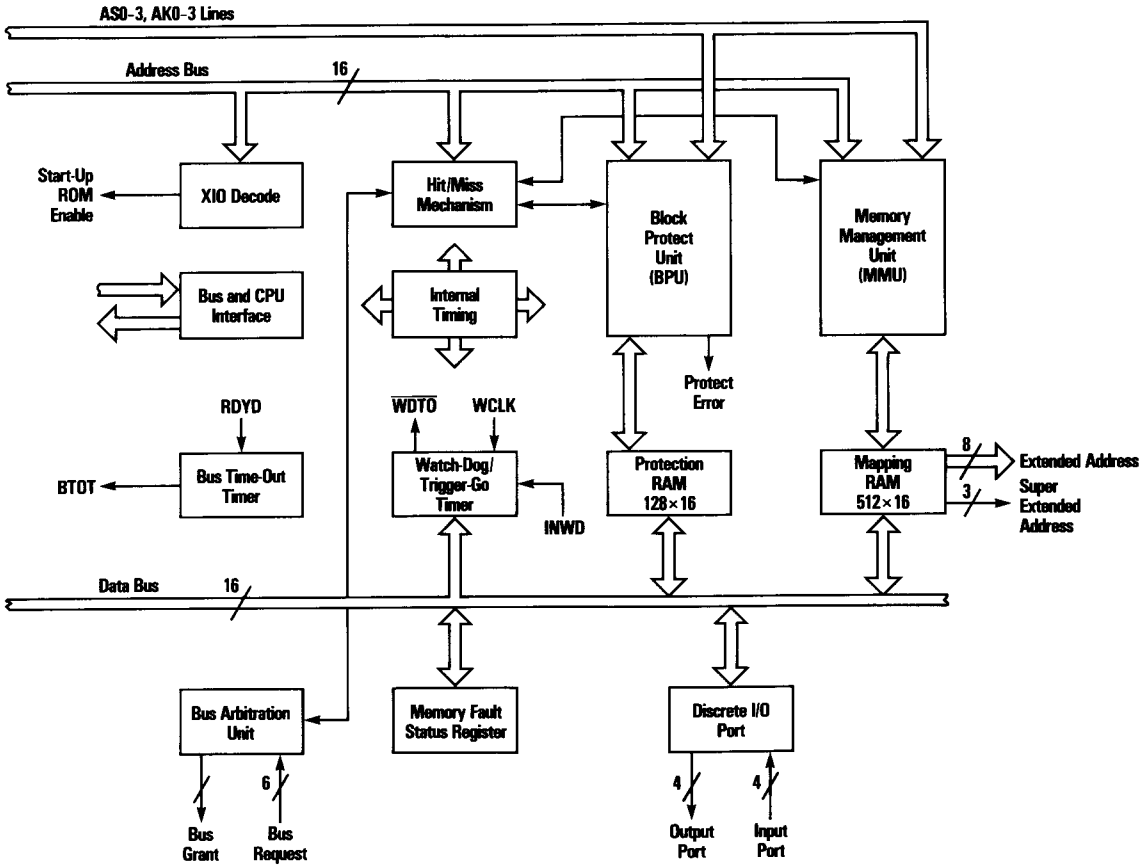


Logic Symbol



Chip Layout

L64550 MBU Block Diagram

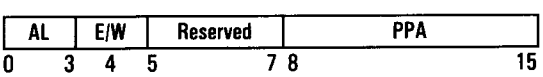


Block Descriptions

The L64550 MBU is a high performance 1.5-micron HCMOS chip which supports the L64500 CPU. The L64550 MBU contains all the optional functional blocks that enhance the MIL-STD-1750A (Notice 1) system.

Memory Management Unit (MMU) – Performs the logical-to-physical address translation and protection of logical space in 4 K word granularity using an on-chip 512×16 cache RAM. It allows addressing up to 1 M word of memory with access lock/access key comparison, execute, and write protection according to MIL-STD-1750A. Super Extended Address (SEA) bits are available to allow addressing up to 8 M words using the MIL-STD-1750A reserved bits in the physical page address.

Page registers of the MMU reside in internal static RAM. The page register organization is described in Figure 1.



AL: Access Lock
E/W: Execute/Write protect
Reserved: Not to be used for MIL-STD-1750A compliance
PPA: Physical Page Address

Figure 1

Block Descriptions (Continued)

The page register manipulation in the L64550 MBU occurs as a result of the L64500 CPU executing one of the instructions shown in Table 1. These instructions belong to the XIO class and are privileged.

Table 1. Page Register Manipulation Instructions

Mnemonic	I/O Command	Effect
WIPR	51XY	Write Instruction Page Register
WOPR	52XY	Write Operand Page Register
RIPR	D1XY	Read Instruction Page Register
ROPR	D2XY	Read Operand Page Register

X is the page register group; Y is the register within that group

Figure 2 shows the mapping structure of the MMU which configures to the MIL-STD-1750A.

Applications not requiring conformance with MIL-STD-1750A can use the page register's three reserved bits as additional address bits expanding the addressing capability to 8 M words.

The MMU employs two means to check for protection violations. It compares the Access Key (AK) from the CPU to the Access Lock (AL) field in the page register. It also examines the write protect (W) bit in the page register if data space is addressed, or the execute protect (E) bit in the page register if instruction space is addressed. If a violation occurs, it asserts the Memory Protect Error signal. Page registers are read or written by means of XIO instructions.

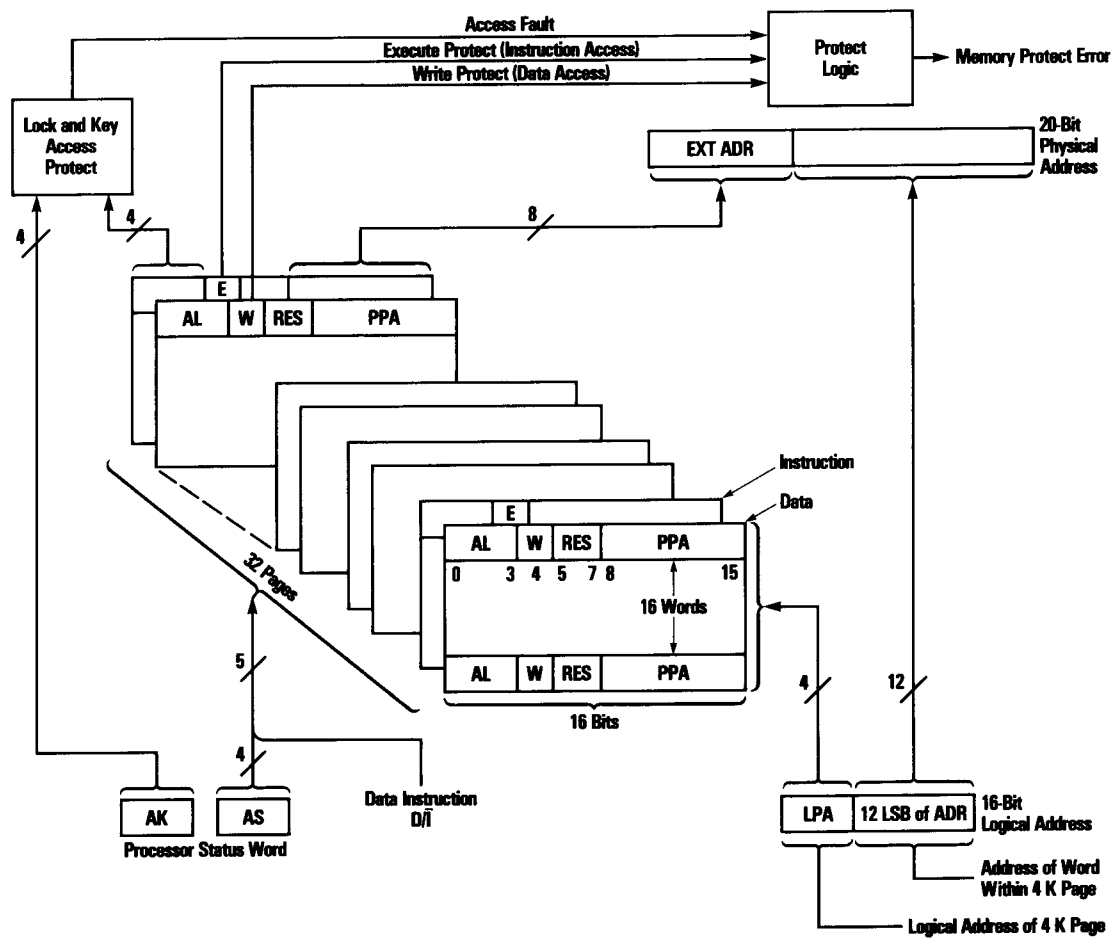


Figure 2. MMU Mapping Structure

Block Descriptions (Continued)

The access key (AK) furnished by the CPU consists of four bits, in which:

- Lock 0F is an "unlocked" lock and allows all keys.
- Key 00 is the "master" key and is acceptable to all access lock codes.
- Keys 01 through 0E are acceptable only to their own matched locks or the "unlocked" lock 0F. For example, if the AK from the CPU equals 0A, the Access Lock in the page register must be either 0A or 0F, or else the MMU asserts the Memory Protect Error output.
- Key 0F is acceptable only to the lock 0F.

Table 2 maps the relationships of MMU locks to CPU keys.

Table 2. Correlation of Locks and Keys

Lock	Key
0	0, 0
1	0, 1
2	0, 2
3	0, 3
4	0, 4
5	0, 5
6	0, 6
7	0, 7
8	0, 8
9	0, 9
A	0, A
B	0, B
C	0, C
D	0, D
E	0, E
F	All keys

Block Protect Unit (BPU) – Provides write protection in 1 K page granularity for up to 1 M word of physical memory for both L64500 CPU and DMA access using an on-chip 128 × 16 RAM as a look-up table. Each bit in the look-up table represents a 1 K word page in physical memory. The L64500 CPU instructions for manipulating the RAM map are shown in Table 3.

Table 3. Map Manipulation Instructions

MMU Control	I/O Command	Manipulation
LMP	50XX	Load Memory Protect RAM
RMP	D0XX	Read Memory Protect RAM
MPEN	4003	Memory Protect Enable

XX is the look-up table address, 00–FF

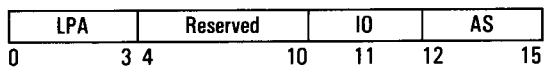
Hit/Miss Mechanism – It is designed to work at high frequency with minimal wait state insertion. If the bus access has been transferred to a DMA device, the hit/miss set-up page will be saved until the bus access has been returned to the CPU.

MMU/BPU Wait States

Freq	15-25 MHz	25-40 MHz
Memory Read		
MMU/BPU		
Hit	0	1
Miss	3	3
Memory Write		
MMU/BPU		
Hit	0	1
Miss	4	4
MMU only		
Hit	0	1
Miss	3	3
BPU only		
Hit	0	1
Miss	3	3

Note: If the L64550 is running slower than the L64500 CPU, a minimum of 1 wait state must be added.

Memory Fault Status Register (MFSR) – The memory fault status register provides the page register selection designators associated with memory faults. The page register designators captured by the MFSR are valid for the memory reference causing the fault. The faults setting bits 0, 1, 2, or 8 of the Fault Register of the L64500 CPU shall cause MFSR to be set.



LPA: Address of page register within the set
Reserved: Not to be used
IO: Instruction/Operand page set selector (1 = instruction)
AS: Address of selection group

XIO Decode – This block is used to decode XIO commands for initialization write protect, general purpose XIO commands and start-up ROM enable.

Watch-Dog/Trigger-Go Counter – This counter can be set by the user. An input clock (WCLK) is divided 200 times before it is used by an 8-bit counter.

Bus Time-Out Timer – This timer activates an output when a memory or I/O device does not respond with READY DATA ($\overline{RDYD}$) within 200 system clocks (CCLK). See pin descriptions for more details.

Discrete I/O Register – This block contains 4 discrete I/O ports. See pin descriptions for more details.

Bus Arbitration – A bus arbitration unit with 6 bus masters. See pin descriptions for more details.

Bus and L64500 CPU Interface – This interface allows for high speed data transfer with minimum impact on system performance. Furthermore it allows for easy connection of each device. See Figure 3.

Block Descriptions
(Continued)

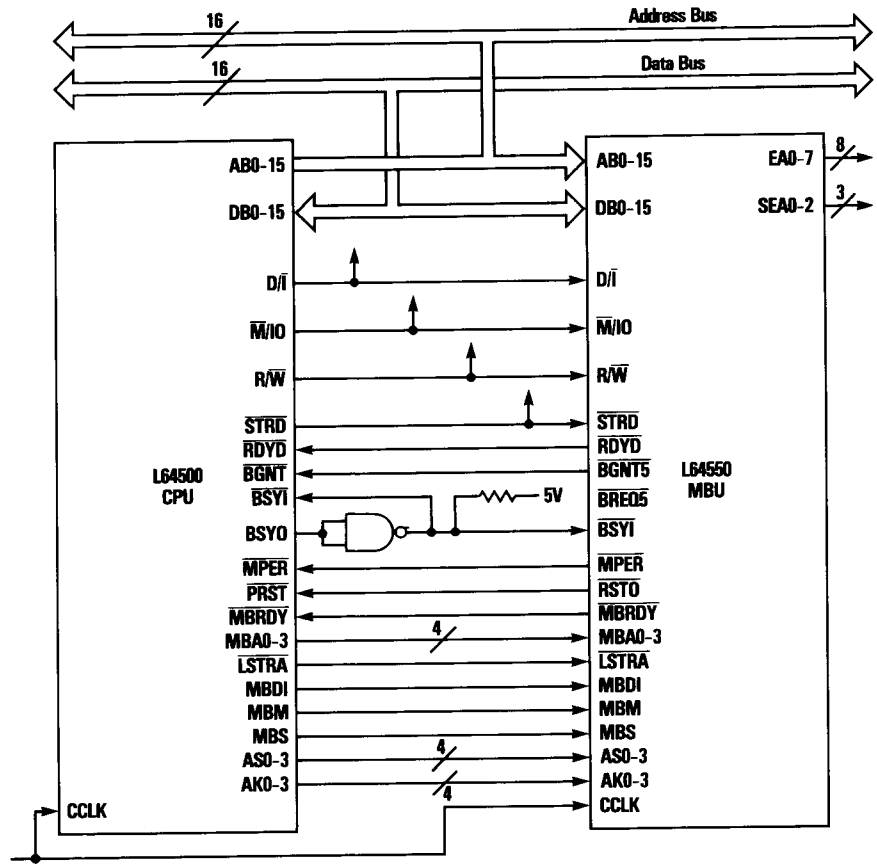


Figure 3. L64500 CPU and L64550 MBU Connection Diagram

Pin Descriptions

The logic symbol on the front page of this data sheet defines the different pin groupings outlined in this section. The pin groupings are: Bus Signals, Bus Controls, Bus Arbitration, Discrete Lines, Configuration Signals, Special XIO Commands, CPU Interface, Clocks, Faults, Special Signals and Test Functions. Figure 4 defines the pin assignments for the L64550. All inputs and outputs are TTL compatible; see DC table for complete information. All I/Os are protected against latch-up and static discharge to a specification of 200 mA and 2000 V.

Power and Ground (VDD, VSS) – There are 19 VDD and VSS pins to distribute the power and ground requirements of the chip. These additional pins will reduce noise due to typically high transient currents generated by fast switching HCMOS output drivers. Standard TTL voltage levels can be applied (see DC specifications).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VDD	AB12	AB8	AB7	AB5	AB1	AB0	VDD	MBA2	MBA1	$\overline{\text{INTOT}}$	TSTO2	$\overline{\text{INWD}}$	$\overline{\text{RDIC}}$	DSCO15
B	MBDI	AB15	AB11	AB9	AB6	AB3	AB2	MBA3	$\overline{\text{BTOT}}$	D/$\overline{\text{I}}$	$\overline{\text{WDTO}}$	WCLK	$\overline{\text{IWPRT}}$	VSS	DSCO12
C	$\overline{\text{MMEN}}$	R/$\overline{\text{W}}$	AB14	AB13	AB10	AB4	$\overline{\text{RDYD}}$	VSS	MBA0	TSTI1	TSTI0	$\overline{\text{SUREN}}$	DSCO14	DSCI15	DSCI12
D	$\overline{\text{BPEN}}$	MBM	VSS										DSCO13	DSCI13	$\overline{\text{RORC}}$
E	$\overline{\text{MBRDY}}$	$\overline{\text{LSTRA}}$	$\overline{\text{STRD}}$										DSCI14	$\overline{\text{ODC}}$	$\overline{\text{DSCNR}}$
F	$\overline{\text{RSTO}}$	SPSC	CCLK										MBS	VSS	NC
G	$\overline{\text{PSTRA}}$	VSS	$\overline{\text{PRST}}$										NC	VDD	NC
H	$\overline{\text{M}}$/IO	GPXIO	VDD										VSS	DB14	DB15
J	AS3	AS1	VSS										DB11	DB10	DB13
K	AS2	AS0	AK3										DB7	DB8	DB12
L	AK2	AK1	VSS										DB4	DB6	DB9
M	AK0	$\overline{\text{UAER}}$	TSTI3										DB0	DB3	VSS
N	DMA STF	$\overline{\text{PAER}}$	TSTI4	EBM0	$\overline{\text{BGNT0}}$	$\overline{\text{BGNT4}}$	$\overline{\text{BREQ1}}$	VDD	VSS	EA4	SEA1	ENSE	TSTO1	DB1	DB5
P	$\overline{\text{MPER}}$	TSTI2	EBM1	$\overline{\text{DMAC}}$	$\overline{\text{BGNT2}}$	$\overline{\text{BGNT5}}$	$\overline{\text{BREQ0}}$	$\overline{\text{BREQ4}}$	EA2	EA3	EA6	SEA0	SEA2	TSTO0	DB2
Q	$\overline{\text{BSYI}}$	EBM2	$\overline{\text{BGNT1}}$	$\overline{\text{BGNT3}}$	VSS	$\overline{\text{BREQ2}}$	$\overline{\text{BREQ3}}$	$\overline{\text{BREQ5}}$	EA0	EA1	EA5	EA7	VSS	VDD	VSS

Figure 4. L64550 Pin Diagram (Top View)

Pin Descriptions (Continued)

Name	Symbol	Pin	Description
BUS SIGNALS			
Address Bus	AB15 AB14 AB13 AB12 AB11 AB10 AB9 AB8 AB7 AB6 AB5 AB4 AB3 AB2 AB1 AB0	B2 C3 C4 A2 B3 C5 B4 A3 A4 B5 A5 C6 B6 B7 A6 A7	Sixteen input address lines indicating a memory or I/O location generated by the L64500 CPU or an external device. AB0 is the most significant bit (MSB).
Data Bus	DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0	H15 H14 J15 K15 J13 J14 L15 K14 K13 L14 N15 L13 M14 P15 N14 M13	A 16-bit bidirectional data bus used to transmit or receive data from the I/O locations in the L64550 MBU. DB0 is the most significant bit (MSB).
Extended Address	EA7 EA6 EA5 EA4 EA3 EA2 EA1 EA0	Q12 P11 Q11 N10 P10 P9 Q10 Q9	Eight output address lines are used to extend the memory address space beyond 64 K words. These lines in conjunction with Bus Address lines AB15–AB4 from the L64500 CPU chip (or DMA) extend the memory space up to 1 M words. EA0 is the most significant bit (MSB).
Super Extended Address	SEA2 SEA1 SEA0	P13 N11 P12	Three output address lines allow memory expansion beyond 1 M words. These lines in conjunction with Extended Address lines EA7–EA0 and Bus Address lines AB15–AB4 extend the memory space up to 8 M words. NOTE: These lines are active only when the ENSE input is HIGH.
BUS CONTROLS			
Data or Instruction	$\overline{D/I}$	B10	An input signal that indicates whether the current bus cycle access is for Data (HIGH) or Instruction (LOW).
Memory or I/O	$\overline{M/IO}$	H1	An input signal that indicates whether the current bus cycle is for Memory (LOW) or I/O (HIGH).
Read or Write	$\overline{R/W}$	C2	An input signal that indicates whether the current bus cycle is Read (HIGH) or Write (LOW) cycle.
Ready Data	$\overline{RDYD}$	C7	An active LOW output asserted by the L64550 MBU to indicate the completion of a data cycle. In cases where the L64550 MBU requires an extension of a data cycle from the L64500 CPU, this line is held HIGH by the L64550 MBU. This signal is 3-state during bus cycles not assigned to the L64550 MBU. NOTE: In case of a Bus Time-Out (i.e., a Memory or I/O device has not responded with $\overline{RDYD}$), the L64550 MBU asserts the $\overline{RDYD}$ signal in conjunction with the $\overline{BTOT}$ signal.
Physical Strobe Address	$\overline{PSTRA}$	G1	An active LOW output asserted by the MBU *only* at DMA bus cycles. This signal can be used to externally latch the Memory Address at the LOW-to-HIGH transition of the strobe. This output is 3-state on non-DMA cycles. NOTE: When not active this signal is 3-state and can be connected to the $\overline{PSTRA}$ output of the L64500 CPU chip.

Pin Descriptions (Continued)

Name	Symbol	Pin	Description
BUS CONTROLS			
Strobe Data	$\overline{STRD}$	E3	An active LOW input used to strobe the information on the Data Bus into the L64550 MBU. The data is sampled at the trailing edge (the LOW-to-HIGH transition) of the signal.
BUS ARBITRATION			
Busy Input	$\overline{BSYI}$	Q1	An active LOW input indicates that the bus is currently used by the L64500 CPU or an external bus user.
Encoded Bus Master	EBM2 EBM1 EBM0	Q2 P3 N4	Three output lines from the Bus Arbitrator module that are active during the DMA cycle. These lines indicate the binary code of the Bus Master ($\overline{BGNT0}$–$\overline{BGNT4}$) that has been granted the bus by the Bus Arbitrator.
Bus Request	$\overline{BREQ5}$ $\overline{BREQ4}$ $\overline{BREQ3}$ $\overline{BREQ2}$ $\overline{BREQ1}$ $\overline{BREQ0}$	Q8 P8 Q7 Q6 N7 P7	Six active LOW inputs used by the Bus Arbitrator module in the L64550 MBU. A LOW signal indicates to the Bus Arbitrator that a particular bus user requires the bus for data transfer. $\overline{BREQ0}$ has the highest priority.
Bus Grant	$\overline{BGNT5}$ $\overline{BGNT4}$ $\overline{BGNT3}$ $\overline{BGNT2}$ $\overline{BGNT1}$ $\overline{BGNT0}$	P6 N6 Q4 P5 Q3 N5	Six active LOW outputs used to indicate to a bus user that no higher priority user is requesting the bus. Each output corresponds to the particular bus request input. NOTE: The $\overline{BGNT5}$ should be connected to the $\overline{BGNT}$ input of the L64500 CPU.
DMA Status Flag	DMASTF	N1	An output indicating the status of the DMA module. A HIGH indicates that the module is enabled.
DMA Cycle	$\overline{DMAC}$	P4	An active LOW output indicates that the bus is currently granted to an external DMA device.
DISCRETE LINES			
Discrete Input	DSCI15 DSCI14 DSCI13 DSCI12	C14 E13 D14 C15	Four input lines that can be sensed by the RDI (XIO = A009) command.
Read Discrete Input Command	$\overline{RDIC}$	A14	An active LOW output indicates the execution of the XIO = A009 command. When active, the four Discrete Inputs (DSCI15–DSCI12) are sensed.
Discrete Outputs	DSCO15 DSCO14 DSCO13 DSCO12	A15 C13 D13 B15	Four output lines from the Discrete Output Register. This register is four bits wide and is loaded with the OD (XIO = 2008) command. DSCO15 is connected internally to DB15.
Output Discrete Command	$\overline{ODC}$	E14	An active LOW output indicates the execution of the XIO = 2008 command. When active the four Discrete Outputs are loaded into the register.
Read Output Register Command	$\overline{RORC}$	D15	An active LOW output indicates the execution of the RDOR command (XIO = A008).
Discrete NOR	$\overline{DSCNR}$	E15	An active LOW output indicates that at least one of the Discrete Inputs (DSCI15–DSCI12) is HIGH. When not active, this output is 3-state.
CONFIGURATION SIGNALS			
MMU Enable	$\overline{MMEN}$	C1	An active LOW input enables the operation of the Memory Management Unit (MMU) in the L64550 MBU. In applications where the MMU is not required, this input must be connected to HIGH, otherwise if used connect to GND.
BPU Enable	$\overline{BPEN}$	D1	An active LOW input enables the operation of the Block Protection Unit (BPU) in the L64550 MBU. In applications where the BPU is not required, this input must be connected to HIGH, otherwise if used connect to GND.
Enable Super Extension	ENSE	N12	An active HIGH input enables the extension of the Memory Address space beyond 1 M words. In applications where this super extension is required, this input must be connected to HIGH, otherwise connect to GND. NOTE: The Super Extension feature is beyond the requirements of the MIL-STD-1750A and is not supported by the BPU.
Speed Select	SPSC	F2	An input signal to indicate the speed range of the CCLK. A HIGH indicates a clock rate beyond 20 MHz, otherwise this input must be connected to GND.

Pin Descriptions (Continued)

Name	Symbol	Pin	Description
CLOCKS			
CPU Clock	CCLK	F3	Input clock signal (square-wave, 40% to 60% duty cycle). The clock signal must be the same (frequency and phase) as that supplied to the L64500 CPU chip.
Watch-Dog	WCLK	B12	A square-wave clock input for the Watch-Dog module in the L64550. NOTE: The clock input is divided internally by 200 prior to clocking the Watch-Dog counter.
SPECIAL XIO COMMANDS			
General Purpose XIO Command	$\overline{\text{GPXIO}}$	H2	An active LOW output indicates the execution of the XIO=0402 command.
Initialization Write Protect	$\overline{\text{IWPRT}}$	B13	An active LOW output activated when $\overline{\text{PRST}}$ is LOW and remains LOW until the MPEN (XIO=4003) command is executed. This signal is intended primarily for write protection of main memory during the initialization sequence. When not used this signal is 3-state.
Start-Up ROM Enable	$\overline{\text{SUREN}}$	C12	An active LOW output indicates that an external Start-Up ROM can be used. This output goes LOW by the ESUR command (XIO=4004) or when $\overline{\text{PRST}}$ is LOW and remains LOW until the DSUR (XIO=4005) command is executed. When not active, this output is 3-state.
CPU INTERFACE			
Logical Strobe Address	$\overline{\text{LSTRA}}$	E2	An active LOW input from the L64500 CPU used by the L64550 MBU to latch the logical address at the LOW-to-HIGH transition of the strobe.
MBU Ready	$\overline{\text{MBRDY}}$	E1	An active LOW output to the L64500 CPU indicating the completion of the L64550 MBU internal address cycle. This signal should only be connected to the $\overline{\text{MBRDY}}$ output of the L64500 CPU.
MBU Data or Instruction	MBDI	B1	An input line from the L64500 CPU used only by the L64550 MBU. This line should be connected to the MBDI output of the L64500 CPU.
MBU Status	MBS	F13	An input line from the L64500 CPU used only by the L64550 MBU. This line should be connected to the MBS output of the L64500 CPU.
MBU Memory	MBM	D2	An input line from the L64500 CPU used only by the L64550 MBU. This line should be connected to the MBM output of the L64500 CPU.
MBU Address	MBA3 MBA2 MBA1 MBA0	B8 A9 A10 C9	Four input lines from the L64500 CPU used only by the L64550 MBU. These lines should be connected to the MBA outputs of the L64500 CPU.
Reset Output	$\overline{\text{RSTO}}$	F1	An active LOW output asserted by the L64550 MBU in response to the $\overline{\text{PRST}}$ input. This output remains LOW until the completion of the initialization sequence of the L64550 MBU. NOTE: This output should be connected to the $\overline{\text{PRST}}$ input of the L64500 CPU.
Address State	AS3 AS2 AS1 AS0	J1 K1 J2 K2	Four input lines from the L64500 CPU or an external DMA device used to select the page group in the L64550 MBU.
Access Key	AK3 AK2 AK1 AK0	K3 L1 L2 M1	Four input lines from the L64500 CPU or an external DMA device used to match the Access Key.

Pin Descriptions (Continued)

Name	Symbol	Pin	Description
FAULT SIGNALS			
Memory Protect Error	$\overline{\text{MPER}}$	P1	An active LOW output indicating that the current bus cycle is violating the memory protection conditions of the MMU and BPU. This signal is active when the Access Key (AK) field does not match the Address Lock (AL) or when an attempt is made to execute an instruction from a protected area, or to write into a memory location protected by the MMU or BPU.
Unimplemented Address Error	$\overline{\text{UAER}}$	M2	An active LOW input used by the Memory Fault Status Register (MFSR) in the L64550 MBU. This input will go LOW when an attempt is made to access an unimplemented memory or I/O location.
Parity Error	$\overline{\text{PAER}}$	N2	An active LOW input used by the Memory Fault Status Register (MFSR) in the L64550 MBU. This input will go LOW when a Parity Error is detected during memory or I/O bus cycles. NOTE: When parity error detection is not implemented, this input should be pulled HIGH.
SPECIAL SIGNALS			
Power-Up Reset	$\overline{\text{PRST}}$	G3	An active LOW input that initializes all the internal modules of the L64550 MBU in accordance to the MIL-STD-1750A.
Inhibit Watch-Dog	$\overline{\text{INWD}}$	A13	An active LOW input that inhibits the Watch-Dog counter from decrementing.
Watch-Dog Time-Out	$\overline{\text{WDTO}}$	B11	An active LOW output asserted by the Watch-Dog counter in the L64550 MBU. This output is active when the Watch-Dog counter has not been reinitialized with the Trigger-Go (XIO=400B) command at the appropriate time, and the down counter simultaneously reaches zero.
Bus Time-Out Timer	$\overline{\text{BTOT}}$	B9	An active LOW output asserted by the Bus Time-Out Timer in the L64550 MBU. This output is activated when a memory or I/O device does not respond with $\overline{\text{RDYD}}$ within 200 clocks (CCLK) after the $\overline{\text{STRD}}$ signal goes LOW.
Inhibit Time-Out Timer	$\overline{\text{INTOT}}$	A11	An active LOW input that inhibits the Time-Out Timer from decrementing.
TEST FUNCTION			
Test Inputs	TSTI0 TSTI1 TSTI2 TSTI3 TSTI4	C11 C10 P2 M3 N3	These inputs are used for factory testing and must be connected to GND.
Test Outputs	TSTO0 TSTO1 TSTO2	P14 N13 A12	These outputs are used for factory testing. USERS SHOULD NOT CONNECT THESE PINS.

Timing Characteristics

This section gives timing characteristics for the L64550. Figures 5 through 13 depict the timing waveforms associated with L64550 signals. Throughout these figures, the following abbreviated symbols are used:

Sn—Clock Cycles
TL—HIGH-to-LOW Transition
TH—LOW-to-HIGH Transition
TS—Setup Time
TD—Hold Time
TZ—to High Impedance State
TIS—Input Setup Time
TOS—Output Setup Time

CPU Timing Characteristics (Preliminary): VDD = 4.5V to 5.5V, TA = −55°C to 125°C, CL = 50 pF

Pin Name	Symbol	Delay (ns)		
		Min	Typ	Max
$\overline{BSYI}$	TL TH TS		12 10	
M/$\overline{IO}$, R/$\overline{W}$, D/$\overline{I}$	TS TD		20 22	
AB0–15	TS TD		14 14	
DB0–15	TS TD		 5	
$\overline{STRD}$	TL TD		15 13	

DMA Hit Timing

Pin Name	Symbol	Delay (ns)		
		Min	Typ	Max
$\overline{MBRDY}$	TL TH		20 18	
EA0–EA7	TS		5	
$\overline{MPER}$	TL		20	
$\overline{PSTRA}$	TL TH TZ		5 18 15	

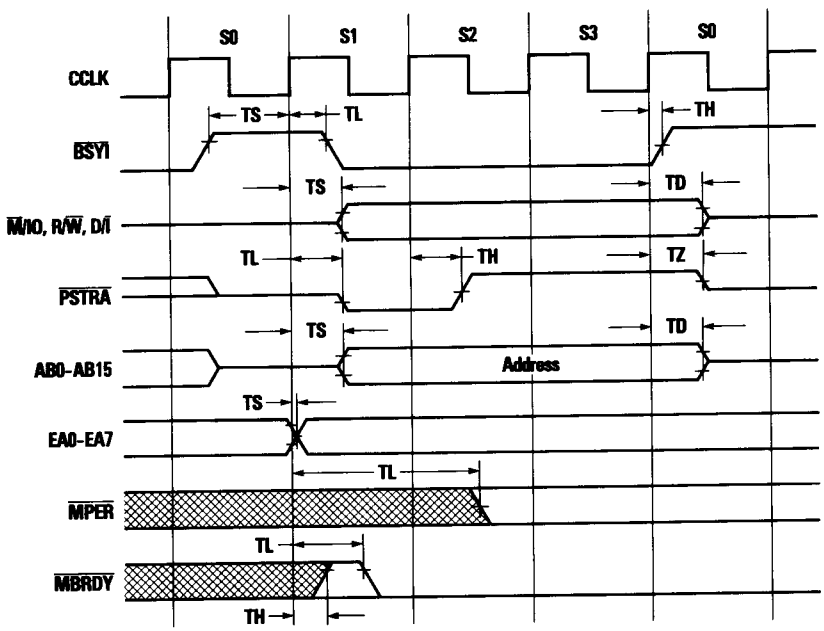


Figure 5. CPU Hit Cycle

Timing Characteristics (Continued)

CPU Miss Cycle Timing

Pin Name	Symbol	Delay (ns)		
		Min	Typ	Max
$\overline{MBRDY}$	TL TH		21 15	
EA0–EA7	TS		5	
$\overline{MPER}$	TL		30	
$\overline{PSTRA}$	TL TH TZ		15 12 15	

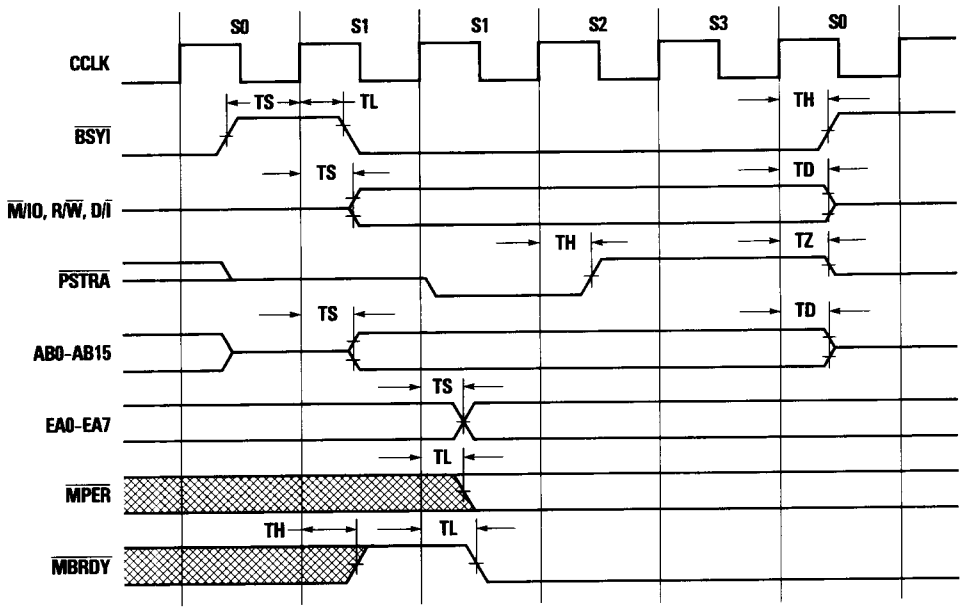


Figure 6. CPU Miss Cycle

Timing Characteristics
(Continued)

MMU and BPU Read/Write Miss Timing

Pin Name	Symbol	Delay (ns)		
		Min	Typ	Max
$\overline{MBRDY}$	TL TH		30 15	
EA0–EA7	TS		35	
$\overline{MPER}$	TL		35	
$\overline{PSTRA}$	TL TH TZ		16 12 15	

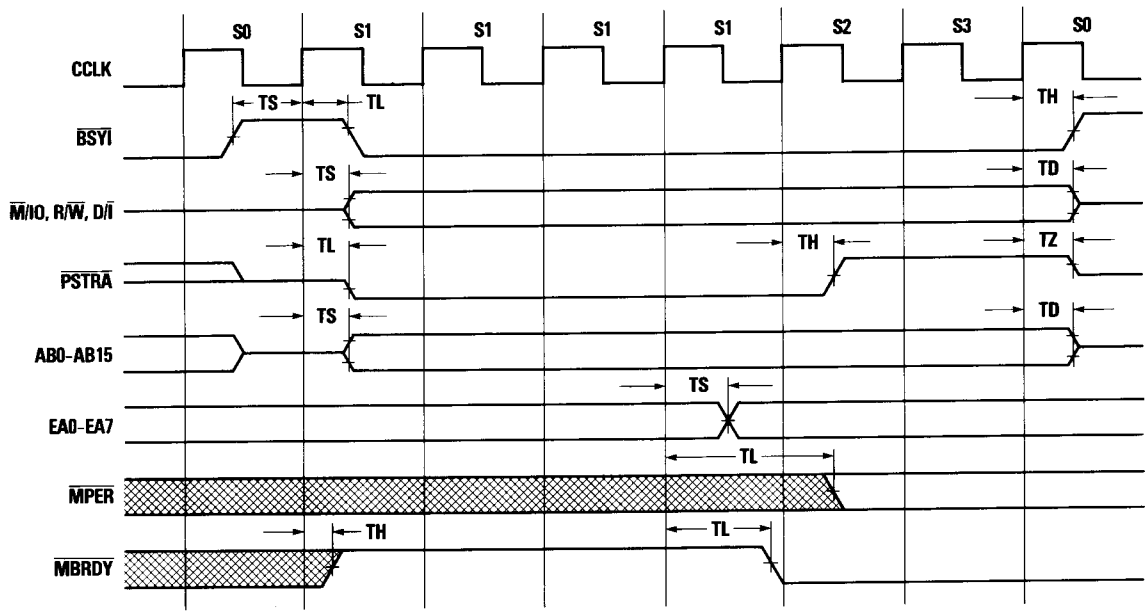


Figure 7. Miss Read Cycle (MMU and BPU)

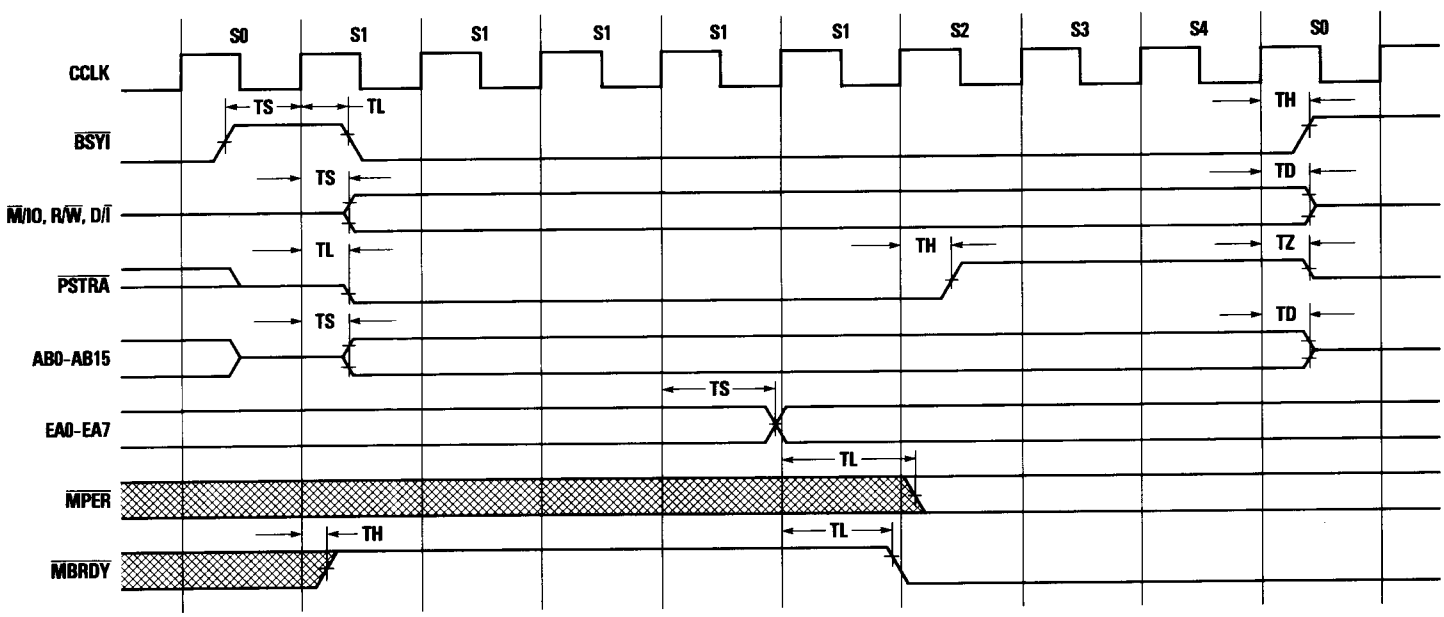


Figure 8. Miss Write Cycle (MMU and BPU)

Timing Characteristics
(Continued)

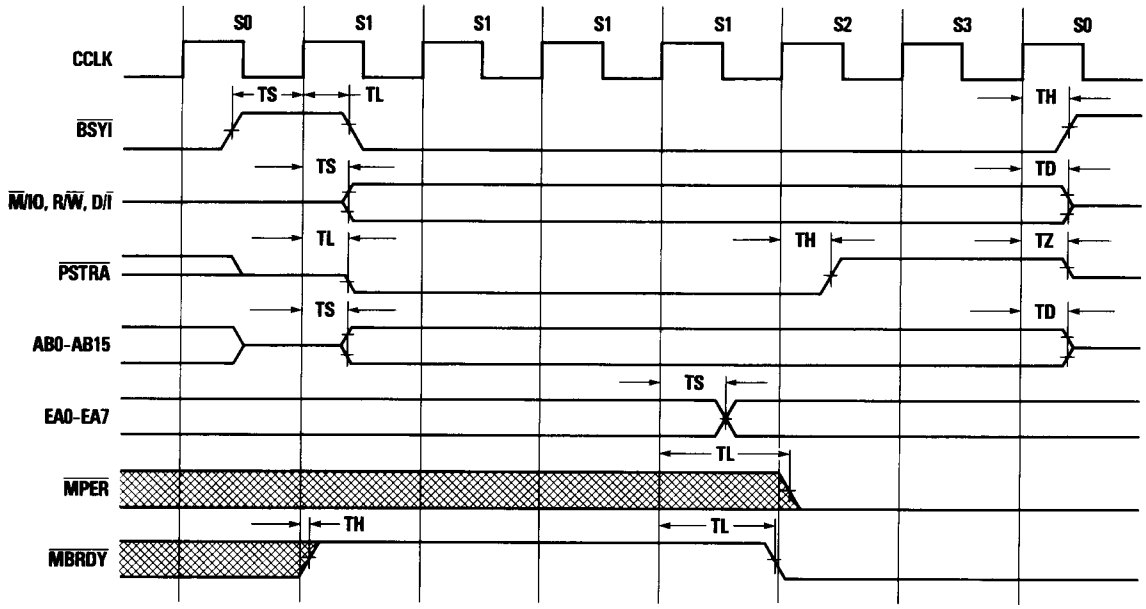


Figure 9. Miss Cycle (MMU Only)

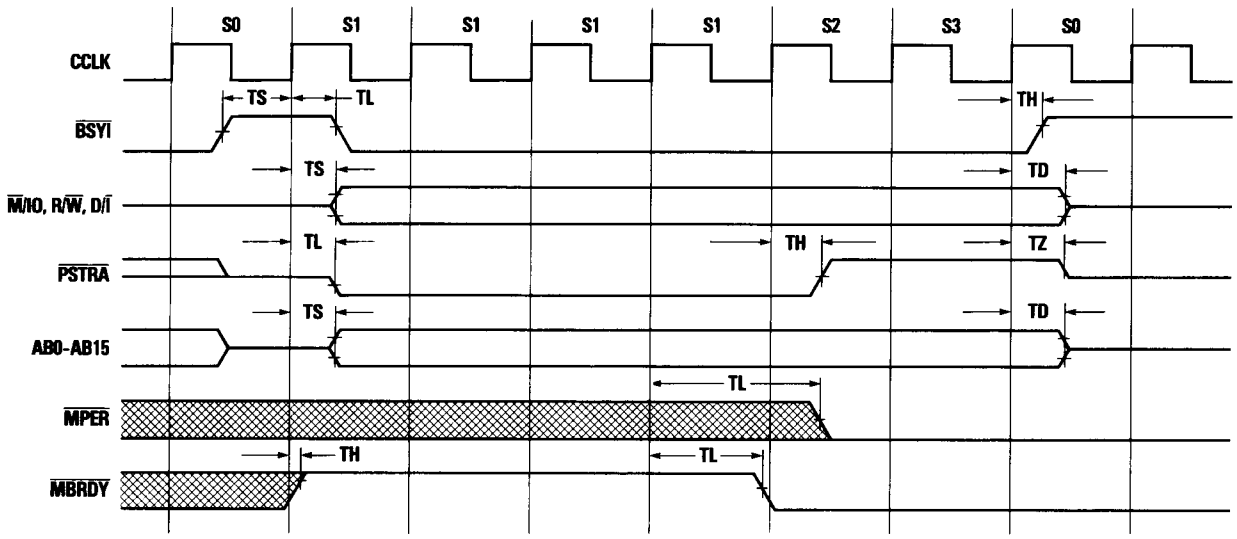


Figure 10. Miss Cycle (BPU Only)

Timing Characteristics
(Continued)

I/O Read Timing

Pin Name	Symbol	Delay (ns)		
		Min	Typ	Max
$\overline{RDYD}$	TS TD		20 32	
DB0–DB15 (Read Cycle)	TS TD		10 30	

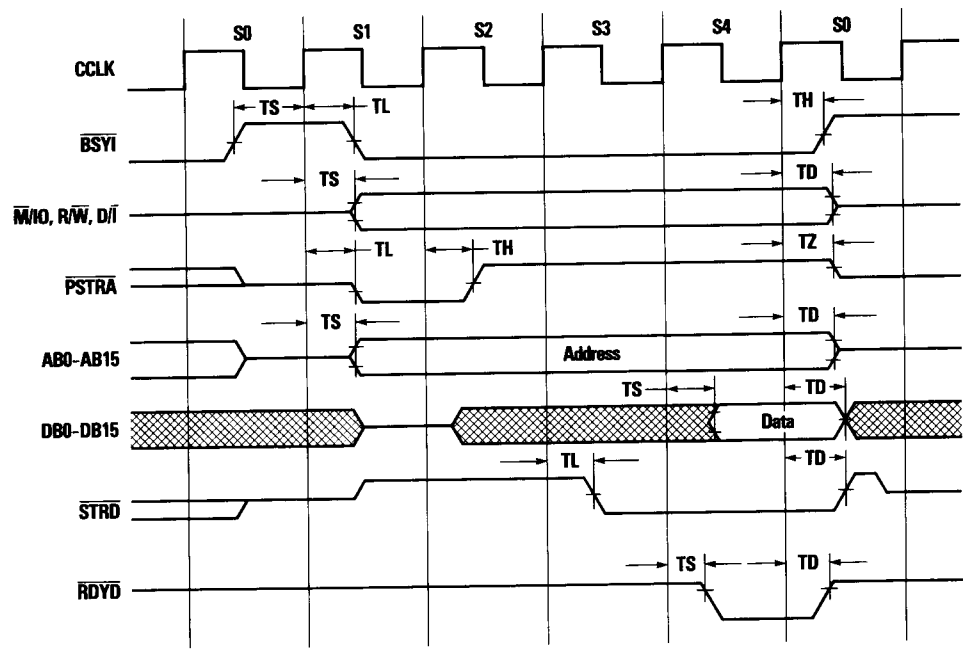


Figure 11. I/O Read Cycle

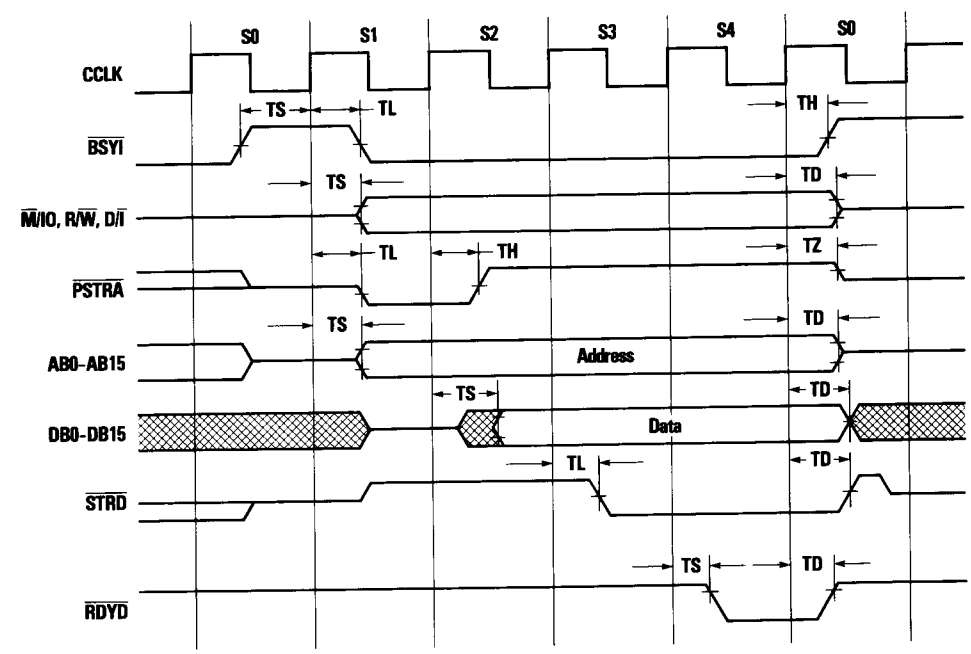


Figure 12. I/O Write Cycle

Timing Characteristics
(Continued)

Arbitration Timing

Pin Name	Symbol	Delay (ns)		
		Min	Typ	Max
$\overline{BGNT0}$–$\overline{BGNT5}$	TL TH		23 18	
$\overline{DMAC}$	TL TH		3 22	
EBM0–2	TS		20	

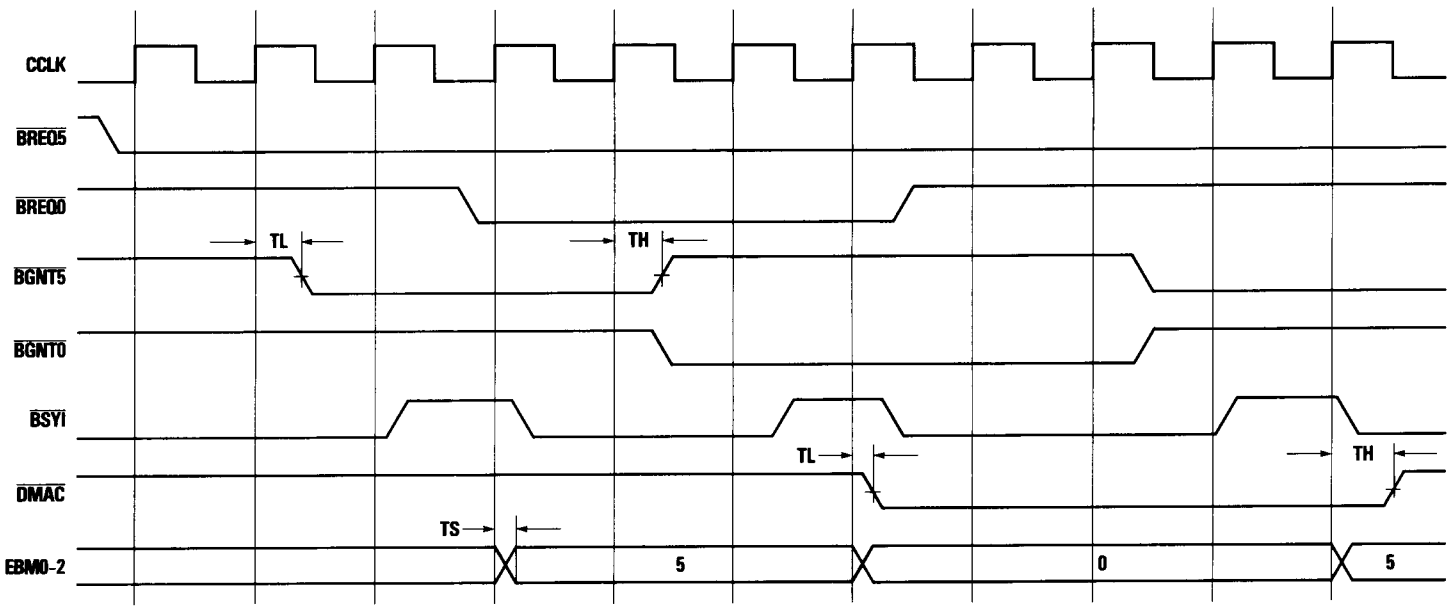


Figure 13. Bus Arbitration

Operating Characteristics

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	−0.3 to +7	V
Input Voltage	VIN	−0.3 to VDD +0.3	V
DC Input Current	IIN	±10	mA
Storage Temperature Range (Ceramic)	TSTG	−65 to +150	°C
Storage Temperature Range (Plastic)	TSTG	−40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+3 to +6	V
Operating Ambient Temperature Range Military	TA	−55 to +125	°C

DC Characteristics: VDD = 5 V ±10%, TA = −55°C to +125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIL	Voltage Input LOW				0.8	V
VIH	Voltage Input HIGH		2.25			V
IIL	Input Current LOW		−100	−30	−8	μA
IIN	Input Current HIGH				40	μA
VOH	Voltage Output HIGH All Others EBM0–2, $\overline{PSTRA}$, $\overline{RDYD}$ $\overline{MBRDY}$, MPER	 IOH = −3.2 mA IOH = −6.4 mA IOH = −9.6 mA	2.4	4.5		V
VOL	Voltage Output LOW All Others EBM0–2, $\overline{PSTRA}$, $\overline{RDYD}$ $\overline{MBRDY}$, MPER	 IOL = 3.2 mA IOL = 6.4 mA IOL = −9.6 mA		0.2	0.4	V
IOZ	3-State Output Leakage Current	VOH = VSS or VDD	−10	±1	10	μA
IOS	Output Short Circuit Current[1]	VDD = Max, VO = VDD VDD = Max, VO = 0 V	15 −5	50 −25	130 −100	mA mA
IDD	Supply Current	CLK = 20 MHz, CL = 50 pF		100		mA

Note: Not more than one output may be shorted at a time for a maximum duration of one second.

Ordering Information

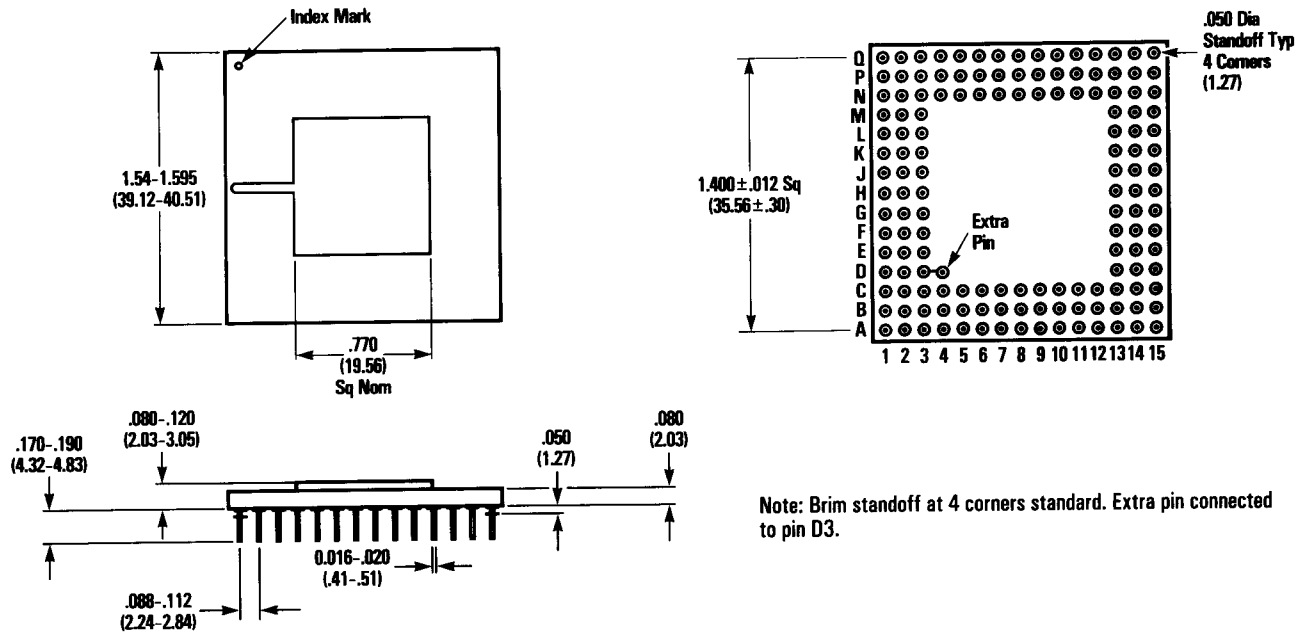
L64550 A G M B

- **B** — Screening Option
  - Blank = Standard Processing
  - B = MIL-STD-883
  - C = Burn-in Only
- **M** — Temperature Range
  - M = Military (−55°C to +125°C)
- **G** — Package
  - G = 144-Pin Ceramic Pin Grid Array
  - X = Dice
  - Other packages available upon request.
- **A** — Speed Range
  - Blank = 15 MHz
  - A = 20 MHz
  - B = 25 MHz
- **L64550** — Device Type
  - L64550
  - MBU Peripheral Device

Valid Options
GMB, GM XMB, XM

Packaging

Initially, the L64550 will be offered in a 144-Pin Grid Array (PGA). The mechanical drawings and dimensions of the package are shown in Figure 14. This package was selected because of its easier breadboarding characteristics. If other package types are required, easy conversion is possible. The different package types available to use are governed by the die cavity and available pins. LSI Logic provides package selector guides for alternative packaging such as Leaded or Leadless chip carriers. Customer unique package requirements can be handled, but must be reviewed by the LSI Logic packaging group.



Note: Brim standoff at 4 corners standard. Extra pin connected to pin D3.

Figure 14. 144-Pin Ceramic Pin-grid Array

Screening Options

The L64550 can be selected as evaluation or production units. Evaluation units have been screened to commercial standards but have the full −55°C to 125°C military temperature specification. These units are not recommended for use in military production environments.

Production units can be ordered to commercial standards, MIL-STD-883B Rev. C and Level S. Contact factory for screening details.

LSI Logic Design System (LDS)

The L64550 can be used with LSI Logic's Design System (LDS) simulation tools as a library element. This unique feature allows the user to develop a full MIL-STD-1750A system environment in software. This environment allows the user to develop accurate systems and sophisticated MIL-STD-1750A associated Application Specific Integrated Circuits (ASIC) offered by LSI Logic. In addition, the user can increase the functionality of the L64550 by adding other circuitry to the library element making the design fit customer-unique requirements. To use this feature, the LSI Logic LDS environment can be licensed or can be accessed through one of LSI Logic's design centers identified on the last page. Training on the LDS system lasts three days.