Ordering number : EN ※4701

Preliminary

SANYO Semiconductors

DATA SHEET

CMOS LSI

LC33864P, M, PL, ML-70/80/10

512K (65536 words × 8 bits) Pseudo-SRAM

Overview

The LC33864 series is composed of pseudo static RAM that operate on a single 5 V power supply and is organized as 65536 words × 8 bits. By using memory cells each composed of a single transistor and capacitor, together with peripheral CMOS circuitry, this series achieves ease of use with high density, high speed, and low power dissipation. Since the LC33864 series products provide refresh counter and timer on chip, this series can easily accomplish auto-refresh and self-refresh by means of $\overline{RFSH}$ input. The available packages are the 32-pin DIP with a width of 600 mil, and the 32-pin SOP with a width of 525 mil.

Features

- 65536 words × 8 bits configuration
- $\overline{CE}$ access time, $\overline{OE}$ access time, cycle time, operating supply current and self-refresh current.

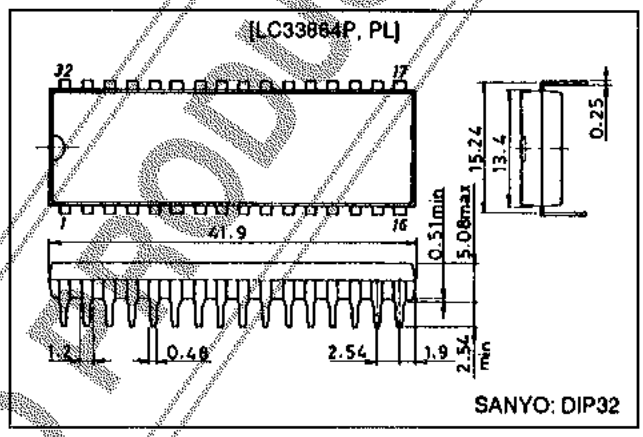
Parameter	LC33864P, M, PL, ML		
	-70	-80	-10
$\overline{CE}$ access time	70 ns	80 ns	100 ns
$\overline{OE}$ access time	30 ns	35 ns	40 ns
Cycle time	115 ns	130 ns	160 ns
Operating supply current	60 mA	70 mA	60 mA
Self-refresh current	1 mA/100 µA (L version)		

- Single 5 V ±10% power supply
- All inputs and outputs (I/O) TTL compatible
- Fast access time and low power dissipation
- 8 ms refresh using 512 refresh cycles
- Supports auto-refresh, self-refresh and $\overline{CE}$-only refresh
- Low-power version: 100 µA standby current
- Packages
  32-pin DIP plastic package: LC33864P
  32-pin SOP plastic package: LC33864M

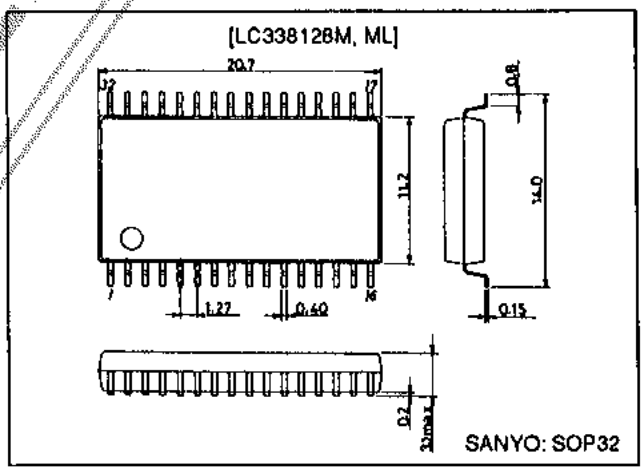
Package Dimensions

unit: mm

3192-DIP32



3205-SOP32



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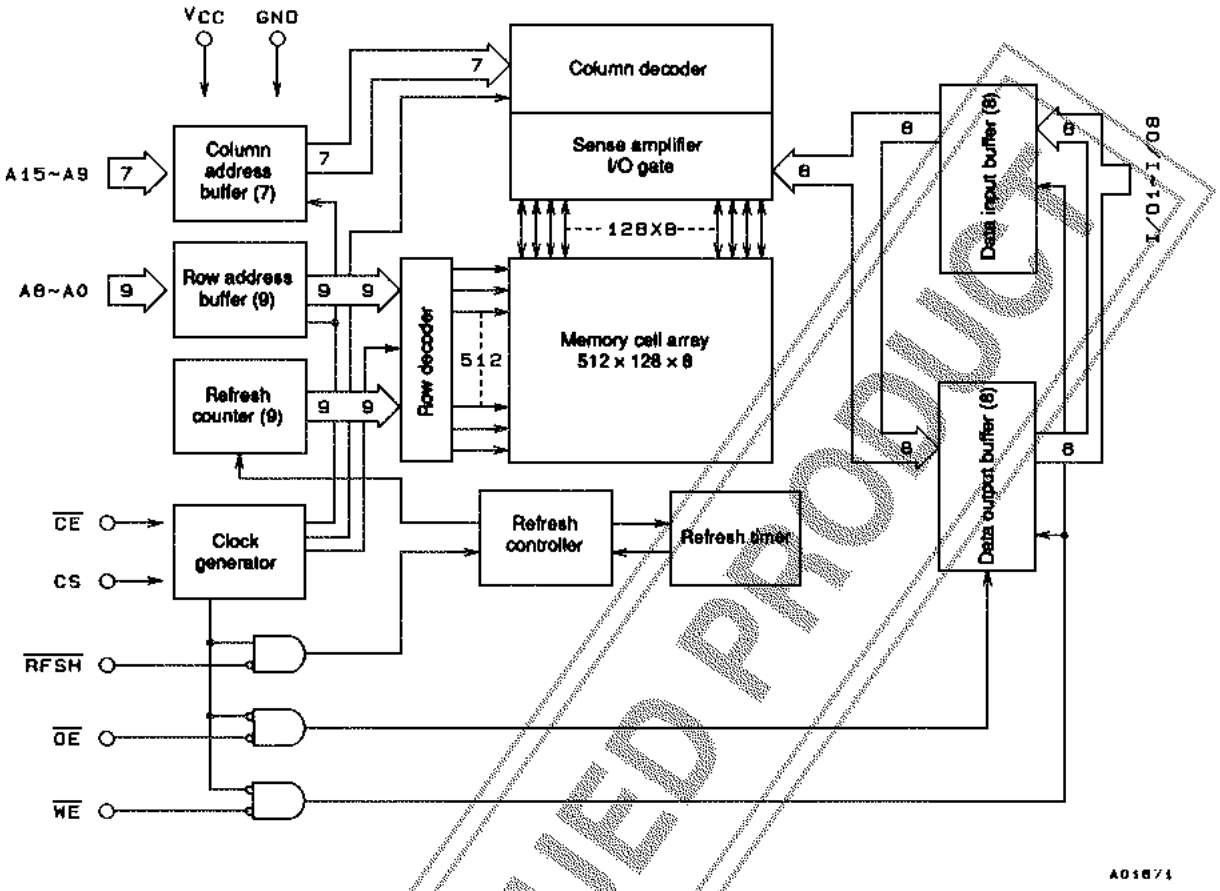
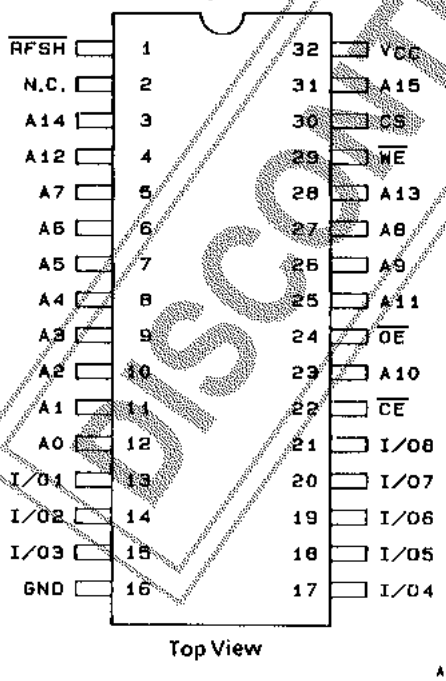
Block Diagram



Pin Assignment

DIP32, SOP32



Pin Functions

A0 to A15	Address input
$\overline{WE}$	Read/write input
$\overline{OE}$	Output enable input
$\overline{RFSH}$	Refresh input
$\overline{CE}$	Chip enable input
CS	Chip select input
I/O1 to I/O8	Data input/output
Vcc	Power supply
GND	Ground

Function Logic

$\overline{CE}$	CS	$\overline{OE}$	$\overline{WE}$	$\overline{RFSH}$	A0 to 8	A9 to 15	I/O1 to 8	State
L	H	L	H	X	VX	VX	OUT	Read
L	H	X	L	X	VX	VX	IN	Write
L	H	H	H	X	VX	X	HZ	$\overline{CE}$ only refresh
L	L	X	X	X	X	X	HZ	CS standby
H	X	X	X	L	X	X	HZ	Self-refresh
H	X	X	X	NP	X	X	HZ	Auto-refresh
H	X	X	X	H	X	X	HZ	Standby

H: High-level input of V_{IN} = 6.5 V to V_{IH} (min)
L: Low-level input of V_{IN} = V_{IL} (max) to −1.0 V
NP: Negative-polarity pulse input
X: High- or Low-level input
VX: "IN" when $\overline{CE}$ = L is confirmed, then "X"
HZ: High impedance
IN: Input state
OUT: Output state

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	V_{CC} max	−1.0 to +7.0	V	1
Input voltage	V_{IN}	−1.0 to +7.0	V	1
Output voltage	V_{OUT}	−1.0 to +7.0	V	1
Allowable power dissipation	Pd max	600	mW	1
Output short current	I_{OUT}	50	mA	1
Operating temperature range	Topr	0 to +70	°C	1
Storage temperature range	Tstg	−55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage	V_{IL}	−1.0		+0.8	V	2

Note: 2. All voltages are referenced to GND.

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Conditions			min	max	Unit	Note
Operating current (average current during operation)	I_{CCA}	$t_{RC} = t_{RC}$ (min)	Cycle time	115 ns		80	mA	3, 4
				130 ns		70		
				160 ns		60		
Standby current 1	I_{CCS1}	$\overline{CE} = \overline{RFSH} = V_{IH}$	LC33864P, M			2	mA	
			LC33864PL, ML			1		
Standby current 2	I_{CCS2}	$\overline{CE} = \overline{RFSH} = V_{CC} - 0.2$ V	LC33864P, M			1	mA	
			LC33864PL, ML			100	µA	
Self-refresh current 1 (average current)	I_{CCF1}	$\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IL}$	LC33864P, M			2	mA	
			LC33864PL, ML			1		
Self-refresh current 2 (average current)	I_{CCF2}	$\overline{CE} = V_{CC} - 0.2$ V, $\overline{RFSH} = 0.2$ V	LC33864P, M			1	mA	
			LC33864PL, ML			100	µA	
Input leakage current	I_{IL}	0 V ≤ V_{IN} ≤ V_{CC}, pins other than measuring pin = 0 V			−10	+10	µA	
Output leakage current	I_{OL}	Output disable, 0 V ≤ V_{OUT} ≤ V_{CC}			−10	+10	µA	
Output high level voltage	V_{OH}	I_{OH} = −1 mA			2.4		V	
Output low level voltage	V_{OL}	I_{OL} = 2.1 mA				0.4	V	

Notes: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller. A bypass capacitor of 0.01 µF or larger should be inserted between VCC and GND for each memory chip to suppress power supply noise (voltage drops) due to transient currents.

4. Dependent on output load. Maximum value is value during free state.

Input/Output Capacitance at Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz

Parameter	Symbol	min	max	Unit
Input capacitance (A0 to A15)	C_{I1}		5	pF
Input capacitance ($\overline{CE}$, CS, $\overline{OE}$, $\overline{RFSH}$ and $\overline{WE}$)	C_{I2}		7	pF
I/O capacitance	C_{IO}		10	pF

Sampling inspections, and not full-lot inspections, are carried out for these parameters.

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10% (Notes 5, 6, 7, 8, 9.)

Parameter	Symbol	70 ns		80 ns		100 ns		Unit	Note
		min	max	min	max	min	max		
Random read or write cycle time	t_{RC}	115		130		160		ns	
Read-modify-write cycle time	t_{RMW}	165		195		235		ns	
$\overline{CE}$ pulse width	t_{CE}	70	10000	80	10000	100	10000	ns	
$\overline{CE}$ precharge time	t_P	35		40		50		ns	
$\overline{CE}$ access time	t_{CEA}		70		80		100	ns	
$\overline{OE}$ access time	t_{OEA}		30		35		40	ns	
$\overline{CE}$ output enable time	t_{CLZ}	20		25		30		ns	
$\overline{OE}$ output enable time	t_{OLZ}	0		0		0		ns	
$\overline{WE}$ output enable time	t_{WLZ}	0		0		0		ns	
$\overline{CE}$ output disable time	t_{CHZ}	0	20	0	25	0	30	ns	9
$\overline{OE}$ output disable time	t_{OHZ}	0	20	0	25	0	30	ns	9
$\overline{WE}$ output disable time	t_{WHZ}	0	20	0	25	0	30	ns	9
$\overline{OE}$ disable setup time	t_{ODS}	0		0		0		ns	
$\overline{OE}$ disable hold time	t_{ODH}	10		10		10		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
Chip select setup time	t_{CSS}	0		0		0		ns	
Chip select hold time	t_{CSH}	15		20		25		ns	
Write pulse width	t_{WP}	55		60		70		ns	
Write command hold time	t_{WCH}	55	10000	60	10000	70	10000	ns	
Write command lead time	t_{CWL}	55	10000	60	10000	70	10000	ns	
Input data setup time for $\overline{WE}$	t_{DSW}	30		35		40		ns	10
Input data setup time for $\overline{CE}$	t_{DSC}	30		35		40		ns	10

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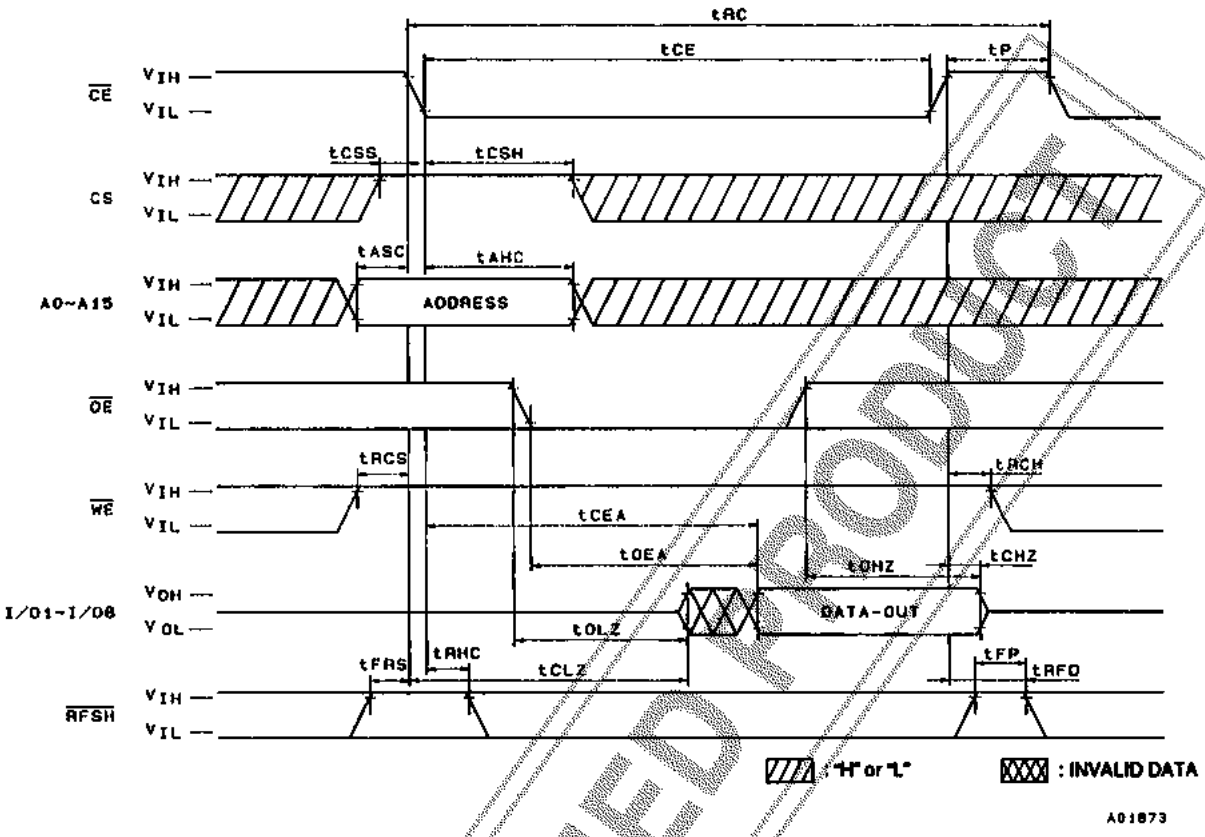
Parameter	Symbol	70 ns		80 ns		100 ns		Unit	Note
		min	max	min	max	min	max		
Input data hold time for $\overline{WE}$	t_{DHW}	0		0		0		ns	10
Input data hold time for $\overline{CE}$	t_{DHC}	0		0		0		ns	10
Address setup time for $\overline{CE}$	t_{ASC}	0		0		0		ns	11
Address hold time for $\overline{CE}$	t_{AHC}	15		20		25		ns	11
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto-refresh cycle time	t_{FC}	115		130		160		ns	
$\overline{RFSH}$ delay time for $\overline{CE}$	t_{RFD}	35		40		50		ns	
$\overline{RFSH}$ pulse width (auto-refresh)	t_{FAP}	35	8000	40	8000	50	8000	ns	12
$\overline{RFSH}$ precharge time (auto-refresh)	t_{FP}	30		30		30		ns	12
$\overline{RFSH}$ pulse width (self-refresh)	t_{FAS}	8000		8000		8000		ns	12
$\overline{RFSH}$ precharge $\overline{CE}$ delay time (self-refresh)	t_{FRS}	135		160		190		ns	12
Refresh time (512 cycles, A0 to A8)	t_{REF}		8		8		8	ms	
Rise or fall times	t_T	3	50	3	50	3	50	ns	

Note: 5. To accomplish internal initialization, $\overline{CE}$ is fixed at V_{IH} for an interval of 100 µs when V_{CC} reaches the specified voltage after power is switched on. At least eight cycles must be executed following that period.

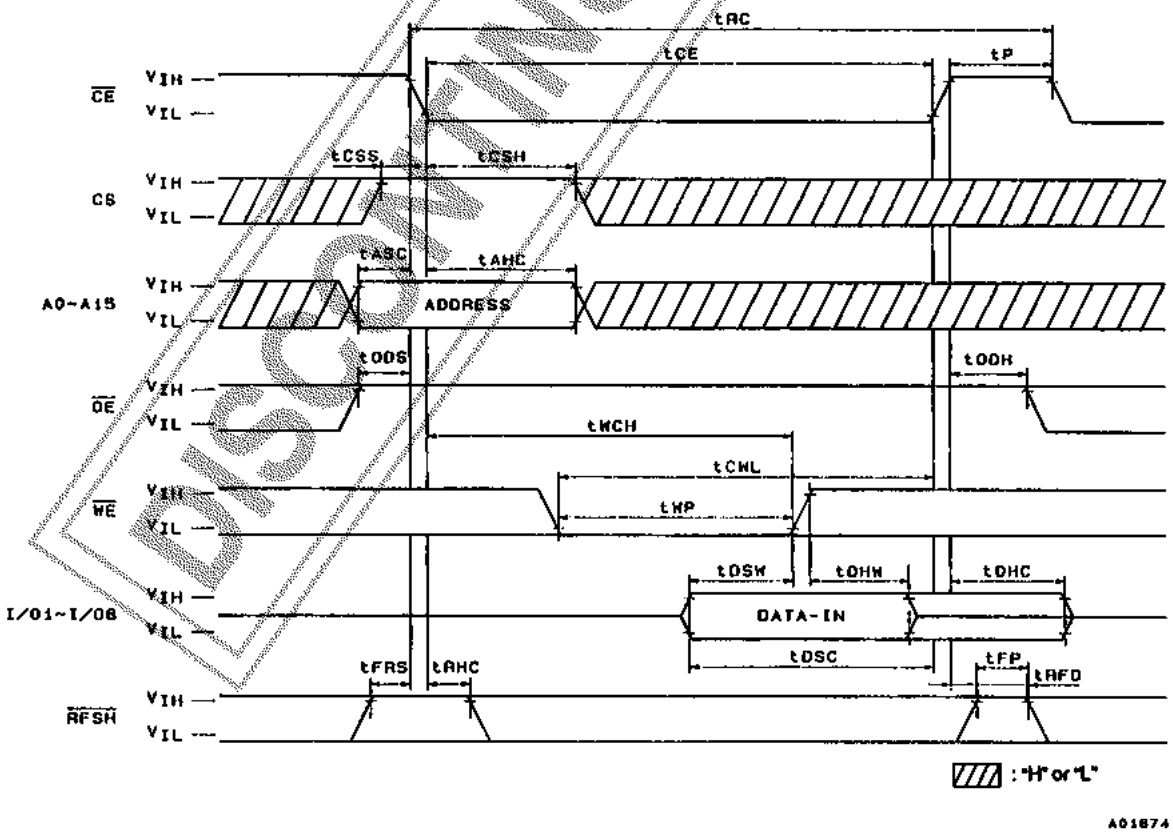
6. Measured at t_T = 5 ns.
7. When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are reference levels.
8. Measured using an equivalent of 100 pF and two standard TTL loads.
9. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time until output enters the open circuit state and the output voltage level becomes immeasurable.
10. As with ordinary static RAM, write data is incorporated at the rise of $\overline{WE}$ input or $\overline{CE}$ input, whichever is earlier, and write data is therefore held during t_{DSW}, t_{DSC}, t_{DHW}, or t_{DHC}.
11. Because address input is incorporated at the fall of $\overline{CE}$, the address is maintained during t_{ASC} or t_{AHC}.
12. Auto-refresh and self-refresh are determined by $\overline{RFSH}$ pulse width when $\overline{CE}$ = V_{IH}, and are defined as auto-refresh when below t_{FAP} (max), or as self-refresh when above t_{FAS} (min). In order to activate $\overline{CE}$ after the completion of each refresh, t_{FCE} must be assured for auto-refresh, or t_{FRS} must be assured for self-refresh.
Similarly, if self-refresh timing ($\overline{RFSH}$ = Low) is used after power is switched on, t_{FRS} must be assured.

Timing Chart

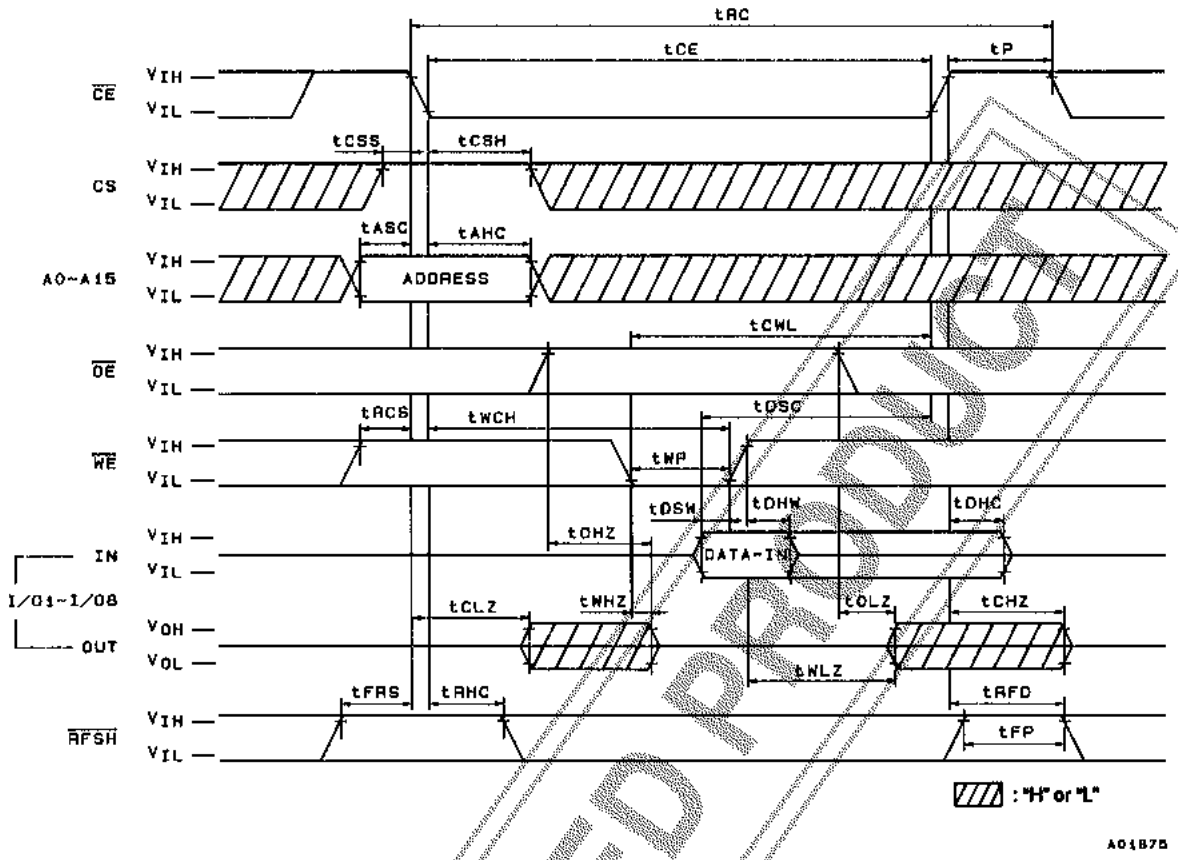
Read Cycle



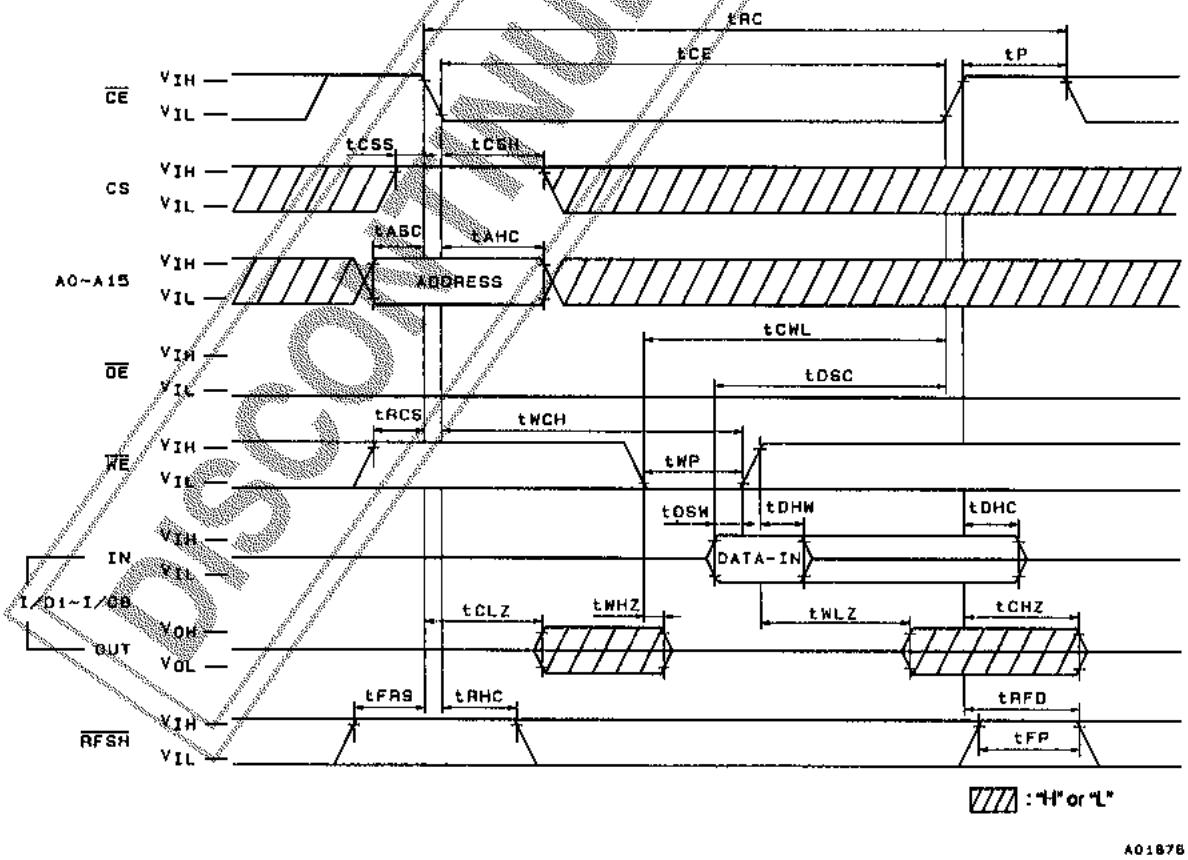
Write Cycle 1 ($\overline{OE}$ Fix High)



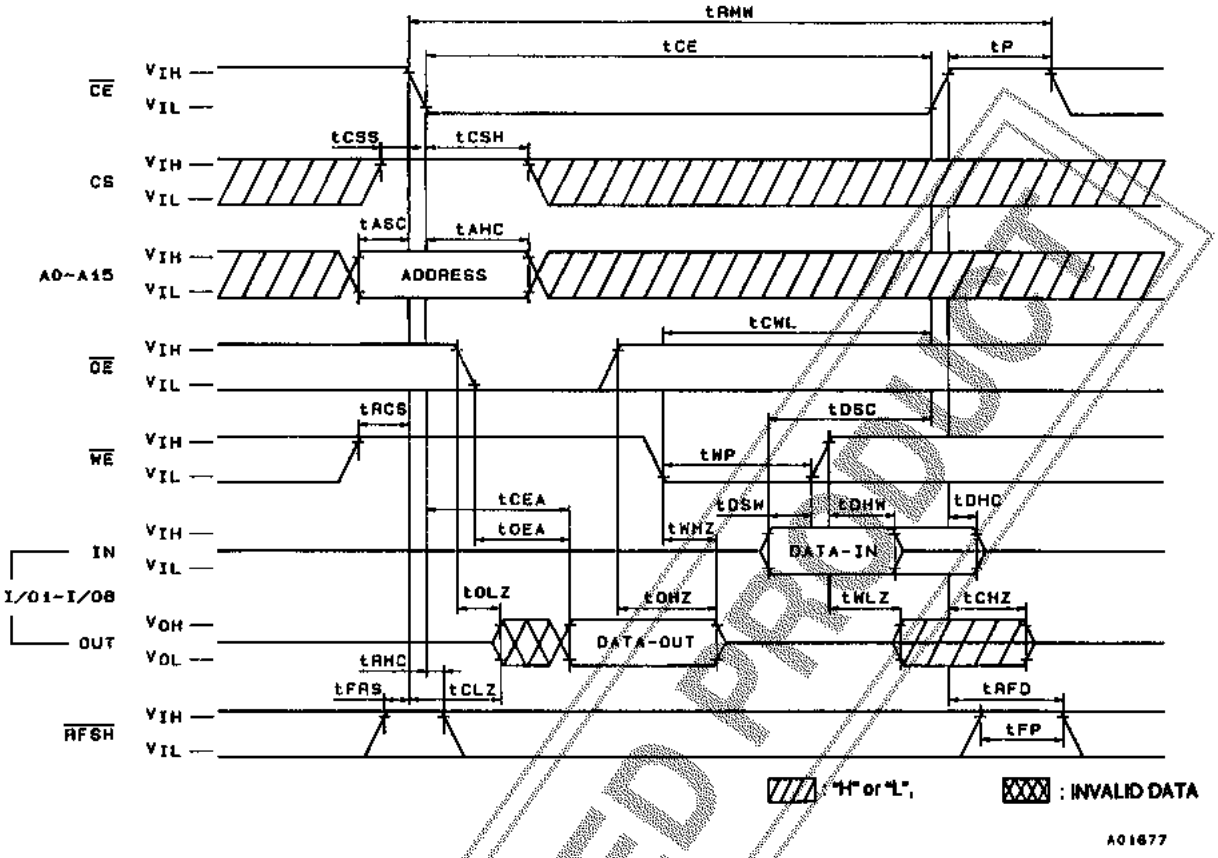
Write Cycle 2 ($\overline{OE}$ Clock)



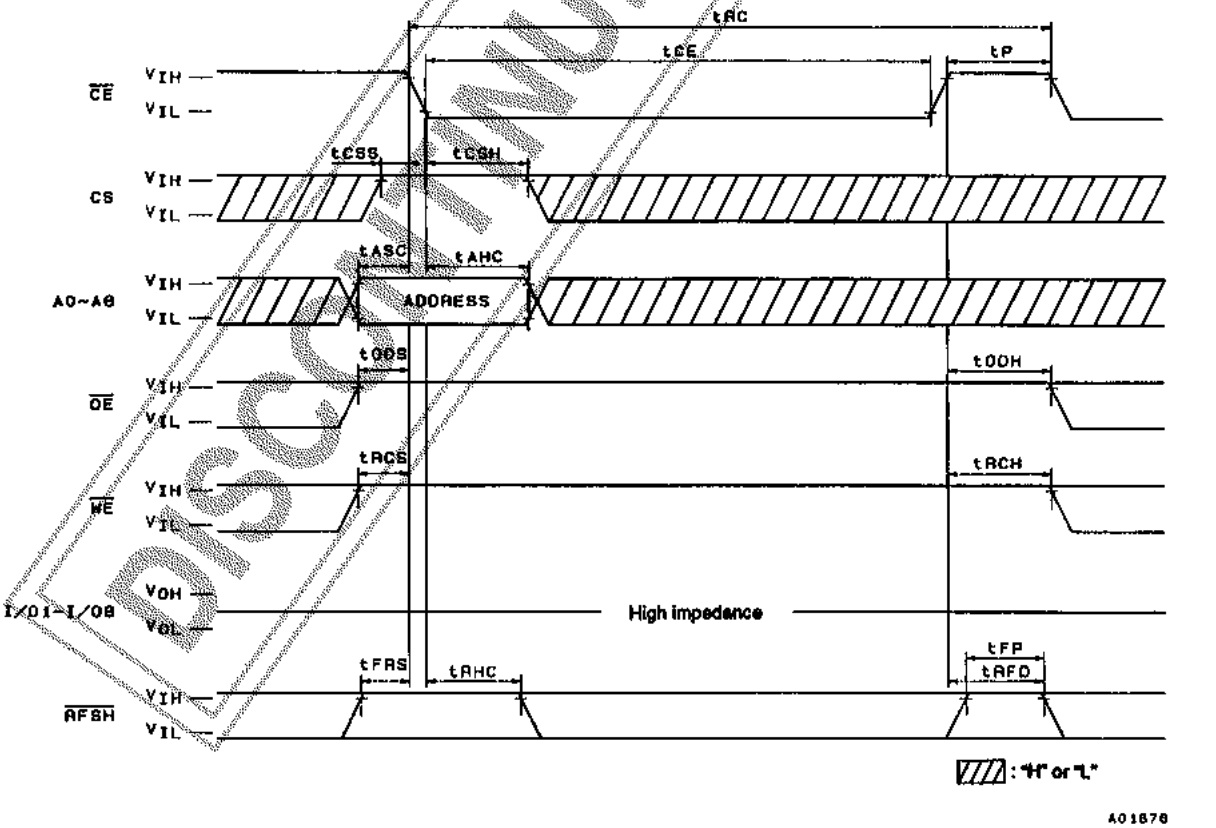
Write Cycle 3 ($\overline{OE}$ Fix Low)



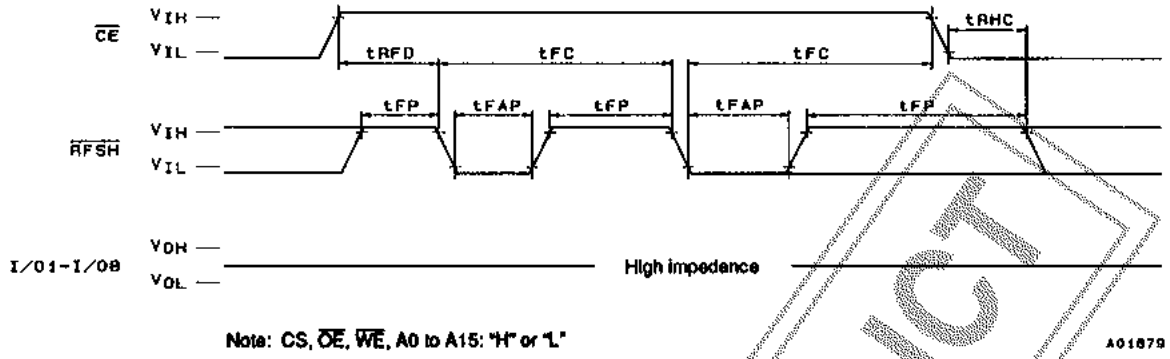
Read-Modify-Write Cycle



CE-Only Refresh



$\overline{RFSH}$ Auto-Refresh



Note: CS, $\overline{OE}$, $\overline{WE}$, A0 to A15: "H" or "L"

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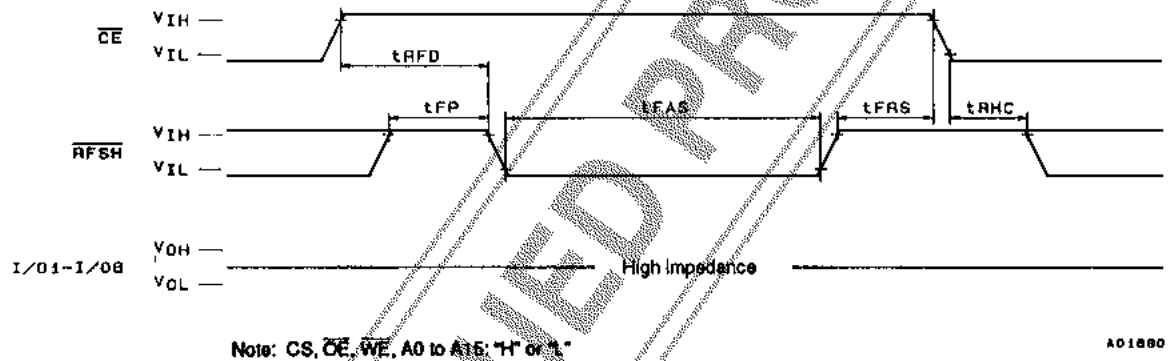
Self-Refresh



Note: CS, $\overline{OE}$, $\overline{WE}$, A0 to A15: "H" or "L"

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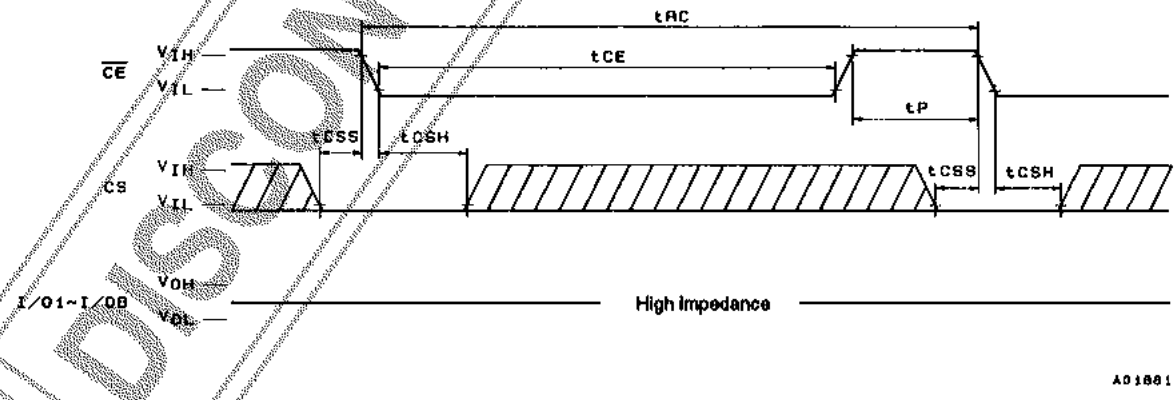
CS Standby Mode



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Note: $\overline{OE}$, $\overline{WE}$, A0 to A15: "H" or "L"

: "H" or "L"