

CDCVF857 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047A – MARCH 2003 – REVISED JUNE 2003

- **Recommended Applications:**
 - DDR Memory Modules (DDR400/333/266/200)
 - Zero Delay Fan-Out Buffer
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 220 MHz
- Low Jitter (Cycle-Cycle): ± 50 ps
- Low Static Phase Offset: ± 50 ps
- Low Jitter (Period): ± 35 ps
- 1 To 10 Differential Clock Distribution (SSTL2)
- Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low
- Operates From Dual 2.6-V Supplies
- Available in a 40-Pin MLF Package, 48-Pin TSSOP Package, or 56-Ball MicroStar Junior™ BGA Package
- Consumes $< 100\text{-}\mu\text{A}$ Quiescent Current
- External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks
- Meets/Exceeds JEDEC Standard (JESD82–1) For DDRI-200/266/333 Spec
- Meets/Exceeds Proposed DDRI-400 Spec (JESD82–1A)

description

The CDCVF857 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to 10 differential pairs of clock outputs (Y[0:9], $\overline{\text{Y}}[0:9]$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a $>20\text{-MHz}$ input signal, this detection circuit turns the PLL on and enables the outputs.

When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF857 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCVF857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF857 is characterized for both commercial and industrial temperature ranges.

AVAILABLE OPTIONS

T _A	TSSOP (DGG)	MicroStar Junior™ BGA (GQL)	40-Pin MLF
0°C to 85°C	CDCVF857DGG	CDCVF857GQL	CDCVF857RTB
–40°C to 85°C	CDCVF857IDGG	—	CDCVF857IRTB

FUNCTION TABLE (Select Functions)

INPUTS				OUTPUTS				PLL
AV _{DD}	$\overline{\text{PWRDWN}}$	CLK	$\overline{\text{CLK}}$	Y[0:9]	$\overline{\text{Y}}[0:9]$	FBOUT	$\overline{\text{FBOUT}}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off



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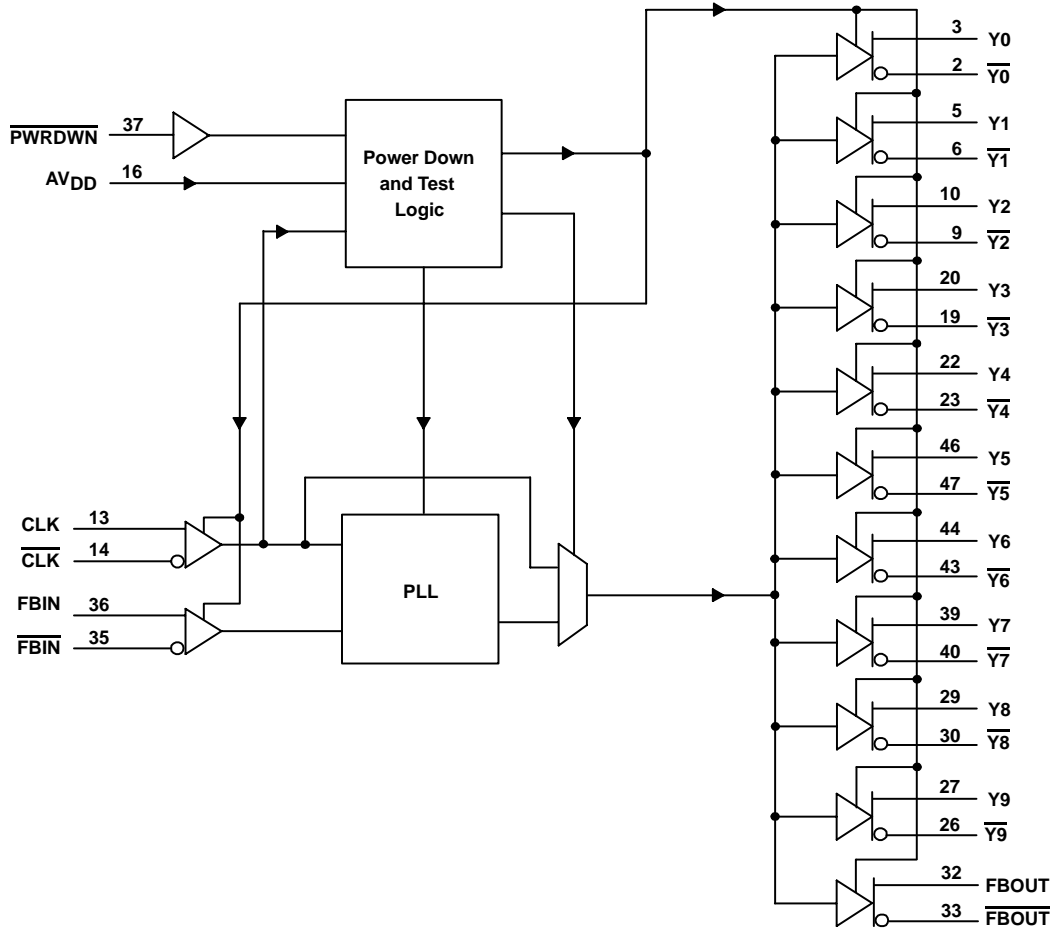
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functional block diagram



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CDCVF857

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Terminal Functions

NAME	TERMINAL				DESCRIPTION
	DGG	GQL	RTB		
AGND	17	H1	9		Ground for 2.5-V analog supply
AVDD	16	G2	8		2.5-V Analog supply
CLK, $\overline{\text{CLK}}$	13, 14	F1, F2	5, 6	I	Differential clock input
$\overline{\text{FBIN}}$, FBIN	35, 36	F5, F6	25, 26	I	Feedback differential clock input
FBOU $\overline{\text{T}}$, $\overline{\text{FBOU}}$	32, 33	H6, G5	21, 22	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4	1, 10		Ground
$\overline{\text{PWRDWN}}$	37	E6	27	I	Output enable for Y and $\overline{\text{Y}}$
VDDQ	4, 11, 12, 15, 21, 28, 34, 38, 45	B3, B4, E1, E2, E5, G1, G6, J3, J4	4, 7, 13, 18, 23, 24, 28, 33, 38		2.5-V Supply
Y0, $\overline{\text{Y0}}$	3, 2	A1, A2	37, 36	O	Buffered output copies of input clock, CLK, $\overline{\text{CLK}}$
Y1, $\overline{\text{Y1}}$	5, 6	B2, B1	39, 40	O	
Y2, $\overline{\text{Y2}}$	10, 9	D1, D2	3, 2	O	
Y3, $\overline{\text{Y3}}$	20, 19	J2, J1	12, 11	O	
Y4, $\overline{\text{Y4}}$	22, 23	K1, K2	14, 15	O	
Y5, $\overline{\text{Y5}}$	46, 47	A6, A5	34, 35	O	
Y6, $\overline{\text{Y6}}$	44, 43	B5, B6	32, 33	O	
Y7, $\overline{\text{Y7}}$	39, 40	D6, D5	29, 30	O	
Y8, $\overline{\text{Y8}}$	29, 30	J5, J6	19, 20	O	
Y9, $\overline{\text{Y9}}$	27, 26	K6, K5	17, 16	O	

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, VDDQ, AVDD	0.5 V to 3.6 V
Input voltage range, VI (see Notes 1 and 2)	-0.5 V to VDDQ + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	-0.5 V to VDDQ + 0.5 V
Input clamp current, IIK (VI < 0 or VI > VDDQ)	±50 mA
Output clamp current, IOK (VO < 0 or VO > VDDQ)	±50 mA
Continuous output current, IO (VO = 0 to VDDQ)	±50 mA
Continuous current to GND or VDDQ	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): GQL package	137.6°C/W
Storage temperature range Tstg	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

			MIN	TYP	MAX	UNIT
Supply voltage	V _{DDQ}	PC1600 – PC2700	2.3		2.7	V
		PC3200	2.5		2.7	
	AV _{DD}		V _{DDQ} – 0.12		2.7	
Low-level input voltage, V _{IL}	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$		V _{DDQ} /2 – 0.18			V
	PWRDWN		–0.3		0.7	
High-level input voltage, V _{IH}	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$		V _{DDQ} /2 + 0.18			V
	PWRDWN		1.7		V _{DDQ} + 0.3	
DC input signal voltage (see Note 5)			–0.3		V _{DDQ} + 0.3	V
Differential input signal voltage, V _{ID} (see Note 6)	dc	CLK, FBIN	0.36		V _{DDQ} + 0.6	V
	ac	CLK, FBIN	0.7		V _{DDQ} + 0.6	
Input differential pair cross voltage, V _{IX} (see Note 7)			V _{DDQ} /2 – 0.2		V _{DDQ} /2 + 0.2	V
High-level output current, I _{OH}					–12	mA
Low-level output current, I _{OL}					12	mA
Input slew rate, SR			1		4	V/ns
Operating free-air temperature, T _A	Commercial		0		85	°C
	Industrial		–40		85	

- NOTES: 4. The unused inputs must be held high or low to prevent them from floating.
 5. The dc input signal voltage specifies the allowable dc execution of the differential input.
 6. The differential input signal voltage specifies the differential voltage |V_{TR} – V_{CP}| required for switching, where V_{TR} is the true input level and V_{CP} is the complementary input level.
 7. The differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	Input voltage	All inputs	V _{DDQ} = 2.3 V, I _I = –18 mA				–1.2	V
V _{OH}	High-level output voltage		V _{DDQ} = min to max, I _{OH} = –1 mA		V _{DDQ} – 0.1			V
			V _{DDQ} = 2.3 V, I _{OH} = –12 mA		1.7			
V _{OL}	Low-level output voltage		V _{DDQ} = min to max, I _{OL} = 1 mA		0.1			V
			V _{DDQ} = 2.3 V, I _{OL} = 12 mA		0.6			
V _{OD}	Output voltage swing‡		Differential outputs are terminated with 120 Ω /CL = 14 pF (See Figure 3)		1.1		V _{DDQ} – 0.4	V
V _{OX}	Output differential cross-voltage§		V _{DDQ} /2 – 0.15	V _{DDQ} /2	V _{DDQ} /2 + 0.15			
I _I	Input current		V _{DDQ} = 2.7 V, V _I = 0 V to 2.7 V				±10	μA
I _{OZ}	High-impedance state output current		V _{DDQ} = 2.7 V, V _O = V _{DDQ} or GND				±10	μA
I _{DDPD}	Power-down current on V _{DDQ} + AV _{DD}		CLK and $\overline{\text{CLK}}$ = 0 MHz; PWRDWN = Low; Σ of I _{DD} and A _{DD}			20	100	μA
A _{DD}	Supply current on AV _{DD}		f _O = 170 MHz			7	10	mA
			f _O = 200 MHz			9	12	
C _I	Input capacitance		V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND		2	2.5	3.5	pF

† All typical values are at a respective nominal V_{DDQ}.

‡ The differential output signal voltage specifies the differential voltage |V_{TR} – V_{CP}|, where V_{TR} is the true output level and V_{CP} is the complementary output level.

§ The differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing. The frequency range is 100 MHz to 200 MHz.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I _{DD}	Dynamic current on V _{DDQ}	Without load	f _O = 170 MHz	100	110	mA
			f _O = 200 MHz	105	120	
		Differential outputs terminated with 120 Ω/CL = 0 pF	f _O = 170 MHz	200	240	
			f _O = 200 MHz	210	250	
		Differential outputs terminated with 120 Ω/CL = 14 pF	f _O = 170 MHz	260	300	
			f _O = 200 MHz	280	320	
ΔC	Part-to-part input capacitance variation	V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND			1	pF
C _{I(Δ)}	Input capacitance difference between CLK and CLKB, FBIN, and FBINB	V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND			0.25	pF
C _O	Output capacitance	V _{DDQ} = 2.5 V, V _O = V _{DDQ} or GND	2.5	3	3.5	pF

† All typical values are at a respective nominal V_{DDQ}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f _{CLK}	Operating clock frequency	60	220	MHz
	Application clock frequency	90	220	
Input clock duty cycle		40%	60%	
Stabilization time† (PLL mode)			10	μs
Stabilization time‡ (Bypass mode)			30	ns

† The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V_{DD} must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

‡ A recovery time is required when the device goes from power-down mode into bypass mode (AVDD at GND).

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} §	Low to high level propagation delay time	Test mode/CLK to any output		3.5		ns
t _{PHL} §	High-to low level propagation delay time	Test mode/CLK to any output		3.5		ns
t _{jit(per)} ¶	Jitter (period), See Figure 7	66 MHz	-60		60	ps
		100/133/167/200 MHz	-35		35	ps
t _{jit(cc)} ¶	Jitter (cycle-to-cycle), See Figure 4	66 MHz	-75		75	ps
		100/133/167/200 MHz	-50		50	ps
t _{jit(hper)} ¶	Half-period jitter, See Figure 8	66 MHz	-100		100	ps
		100/133/167/200 MHz	-75		75	ps
t _{slr(o)}	Output clock slew rate, See Figure 9	Load: 120 Ω/14 pF	1		2	V/ns
t(∅)	Static phase offset, See Figure 5	66 MHz	-100		100	ps
		100/133/167/200 MHz	-50		50	ps
tsk(o)	Output skew, See Figure 6	Load: 120 Ω/14 pF	100/133/167 MHz		100	ps
			200 MHz		75	
t _r , t _f	Output rise and fall times (20% – 80%)	Load: 120 Ω/14 pF	600		900	ps

§ Refers to the transition of the noninverting output.

¶ This parameter is assured by design but can not be 100% production tested.

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PARAMETER MEASUREMENT INFORMATION

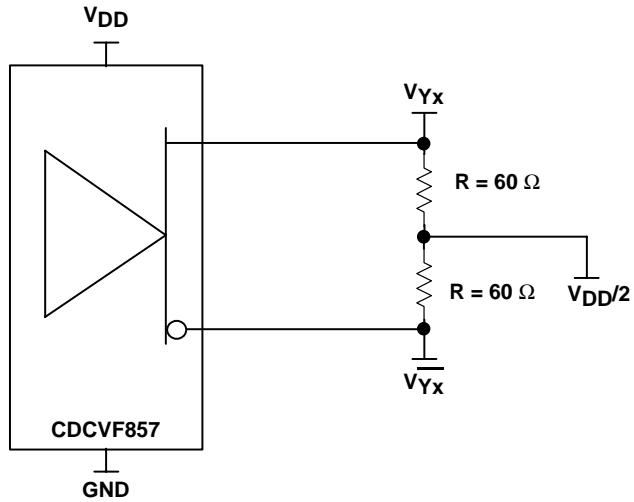


Figure 1. IBIS Model Output Load

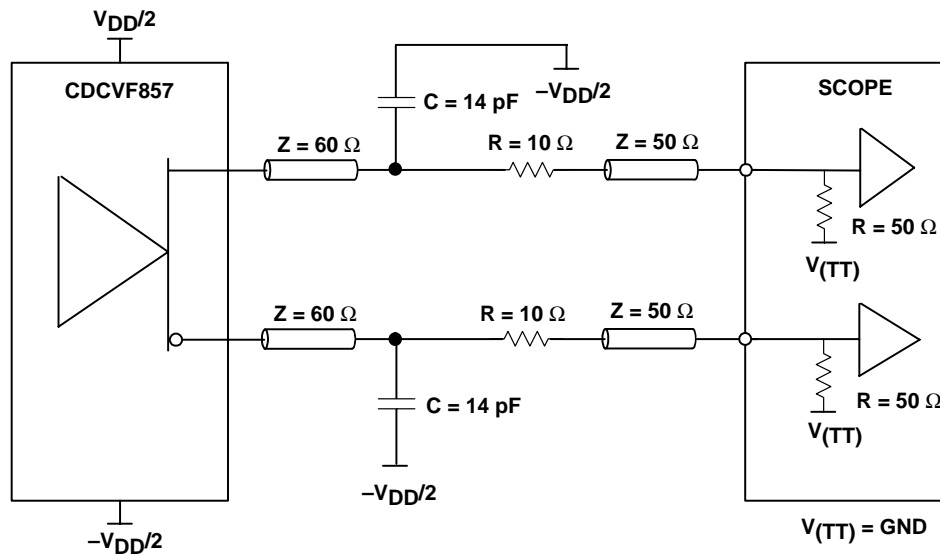


Figure 2. Output Load Test Circuit

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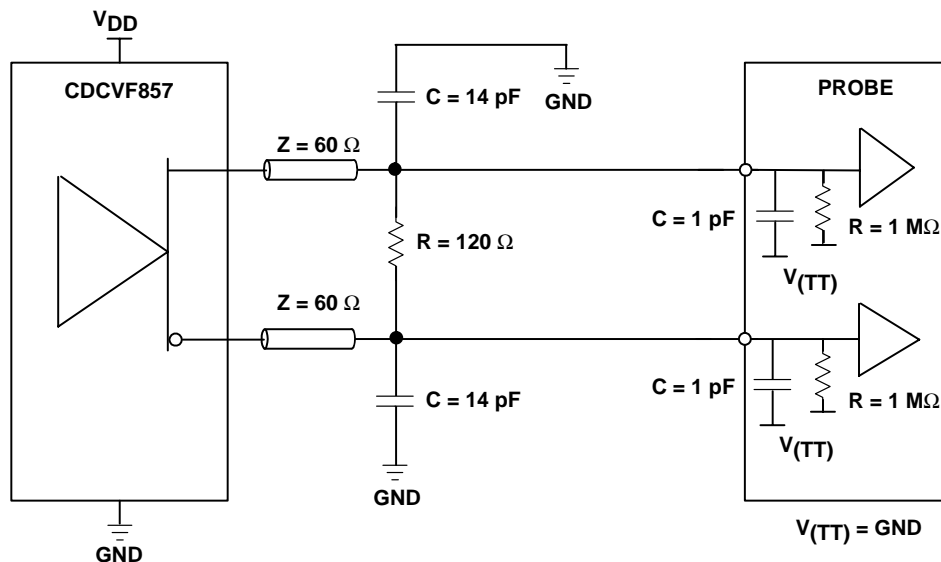


Figure 3. Output Load Test Circuit for Crossing Point

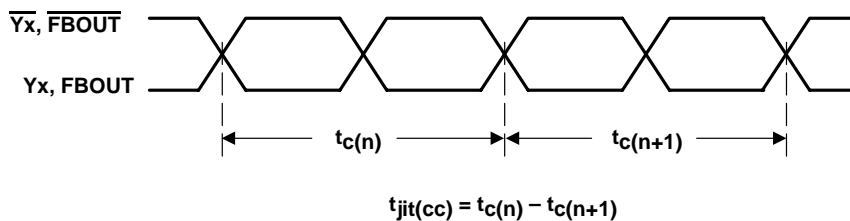


Figure 4. Cycle-to-Cycle Jitter

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PARAMETER MEASUREMENT INFORMATION

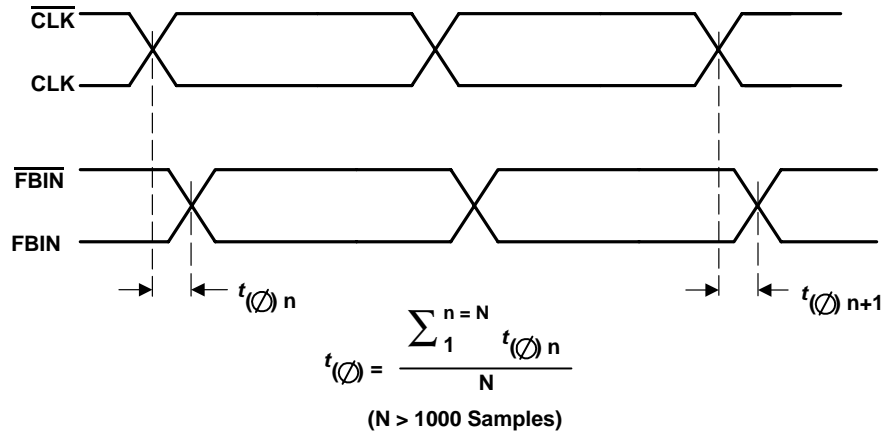


Figure 5. Phase Offset

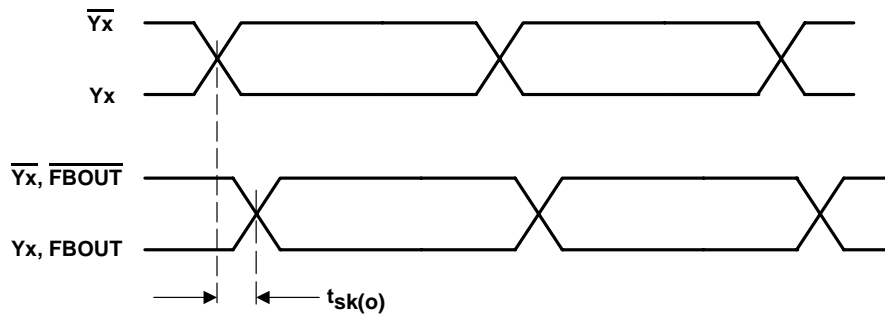


Figure 6. Output Skew

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PARAMETER MEASUREMENT INFORMATION

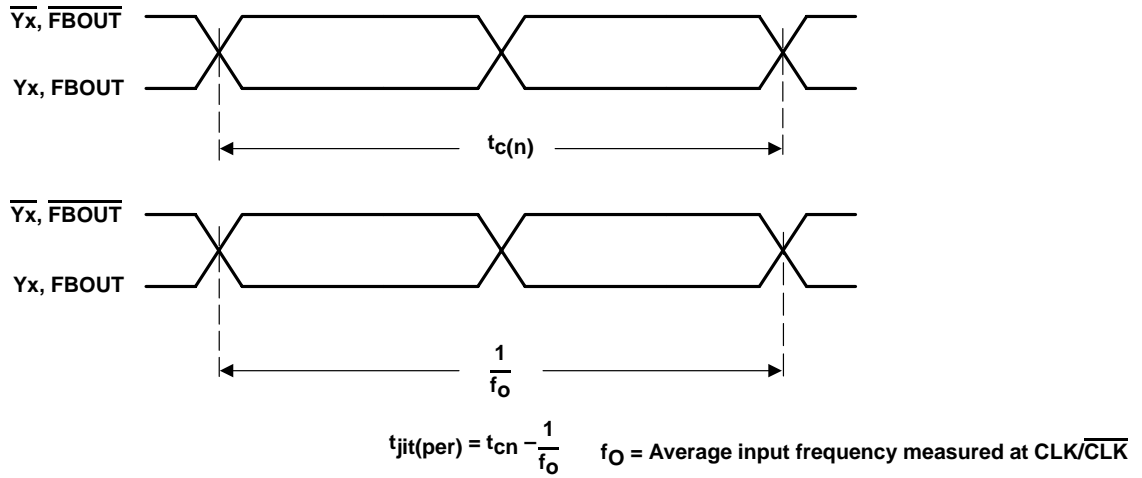


Figure 7. Period Jitter

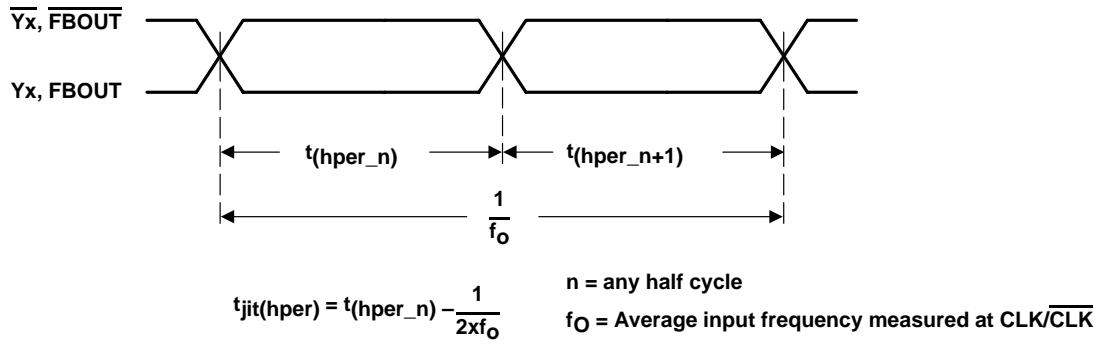


Figure 8. Half-Period Jitter

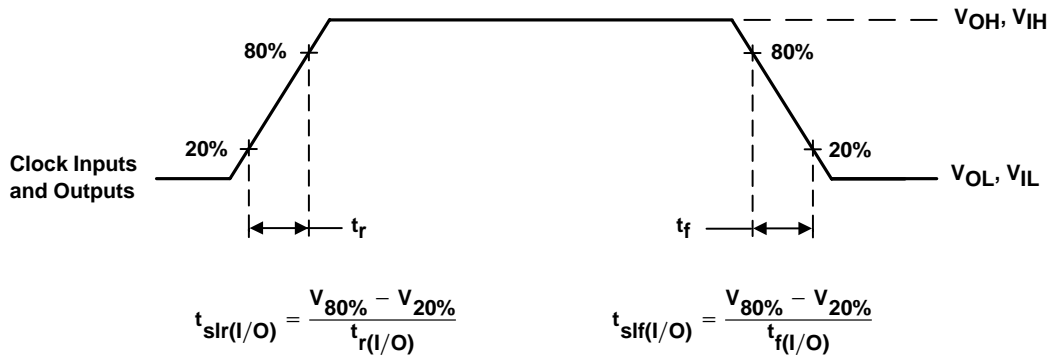


Figure 9. Input and Output Slew Rates

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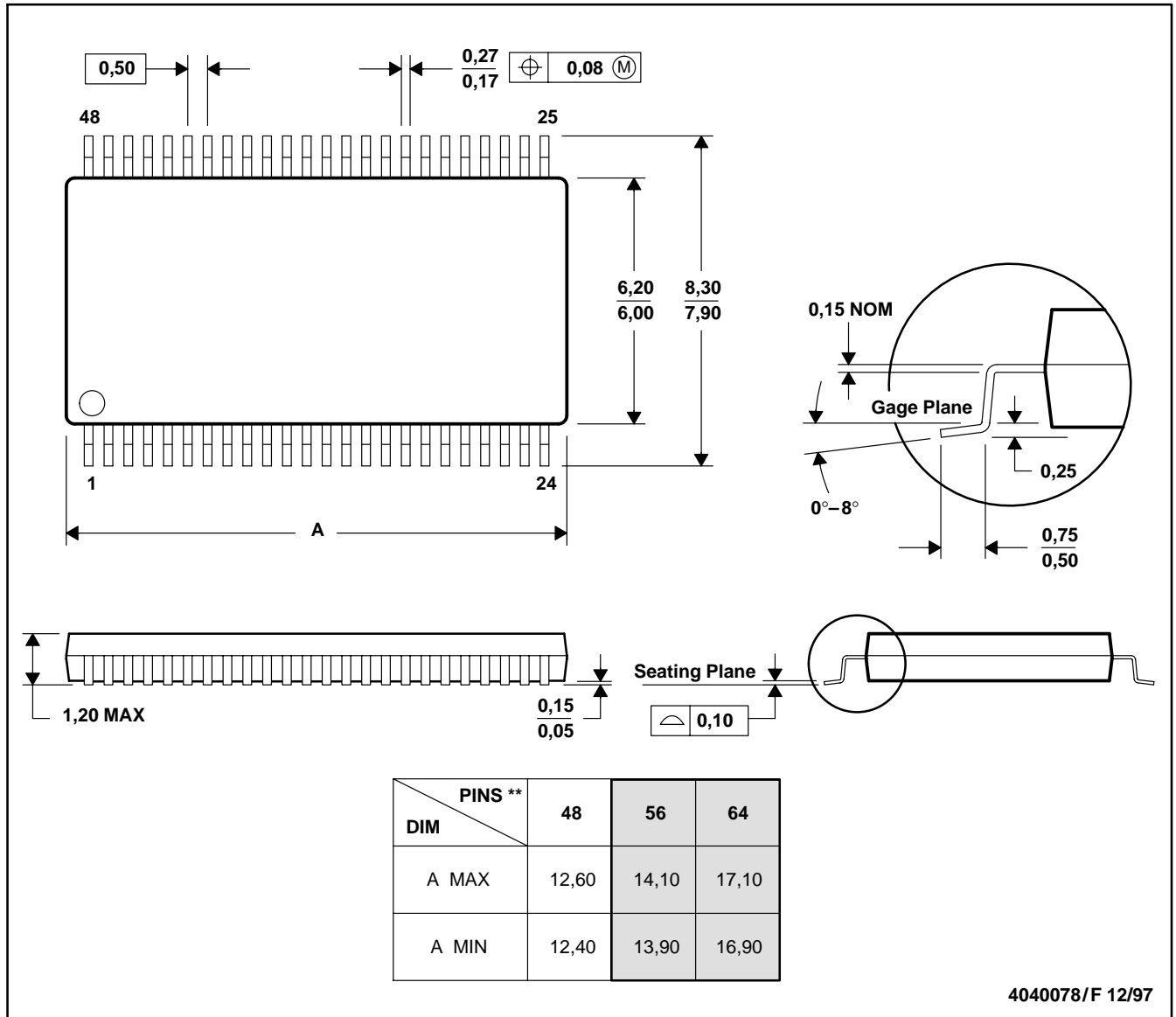


MECHANICAL DATA

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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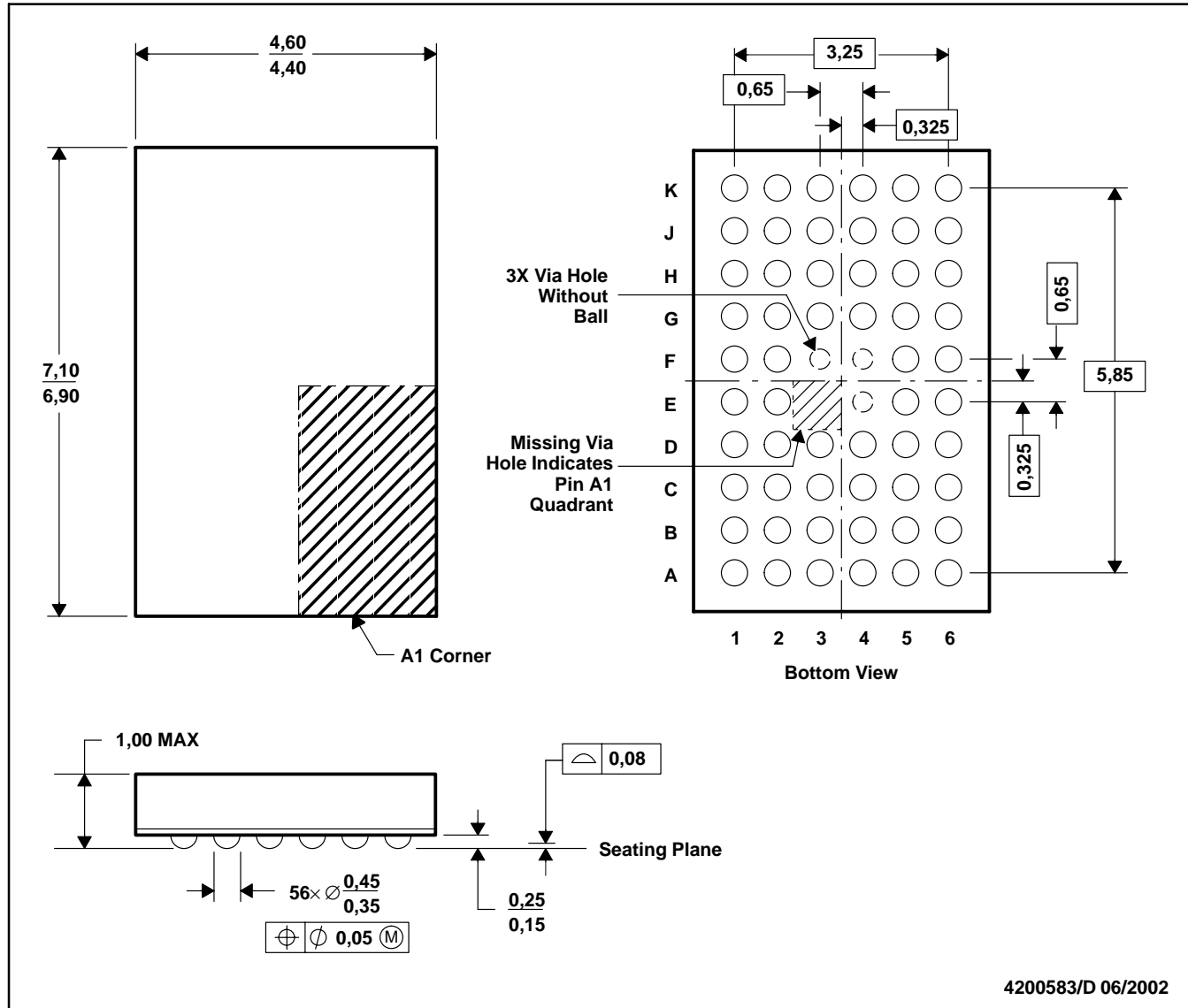
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MECHANICAL DATA

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. MicroStar Junior™ BGA configuration
 D. Falls within JEDEC MO-225 variation BA.
 E. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

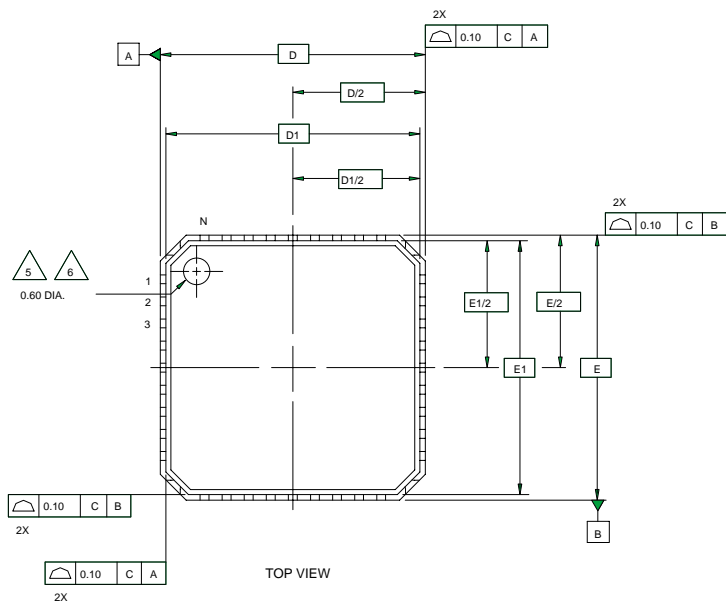
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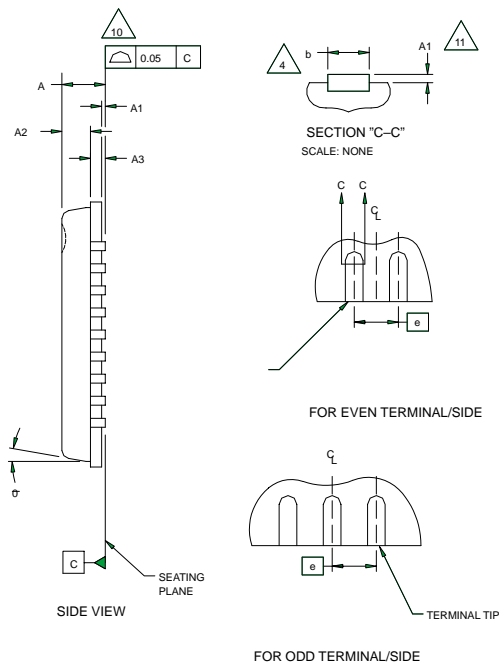
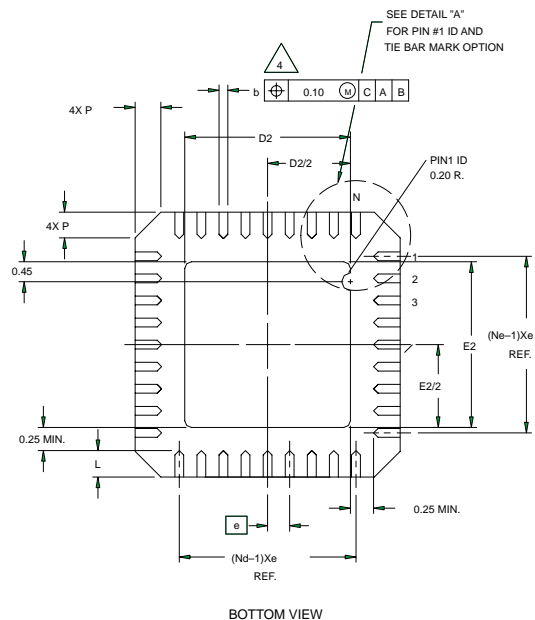
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MECHANICAL DATA

RTB (MLF2-N40)



HIGH-DENSITY MATRIX LEADFRAME



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	—	0.85	0.90	
A1	0.00	0.01	0.05	D
A2	—	0.65	0.80	
A3	0.20 REF.			
D	6.00 BSC			
D1	5.75 BSC			
E	6.00 BSC			
E1	5.75 BSC			
θ	12			
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	C

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	40			A
Nd	10			A
Ne	10			A
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	B
Q	0.00	0.20	0.45	C
D2	2.75	2.90	3.05	
E2	2.75	2.90	3.05	

- NOTES:
- A. N is the number of terminals
 - B. Dimension b applies to the plated terminal and is measured
 - C. Q and R apply only for the straight tiebar shapes.
 - D. Applied only for terminals
 - E. 40-pin HP-VFQFP-N, 6.0 × 6.0 mm body size, 0.5-mm pitch, variation VJJD-2, E2 & D2 = 2.9 mm ±0.15 mm

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