Preliminary

MB85101

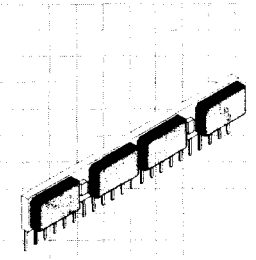
FUJITSU

MB85101A-10, MB85101A-12, MB85101A-15
MOS 65,536 x 4-Bit Dynamic RAM Module

Description

The Fujitsu MB85101A is a 64K x 4 dynamic RAM high density memory module. It consists of four MB8264A DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

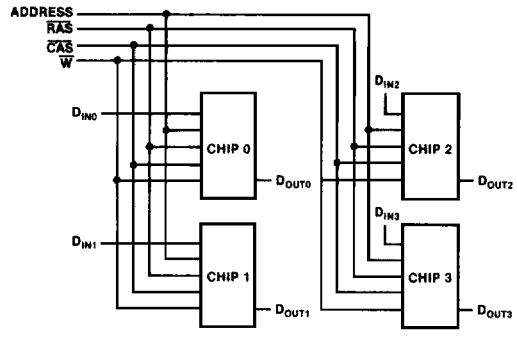
The MB85101A is intended for use in memory applications in which large amounts of memory are required in a compact space or in which board space is limited. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desktop computers and peripheral storage.

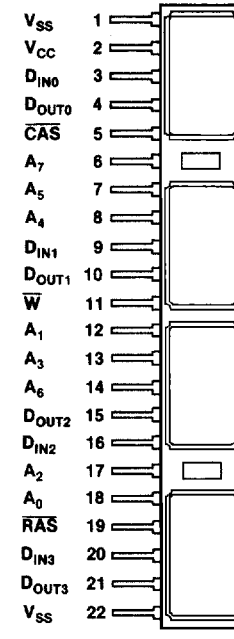


Features

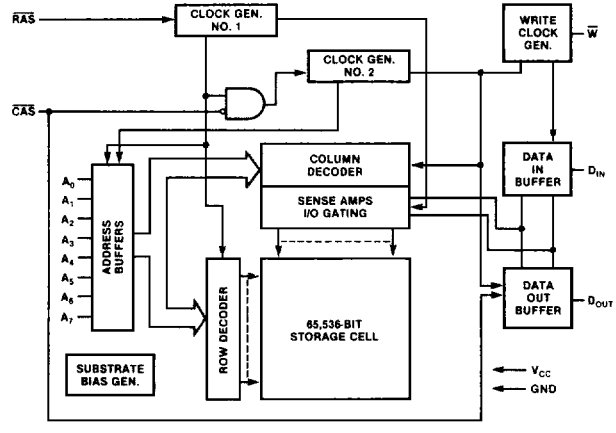
- 65,536 x 4-bit DRAM module
- Row Access Time
  - 100 ns max. (MB85101A-10)
  - 120 ns max. (MB85101A-12)
  - 150 ns max. (MB85101A-15)
- Cycle Time
  - 200 ns min. (MB85101A-10)
  - 230 ns min. (MB85101A-12)
  - 260 ns min. (MB85101A-15)
- Single +5 V supply, ±10% tolerance
- Low power (active)
  - 1100 mW max. (MB85101A-10)
  - 990 mW max. (MB85101A-12)
  - 880 mW max. (MB85101A-15)
  - 88 mW max. (standby)
- 2 ms/128 cycle refresh
- $\overline{RAS}$-only and Hidden refresh capability
- Read-Modify-Write and Page Mode capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows extended page boundary and two dimentional chip selects.
- On-chip latches for Addresses and Data-in

MB85101 Block Diagram and Pin Assignment





Block Diagram for Each Chip



Package Dimensions
Dimensions in inches (millimeters)

22-Lead Single In-Line Package
(Module MDL-22S-CC01)