GBL GigaBit Logic

16G020

T-43-25

Programmable Single Gate GaAs D-MESFET Array

FEATURES

- 11 single gate depletion MESFETs on each chip
- f_t = 22 GHz typical frequency response
- -0.9 V pinchoff voltage, 35 mA I_{DSS} (typ.)
- Excellent thermal and electrical matching
- Very low capacitance
- Available with personalized interconnects in the package for design integration and improved performance
- Available in leadless chip carrier (LCC), flatpack or die form

APPLICATIONS

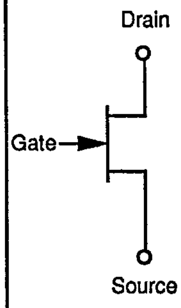
- Low noise amplifiers (broadband, video, IF, RF, or microwave)
- Interface circuitry to digital logic
- Ultra low capacitance buffers
- RF or high-speed current source/Active load
- Analog switches
- Switch drivers
- Laser drivers
- Source-follower line drivers (digital or analog)
- Differential amplifiers/current-steering circuits

FUNCTIONAL DESCRIPTION

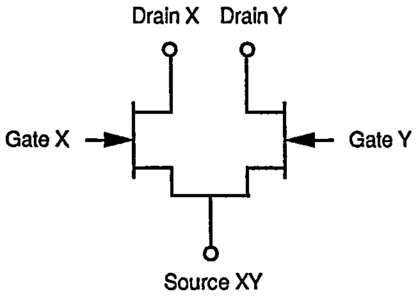
The 16G020 contains 11 single gate GaAs depletion mode MESFETs on a single chip. The device characteristics of these N-channel, Schottky-gate D-MESFETs are similar to those of silicon N-channel JFETs. Typical gate voltage ranges between Vgs =-0.9V (threshold of drain conduction) to Vgs = +0.6 V (onset of strong gate forward conduction current). The device structure is symmetrical, allowing interchange of source and drain electrodes. Electrically, the source is defined as the more negative of these two electrodes. To reduce Miller capacitance (Cgd), the source electrode is defined as the pad immediately adjacent to the gate bonding pad, since this will have slightly more parasitic capacitance than to the second pad over, identified as the drain. One pair of MESFETs has a common source for use as a differential pair. 16G020 MESFETs feature a -0.9V pinchoff voltage and very low junction capacitance, making them ideal for high frequency applications utilizing relatively small signal levels in both digital and analog circuits. In order to take better advantage of the high frequency characteristics of the FETs in the 16G020, GigaBit offers the option to interconnect FETs and add chip components as necessary inside the package (LCC or Flatpack). Package parasitic capacitance and inductance generally limits the performance of packaged parts. By realizing the interconnects inside the package to form a personalized analog function, the overall effect of package parasitic impedance is reduced since there is less I/O per function.

CIRCUIT DIAGRAMS

SINGLE
GATE D-MESFETS
(9 per chip)



SINGLE GATE D-MESFETS
DIFFERENTIAL PAIR
(1 per chip)



ORDERING INFORMATION

PACKAGE TYPE	PART NUMBER
36 I/O Leadless CC	16G020-L36
36 I/O Flatpack	16G020-F
Die	16G020-X

16G020 FET ARRAY PERSONALIZATION

Please contact factory for special part number.

GBL GigaBit Logic **16G020**

T-43-25

CIRCUIT DESIGN INTEGRATION USING PERSONALIZED 16G020

GigaBit Logic can integrate certain analog designs by utilizing the 11 single gate MESFETs in the 16G020. Chip resistors and capacitors can also be added in the package cavity to realize more complex circuits. By interconnecting 16G020 FETs inside the package, GigaBit can offer personalized analog functions with better performance than when the interconnects are external. First, the effect of package and wire bond parasitic capacitance and inductance is reduced since there are fewer I/O per function. Chip capacitors and resistors can be attached close to the die bond pads in order to minimize wire bond length. Second, since there are fewer overall I/O per package, it is possible to adopt a Ground-Signal-Ground approach for the pin-out. This lowers cross capacitance between adjacent pins reducing cross talk as well as potential jitter in the circuit.

PROGRAM FLOW FOR PROTOTYPES

GigaBit will review or propose a circuit schematic to personalize the 16G020 to the desired function. Prototypes are custom wire-bonded during assembly. Chip resistors and capacitors are added in the package as necessary. This approach has two main advantages: no Non-Recurring Engineering Expenses (N.R.E.) and a quick turnaround time (2 to 4 weeks). Since there is no NRE, designers have total flexibility to try out a design and modify it if necessary.

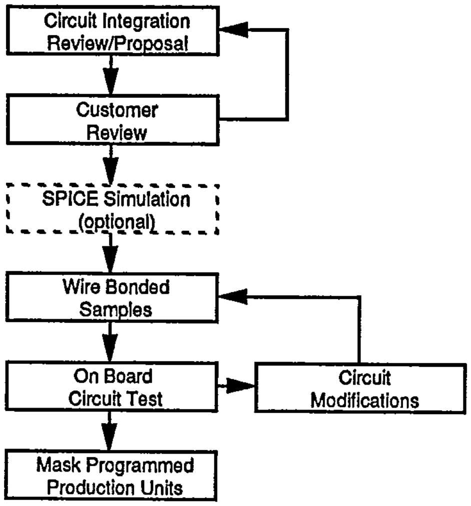
GigaBit can provide, as an option, complete simulation of the circuit utilizing its proprietary spice model.

PROGRAM FLOW FOR PRODUCTION DEVICES

Production devices are customized via mask programming. The interconnects are realized in the IC substrate by changing the top metal layer mask of the 16G020.

Mask programming for production devices is advised to improve reliability and reproducibility compared with wire bonded prototypes. In addition, mask programmed ICs require less assembly work and are lower in cost compared with wire bonded prototypes.

DESIGN INTEGRATION PROGRAM FLOW

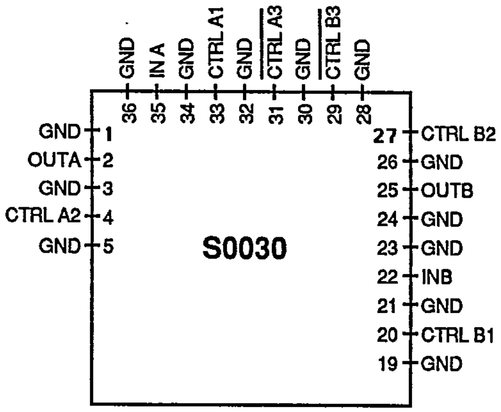


EXAMPLES

Some examples of analog ICs developed using the 16G020 FET arrays are:

- Dual high isolation analog switch with 0.5 ns switching time and 80 dB isolation at 1 GHz (S0030)
- Switch driver/high speed driver with 9V/ns output slew rate
- Octal GaAs to TTL translator

Dual Analog Switch S0030



GBL GigaBit Logic

16G020

T-43-25

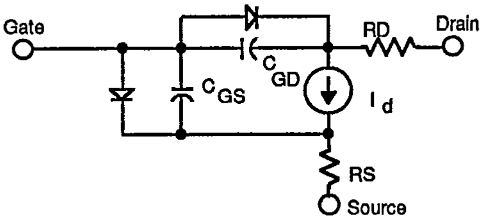
ABSOLUTE MAXIMUM RATINGS
(Beyond which useful life may be impaired)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
V_{DS}	Drain to Source Voltage	15V
V_{GS}	Gate to Source Voltage	-10V
V_{GD}	Gate to Drain Voltage	- 10V
V_{ISOL}	Isolation Voltage Between FETs	50V
I_G	Gate Forward Biased Current	15 mA
I_D, I_S	Continuous Drain/Source Current	50mA
I_D, I_S	Pulsed Drain/Source Current	100mA
P_D	Total Power Dissipation – Per Chip – Per FET	1.5W 400mW
T_{STOR}	Storage Temperature	- 60°C to + 150°C

SPICE PARAMETERS

The following parameters may be used as a first order approximation with the Berkeley Spice Version 2 G JFET, Model. All parameters are normalized to 1µm FET width. For the16G020 FETs: W = 400µm.

FET EQUIVALENT CIRCUIT



SYMBOL	PARAMETER	VALUE	UNITS
VTO	Pinchoff Voltage	-0.90	V
BETA	Gain Coefficient	1.48×10^{-4}	$A/V^2 \times \mu m$
LAMBDA	DC Drain Cond. Coefficient (Note1)	0.05	V^{-1}
RS	Source Resistance	1055	$\Omega \times \mu m$
RD	Drain Resistance	1055	$\Omega \times \mu m$
CGS	Gate-Source Capacitance (Note 2)	1.3×10^{-15}	F/µm
CGD	Drain-Gate Capacitance (Note 2)	0.62×10^{-15}	F/µm
IS	Gate Diode Saturation Current	2×10^{-14}	A/µm
PB	Barrier Height For Capacitance [C(V)]	0.85	V

Notes :
1. Varies Substantially from dc (typically LAMBDA = 0.023 V^{-1}) to ac operating frequencies (typically LAMBDA = 0.13 V^{-1} for f > 100 KHz).
2. The SPICE JFET model assumes $C_{gs} = W \times CGS / \sqrt{1-(V_g - V_s)/PB}$, $C_{gd} = W \times CGD / \sqrt{1+(V_d - V_g)/PB}$ which ignores the fact that both Cgs and Cgd are functions of both Vgs and Vdg. Values calculated for CGS and CGD give average capacitances under typical switching conditions.

GBL GigaBit Logic

16G020

T-43-25

16G020L, 16G020F
ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_P	Pinchoff Voltage	V_{DS} = 2.5V	-0.7	-0.9	-1.1	V
I_{DSS}	Saturation Current	V_{DS} = 2.5V, V_{GS} = 0V	23	32	50	mA
C_{gs}	Gate -- Source Capacitance (Die) (Note 3)	V_{DS} = 2.5V, V_{GS} = 0V		0.5		pF
C_{gd}	Gate - Drain Capacitance (Die) (Note 3)	V_{DS} = 2.5V, V_{GS} = 0V		0.05		pF
C_{ds}	Drain -- Source Capacitance (Die) (Note 3)	V_{DS} = 2.5V, V_{GS} = 0V		0.1		pF
g_m	Transconductance	V_{DS} = 2.5V, V_{GS} = 0V	45	63	80	mS
ΔV_P	Pinchoff Voltage Match (Between any FET and the average pinchoff voltage of the chip)	V_{DS} = 2.5V		30		mV
Δg_m	Transconductance Match (Between any FET and the average transconductance of the chip)	V_{DS} = 2.5V, V_{GS} = 0V		5		mS
R_{on}	Drain-Source On Resistance	V_{GS} = 0.6V V_{GS} = 0V		10 16	20	Ω Ω
R_s	Source Resistance	I_G = 0.8mA		3		Ω
g_{os}	Common Source Output Conductance (Note 2)	V_{DS} = 2.5V, V_{GS} = 0V f > 10 MHz		4.5		mS
V_{BRDS}	Drain-Source Breakdown Voltage (Note 4)	V_{GS} = -1.5V, $I_D \leq$ 0.5mA	9	11		V
V_{BRGS}	Gate-Source Breakdown Voltage	I_D = .1mA		8		V
I_D	Drain Leakage Current	V_{DS} = 2.5V, V_{GS} = - 2.5V		500		nA
I_G	Gate Leakage Current	V_{DS} = 2.5V, V_{GS} = -2.5V		100		nA
F_t	Unity Gain Frequency (Die)	V_{DS} = 2.5V, V_{GS} = 0V		22		GHz
N_F	Optimum Noise Figure	V_{DS} = 2.5V, V_{GS} = -0.3V f0 = 1 GHz f0 = 2 GHz f0 = 4 GHz		 .45 .85 1.65		 dB dB dB

NOTES:
1. Test conditions, unless otherwise stated: TA = 25°C
2. At frequencies below the 10 KHz to 1 MHz range, the common source output conductance is typically at least an order of magnitude lower than the high frequency value given above.
3. For packaged parts, the measured capacitances will be increased by both shunt capacitance (C1G from each pin to ground) and interelectrode capacitance (C12, between adjacent pins). For the flatpack (assuming 0.150" external leads), the shunt capacitance is C1G = 0.25 pf and the interelectrode contribution is C12 = 0.20 pf. In addition, each lead has a series inductance of about 7nH in the flatpack (including the 0.150" Leads). For the leadless chip carrier package these values are C1G = 0.5 pf shunt and C12 = 0.1 pf, with a series inductance of 4nH on each lead. The shunt capacitances are principally to the ground pin on the package, which should be connected to an AC ground to minimize high frequency crosstalk between FETs.
4. Operation at drain to source voltages above VBRDS may involve some degradation in output conductance (gos) and some increase in noise (particularly flicker or "popcorn" noise). These factors should not interfere with switching applications at higher VDS voltage levels.

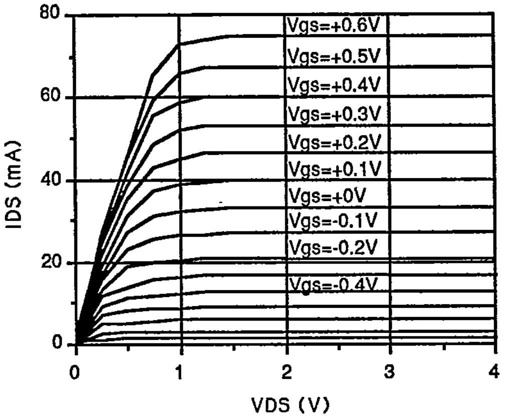
T-43-25

GBL GigaBit Logic

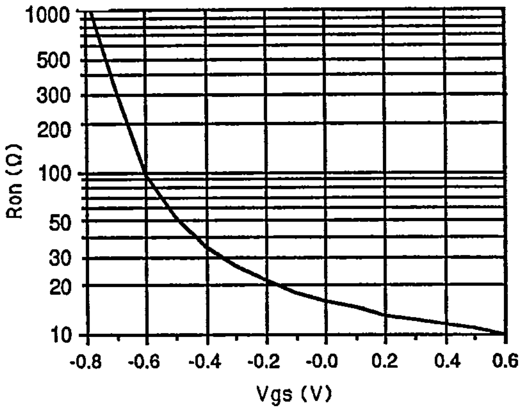
16G020

DEVICE CHARACTERISTICS (Ta = 25°C)

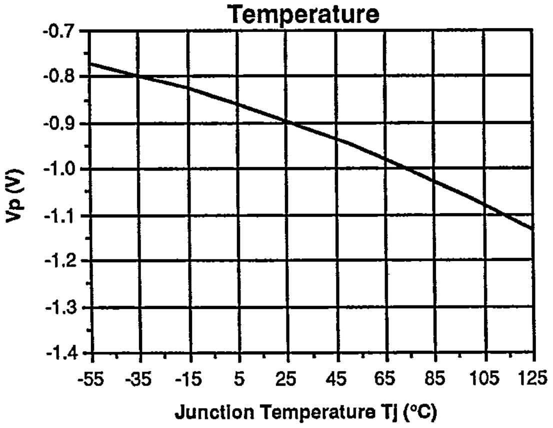
IDS vs. VDS



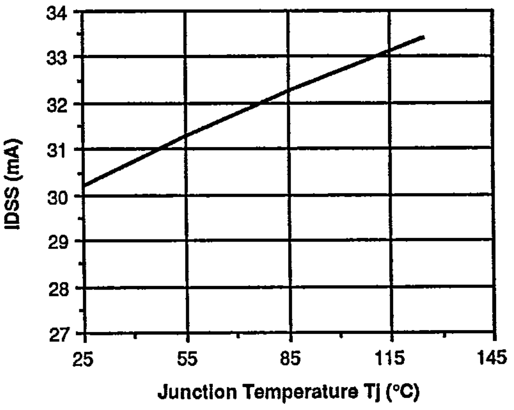
"ON" RESISTANCE VS. VGS



Pinchoff Voltage vs. Temperature



IDSS vs. Temperature



T-43-25

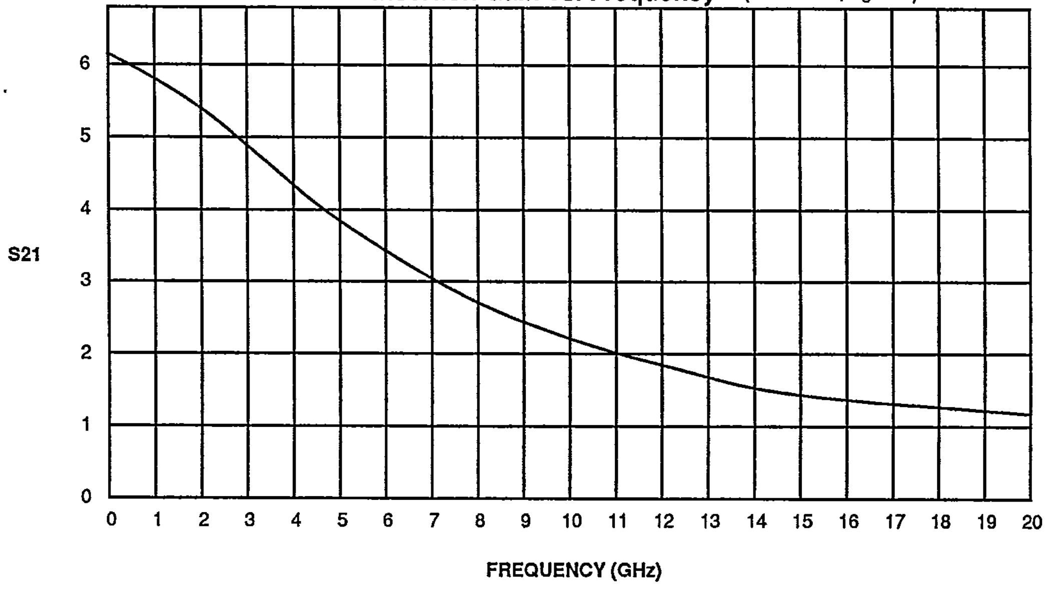
GBL GigaBit Logic

16G020

TYPICAL S-PARAMETERS (Vds=2.5V, Vgs=0V)

Frequency (MHz)	S11		S21		S12		S22	
	MAG	PHASE	MAG	PHASE	MAG	PHASE	MAG	PHASE
100	.99	-2.6	6.1	178	0.004	8.9	0.56	-1.77
1000	.99	-25.4	5.92	164	0.037	7.5	0.55	-17.4
2000	.97	-48.3	5.46	150	0.068	6.2	0.52	-33.2
2800	.95	-64.6	4.99	140	0.088	5.2	0.497	-44.4
4000	.92	-83	4.33	129	0.11	4.2	0.46	-57.4
5000	.90	-96	3.80	120	0.12	3.4	0.44	-66.6
7000	.88	-115	2.99	108	0.13	2.3	0.41	-80
10000	.86	-130	2.24	95.8	0.14	1.3	0.4	-92
12500	.85	-140	1.81	87.6	0.142	0.5	0.41	-99
16000	.85	-147	1.45	79.1	0.142	-3.8	0.44	-105
18000	.85	-150	1.28	74	0.141	-3.1	0.46	-109
20000	.85	-153	1.14	70	0.14	-6.2	0.48	-111

Insertion Gain vs. Frequency (Vds = 2.5V, Vgs = 0)



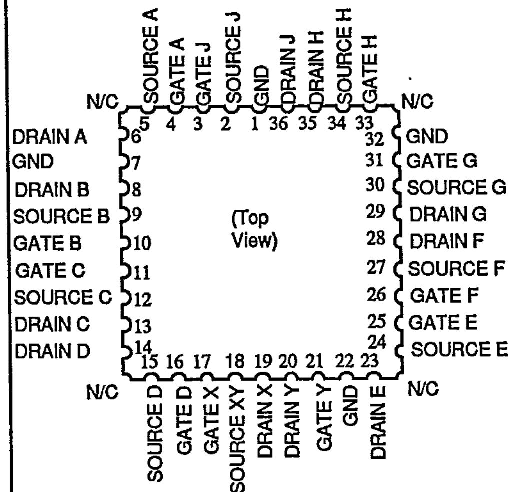
T-43-25

GBL GigaBit Logic

16G020

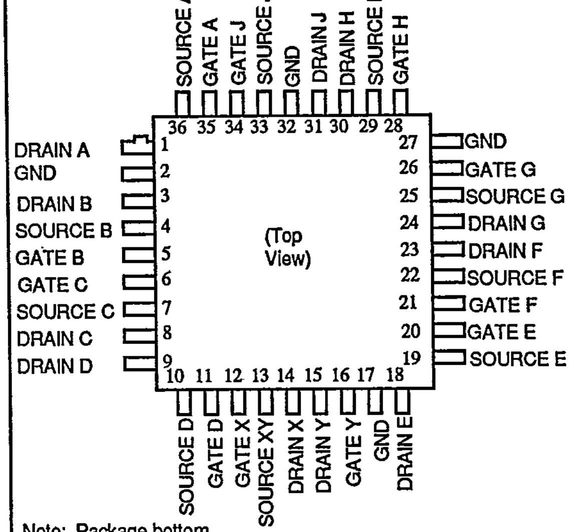
PACKAGE PINOUT DIAGRAM

36 I/O LEADLESS CHIP CARRIER
16G020-L36



Note: Pins 1,7,22 and 32 are internally connected.

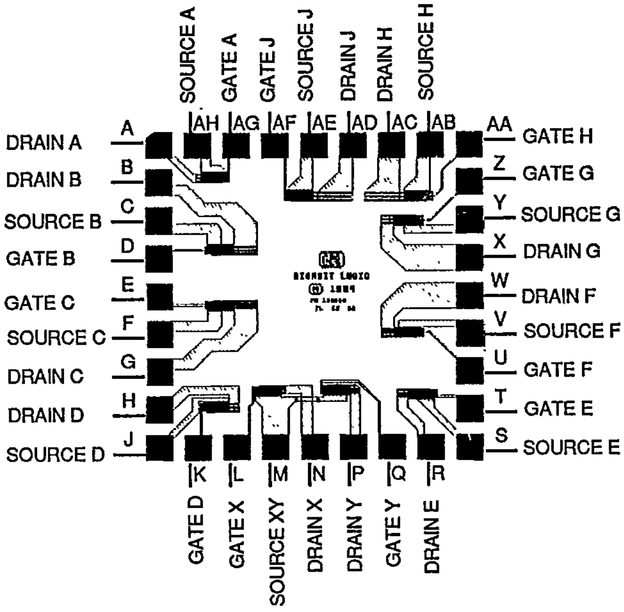
36 LEAD FLATPACK
16G020-F



Note: Package bottom surface and pins 2, 17, 27 and 32 are internally connected.

METALLIZATION AND PAD LAYOUT

16G020-X



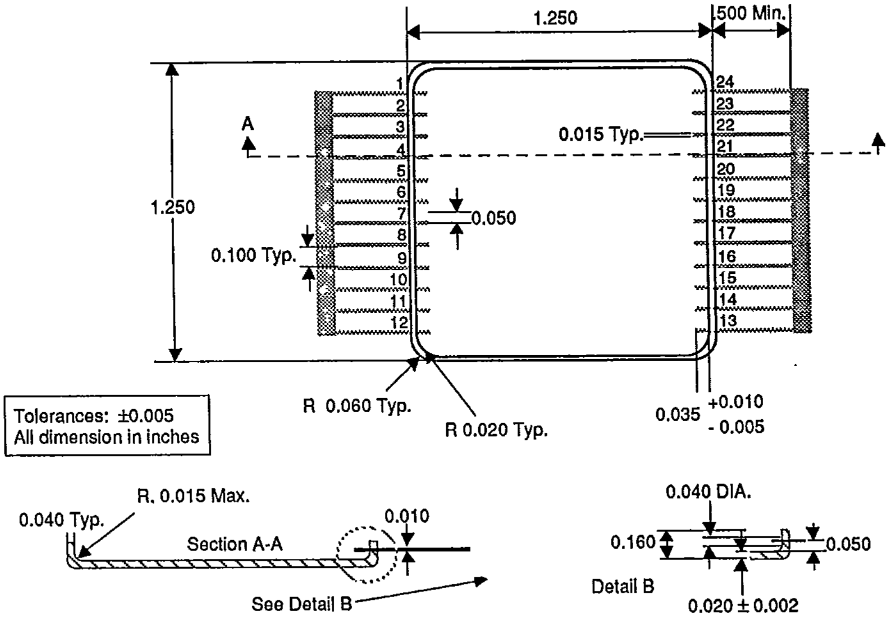
GBL GigaBit Logic

24 PIN HYBRID
18 PIN PACKAGE

T-90-20

24 PIN HYBRID PACKAGE

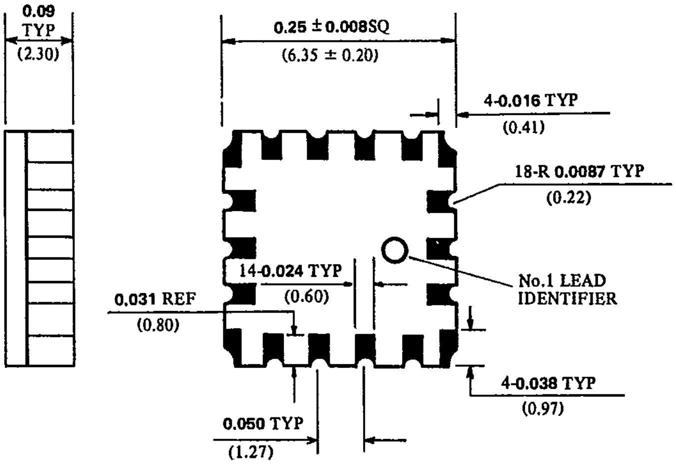
Type H



Tolerances: ±0.005
All dimension in inches

18 PIN LEADLESS CHIP CARRIER

TYPE L1



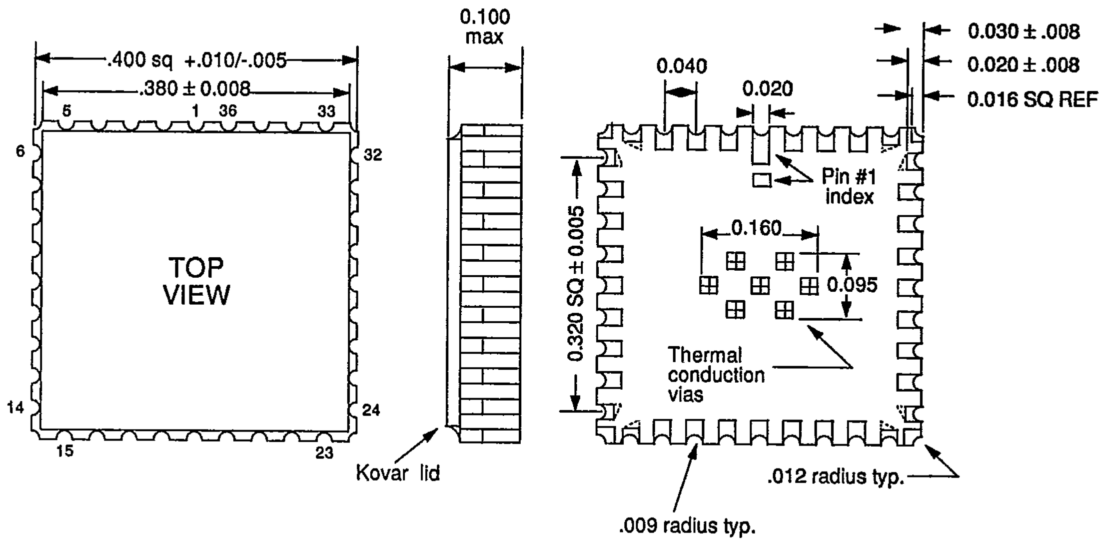
All dimensions shown in inches and (millimeters)

T-90-20

36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER

TYPE L36

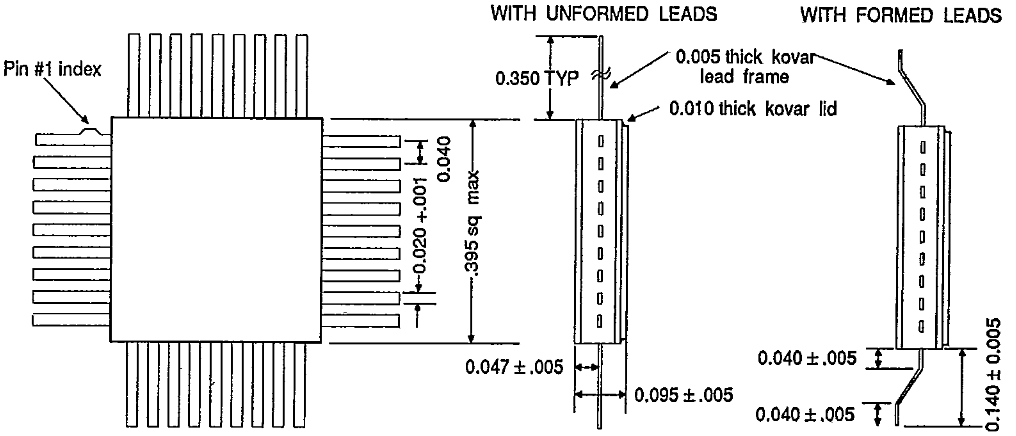


NOTES:

1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK

TYPE F

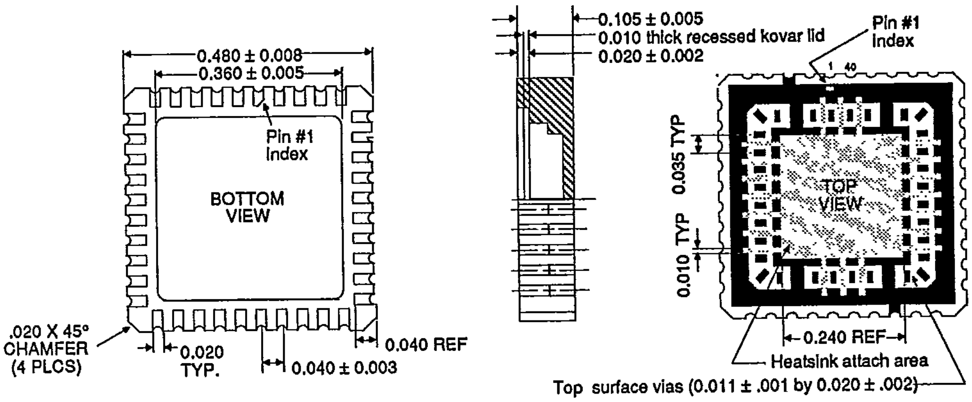


T-90-20

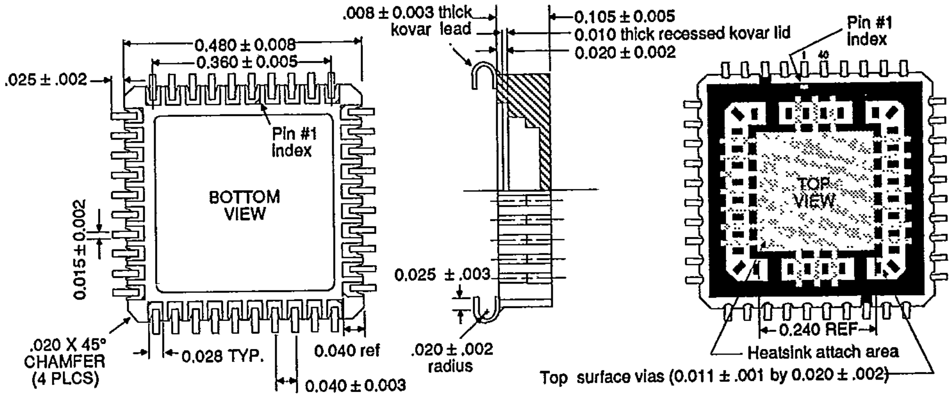
GBL GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

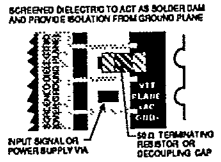


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0 010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:	
Metalized Ceramic......	■
Screened Dielectric.....	▨
Bare Ceramic.............	☐

Top Surface Terminating/Decoupling Detail

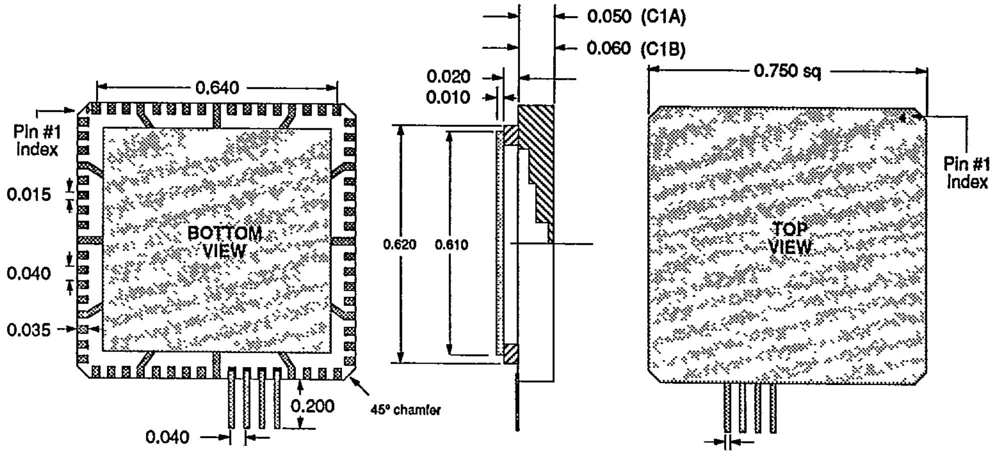


GBL GigaBit Logic

68 & 132 PIN PACKAGES

T-90-20

68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3