SPT8120

16-bit, 20 MSPS, CMOS A/D Converter

Features

- 16-bit, 20 MSPS CMOS analog-to-digital converter
- Excellent performance:
  DLE: -0.5/+1.2 LSB, ILE: ±4 LSB
  SFDR = 89dB @ f_{IN} = 5MHz
- Guaranteed no missing codes
- Internal sample-and-hold and voltage reference
- Internal digital calibration
- Power dissipation: 800mW at 20 MSPS
- +5V analog supply and +3.3/5V digital output supply
- Out-of-range indicator
- 64-pin leadless plastic chip carrier (LPCC) package
- -40˚C to +85˚C temperature range

Applications

- Wireless communications
- IR imaging
- Scanners and digital copiers
- High-end CCD cameras
- Medical imaging
- Automatic test equipment
- Data acquisition systems
- Lab and test equipment

Description

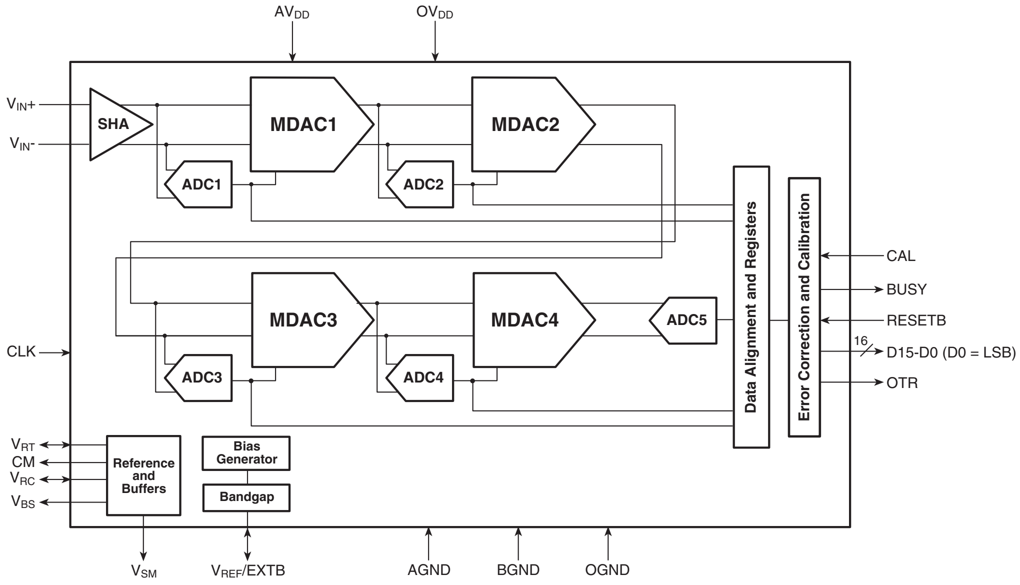
This high-performance, 16-bit analog-to-digital converter operates at a sample rate of up to 20 MSPS. It utilizes a digitally calibrated, pipelined CMOS architecture to achieve excellent dynamic performance and linearity. Incorporated on chip are a high-performance sample-and-hold amplifier and internal reference for minimal external circuitry.

The excellent linearity and superb dynamic performance of this device make it ideal for image processing and instrumentation applications, as well as communications applications.

The device operates from a single +5V supply. A separate digital output supply pin is provided for +3/5V logic output levels. Total power dissipation, including internal reference, is 800mW. It is in a 64-pin leadless plastic chip carrier (LPCC) package over the industrial temperature range of -40˚C to +85˚C.

Preliminary Data

Block Diagram



Preliminary Data

Absolute Maximum Ratings (beyond which damage may occur)[1] 25°C

Parameter	Min.	Max.	Unit
Supply Voltages			
AV_{DD}		+6	V
OV_{DD}		+6	V
Input Voltages			
Analog Inputs	-0.3	AV_{DD} +0.3	V
CLK Input	-0.3	AV_{DD} +0.3	V
Digital Inputs	-0.3	AV_{DD} +0.3	V
Digital Outputs			
Output Current	-10	+10	mA
Temperature			
Operating Temperature	-40	+85	°C
Junction Temperature		+175	°C
Lead Temperature (soldering 10 seconds)		+300	°C
Storage Temperature	-65	+150	°C

Note:

1. Operation at any absolute maximum rating is not implied.
   See Electrical Specifications table for proper nominal applied conditions in typical applications.

Electrical Specifications

(T_A = 25°C, AV_{DD} = +5V, OV_{DD} = 3.3V, f_S = 20 MSPS, internal references, unless otherwise noted)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Unit
Resolution				16		Bits
DC Performance						
Differential Linearity Error (DLE)		V		-0.5/+1.2		LSB
Integral Linearity Error (ILE)		V		±4		LSB
No Missing Codes				Guaranteed		
Offset (Mid Scale) Error		V		±0.02		%FS
Gain Error	External V_{RT} & V_{RC}	V		±0.15		%FS
Offset Error Temperature Drift[1]	-40°C to +85°C	V		±2.4		ppm FS/°C
Gain Error Temperature Drift	External V_{RT} & V_{RC} -40°C to +85°C	V		±3.5		ppm FS/°C
Analog Input						
Input Voltage Range[2]: V_{IN}+, V_{IN}-		V		±1		V
Input Capacitance		V		10		pF
Input Bandwidth (Full Power)		V		82		MHz
Timing Characteristics						
Conversion Rate		V		20	25	MSPS
Pipeline Delay (Latency)		V		16.5		CLK Cycles
Clock Duty Cycle		V	40	50	60	%
Clock Period (t_{CLK})		V		50		ns
Output Delay (t_{OD})	C_L = 3.5pF	V		TBD		ns

Notes:

1. After one-time calibration at 25˚C.
2. Each of V_{IN}+ and V_{IN}- ranges from +1.25V to +3.25V, making the span of differential input, (V_{IN}+) – (V_{IN}-), to be -2.0V to +2.0V.
3. Advanced Data describes products that are in the definition stage at the time of printing. Specifications are based on design goals and simulation. They may change without notice. Contact Fairchild Semiconductor for current information.

Electrical Specifications

(T_A = 25°C, AV_{DD} = +5V, OV_{DD} = 3.3V, f_S = 20 MSPS, internal references, unless otherwise noted)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Unit
Dynamic Performance						
Signal-to-Noise & Distortion (SINAD)	f_{IN} = 5MHz	V		77		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 5MHz	V		77.5		dB
Total Harmonic Distortion (THD)	f_{IN} = 5MHz	V		-85		dB
Spurious Free Dynamic Range (SFDR)	f_{IN} = 5MHz	V		89		dB
Digital Inputs (CAL, RESETB)						
Logic “1” Voltage			2.4			V
Logic “0” Voltage					0.8	V
Logic “1” Input Current		V	-10		+10	µA
Logic “0” Input Current		V	-10		+10	µA
Input Capacitance		V		5		pF
Clock Input (CLK)						
Logic “1” Voltage				TBD		V
Logic “0” Voltage				TBD		V
Logic “1” Input Current		V	-10		+10	µA
Logic “0” Input Current		V	-10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs (DO-D13, OTR, BUSY)						
Logic “1” Output Current	V_{OH} = 4.5V, OV_{DD} = 5V	V		TBD		mA
Logic “1” Output Current	V_{OH} = 2.97V, OV_{DD} = 3.3V	V		-1.3		mA
Logic “0” Output Current	V_{OL} = 0.5V, OV_{DD} = 5V	V		TBD		mA
Logic “0” Output Current	V_{OL} = 0.33V, OV_{DD} = 3.3V	V		1.6		mA
Voltage Reference						
Output Voltage (V_{REF})		V		1.0		V
Reference Temp. Coefficient		V		100		ppm/°C
Top Reference Voltage (V_{RT})		V		3.25		V
Bottom Reference Voltage (V_{RC})		V		1.25		V
Common Mode Voltage (CM)		V		2.25		V
Power Supply Requirements						
AV_{DD} Supply Voltage		V	4.75	5.0	5.25	V
OV_{DD} Supply Voltage		V	3.0		5.25	V
AV_{DD} Supply Current	Full Scale 5MHz Input	V		158		mA
OV_{DD} Supply Current	Full Scale 5MHz Input	V		4		mA
Power Dissipation	Full Scale 5MHz Input	V		800		mW

NOTE: All electrical characteristics are subject to the following condition:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL CODES:

Level	Test Procedure
V	Parameter is a typical value for information purposes only.

Preliminary Data

Specification Definitions

Differential Linearity Error (DLE) or Differential Nonlinearity (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential Linearity Error is the maximum deviation, expressed in LSBs, from this ideal value.

Integral Linearity Error (ILE) or Integral Nonlinearity (INL)

The ideal transfer for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 0.5 LSB before the first code transition. "Full scale" is defined as a level 1.5 LSB beyond the last code transition. ILE is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

Missing Code

A code with zero width is missing. A code that is missing will have a DLE of –1. For example, as the input voltage is increasing, the output will jump between the adjacent codes, from 11…001 to 11…011, skipping 11…010. A specification that guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased.

Offset Error, Bipolar

In the differential mode, the major carry transition (0111…1 to 1000…0) should occur for an analog value 0.5 LSB below mid scale (0V differential input). The Offset Error specifies the deviation of the actual transition from that point.

Gain Error

The last transition should occur at an analog value 1.5 LSB below the nominal full scale. The first transition is 0.5 LSB above the low end of the scale (-FS in bipolar converters). The gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last transitions.

Input Full-Power Bandwidth

The frequency at which the amplitude of the reconstructed fundamental signal is reduced by 3 dB for a full-scale input.

Clock Duty Cycle

Ratio of clock pulse high (t_{CH}) to total clock period (t_{CLK}) times 100%.

$$\text{Duty Cycle} = \frac{t_{CH}}{t_{CLK}} \text{ X } 100\%$$

Signal-To-Noise Ratio (SNR)

The ratio of the power of the desired signal (fundamental) to the sum of the power of noise signals at a given point in time. The first 9 harmonics are excluded from the noise signals. Usually expressed in dB.

Harmonic

1. Of a sinusoidal wave, an integral multiple of the frequency of the wave. Note: The frequency of the sine wave is called the fundamental frequency or the first harmonic, the second harmonic is twice the fundamental frequency, the third harmonic is thrice the fundamental frequency, etc.

2. Of a periodic signal or other periodic phenomenon, such as an electromagnetic wave or a sound wave, a component frequency of the signal that is an integral multiple of the fundamental frequency. Note: The fundamental frequency is the reciprocal of the period of the periodic phenomenon. Contrast with fundamental overtone.

Total Harmonic Distortion (THD)

The ratio of the sum of the power of first 9 harmonics above the fundamental frequency to the power of the fundamental frequency. Usually expressed in dB.

Signal-to-Noise and Distortion Ratio (SINAD)

The ratio of the power of the desired signal (fundamental) to the sum of the power of all spectral components below Nyquist Frequency, including noise and distortion. Usually expressed in dB.

Effective Number of Bits (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{\text{SINAD} - 1.76}{6.02}$$

Spurious Free Dynamic Range (SFDR)

The ratio of the fundamental sinusoidal power to the power of the single largest harmonic or spurious signal.

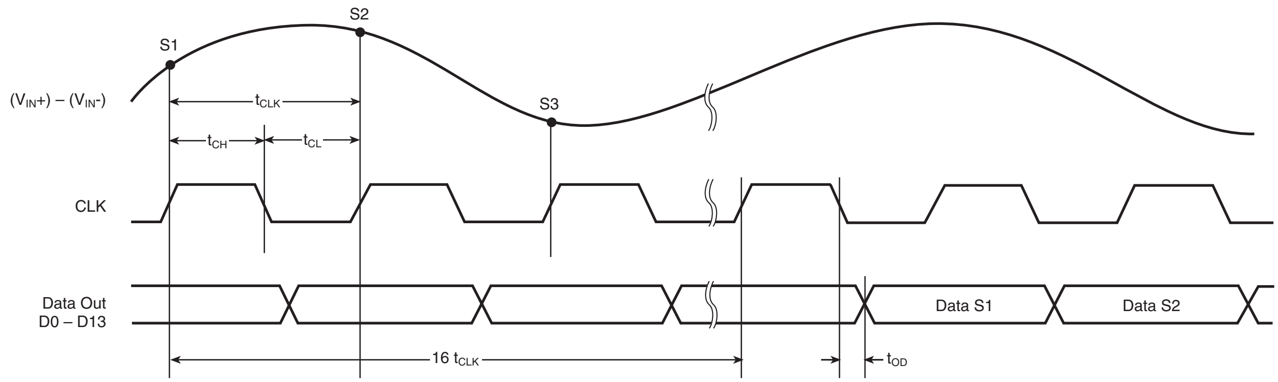


Figure 1: Timing Diagram

Functional Description

The SPT8120 is a five-stage, pipeline analog-to-digital converter (ADC) implemented in a fine-line CMOS process. The block diagram on page one illustrates the device's functional block-level implementation. The input sample-and-hold amplifier (SHA) guarantees its specified performance for the input signal frequencies up to the Nyquist frequency. It samples the differential analog input signal at the rising edge of CLK input and holds it for the next half-clock cycle. The SHA starts acquiring the input signal once CLK input goes low and acquires the next sample at the next rising edge of CLK.

Each of the first four pipeline stages consists of a flash ADC (ADCn) and a multiplying digital-to-analog converter (MDACn), where n = 1, 2, 3 or 4. The first stage flash ADC (ADC1) digitizes the output of the SHA and produces a lower-resolution digital code corresponding to the SHA output. The first stage MDAC1 subtracts from the SHA output the ideal voltage corresponding to the ADC1 code to generate the residue voltage, then amplifies the residue and passes it to the second stage. The subsequent stages 2 through 4 repeat the same operation, and ADC5 gives the last digital code corresponding to the output of MDAC4. The digital codes from ADC1 to ADC5 are time aligned and stored inside the "Data Alignment & Registers" block. The SPT8120 incorporates one bit of overlap between two subsequent pipeline stages and uses this redundancy to digitally correct for errors in ADC1 through ADC4. In addition, the SPT8120 employs an internal digital calibration circuitry to eliminate errors of the SHA and MDACs. Its function is controlled by an internal microcontroller. When in calibration mode, the SPT8120 configures itself such that errors of each stage can be measured by the ADC made of subsequent stages. The measured errors are stored in on-chip digital memory (RAM). During subsequent normal conversions, the microcontroller looks up the RAM contents and makes digital corrections of the errors, to produce the final 16-bit digital output free of the errors. The 16-bit digital output along with OTR (out-of-range flag) are latched and buffered to drive the output pins. These output buffers have their own power supply and ground (OV_{DD} and OGND), and can interface +5V or +3.3V external logic circuitry.

The SPT8120 has an internal bandgap voltage reference that produces a temperature-stable 1V output at V_{REF}/EXTB pin. This voltage sets the input span of the SPT8120 about CM of 2.25V. Therefore, the input span nominally is set to 1.25V (V_{RC}) to 3.25V (V_{RT}). Internal buffers provide low-impedance outputs for CM, V_{RT} and V_{RC} that are used throughout the pipeline stages. The output impedance of the V_{REF}/EXTB pin is set relatively high (approximately 4.7kΩ), allowing the user to override the internal 1V reference and change the input span. The user can also drive V_{RT} and V_{RC} directly with external buffers. To do this, V_{REF}/EXTB must be shorted to AGND. Shorting this pin to AGND disables the internal buffers driving V_{RT} and V_{RC}.

Internal Digital Calibration

The SPT8120 achieves the specified performance by internal digital calibration, eliminating the need for external adjustments or trimming by the user.

The calibration takes advantage of the fact that the accuracy requirement for a pipeline stage is progressively reduced. For example, the SHA and MDAC1 must be accurate to 16 bits in order to achieve 16 bits of overall ADC accuracy. If we assume that ADC1's resolution is N and that there is a one-bit overlap between the first and second stages, the accuracy requirement for MDAC2 is reduced to (16–N+1) bits (Note: N>1). The obtainable accuracy of a stage is set by the circuit's non-idealities such as device mismatches, finite bandwidth, finite gain, etc. For the specific implementation of the SPT8120, the process warrants the required accuracy of stage 4 and stage 5 without calibration.

The calibration sequence starts with the ADC made of stage 4 and 5 measuring errors in MDAC3 and storing the digital representation of each of the errors (calibration coefficient) in RAM. The stage 3 calibration coefficients are used to make the ADC composed of stage 3, 4 and 5 accurate to its required specifications. The next sequence measures errors in MDAC2 by the ADC made of stages 3, 4 and 5, and stores the calibration coefficients in RAM. This is repeated until all relevant errors of SHA and MDACs are measured and stored in RAM.

The user can initiate the calibration by driving the CAL pin high for more than two falling edges of CLK while holding RESETB high. The internal microcontroller then outputs high to the BUSY pin, indicating that the SPT8120 is in calibration mode. BUSY will remain high until all the calibration coefficients have been successfully measured and stored in RAM. Once BUSY returns to low, the SPT8120 is ready for normal conversions of analog input at V_{IN}+ and V_{IN}-. The number of clock cycles it takes to complete the digital calibration is about 1.49 million, which translates to 74.5ms for a 20MHz clock. By driving low the asynchronous reset pin, RESETB, the user can interrupt the calibration in progress. When the SPT8120 detects RESETB low, it clears all the calibration coefficients in RAM and sits in the initial idle state. In order to start new conversions to the specifications, the user must drive RESETB high again and drive CAL high to restart calibration.

It is important to note that both V_{IN}+ and V_{IN}- pins are shorted to CM through a pair of internal switches. Therefore, the user must either leave V_{IN}+ and V_{IN}- open or drive both to CM during the calibration mode. The digital outputs during the calibration are controlled by the internal calibration machine and should be disregarded. It is the user's responsibility to establish stable power supplies and references (when external references are used) prior to issuing CAL high, and to maintain their integrity during the calibration.

Power-on Sequence and Initialization

Power supplies AV_{DD} and OV_{DD} may be turned on in any sequence. Inputs V_{IN}+, V_{IN}-, and CLK may be driven only after all the supplies have been established. If external references are used to drive V_{RT} and V_{RC} pins, they can be applied only after all supplies are in their normal range. Once all supplies have been provided, CLK input may be driven with a frequency up to 20MHz. The user must then initialize the SPT8120 in order to obtain the specified performance. To do this, the user must first drive RESETB pin to logic low for at least one full clock cycle and subsequently drive CAL high to initiate the internal calibration (see Internal Digital Calibration and Typical Interface Circuit sections).

Reference Circuit

Figure 2 shows the equivalent circuit that produces V_{RT}, V_{RC}, CM and V_{REF}/EXTB. The on-chip bandgap circuit creates temperature-stable reference voltages of 2.25V and 1.0V. The op amp A1 provides a buffer for 2.25V and drives the CM pin, as well as the internal ADC core circuitry. The 1.0V output from the bandgap has about 4.7kΩ output impedance to the V_{REF}/EXTB pin. The span of the ADC is set to $+V_{REF}$ and $–V_{REF}$ about CM as shown in Figure 2, where V_{REF} is the voltage at pin V_{REF}/EXTB. A2 and A3 provide low impedance outputs at V_{RT} and V_{RC}. It should be noted that all three op amps in Figure 2 (A1, A2, and A3) require an external capacitor of 4.7 µF or larger from each output pin (V_{RT}, V_{RC}, or CM) to AGND for compensation as well as noise reduction.

The finite output impedance of the V_{REF}/EXTB pin allows the user to use an external reference circuit to overdrive this pin. The user may do so in order to set a different ADC span voltage or to obtain a span voltage that has less drift over temperature than the internal reference. Note that the specified performance is guaranteed only for $V_{REF} = 1.0$ V. The user can also drive V_{RT} and VRC directly with external buffers by shorting the V_{REF}/EXTB pin to AGND externally. The internal comparator COMP detects this and disables both A2 and A3, making V_{RT} and V_{RC} pins high impedance.

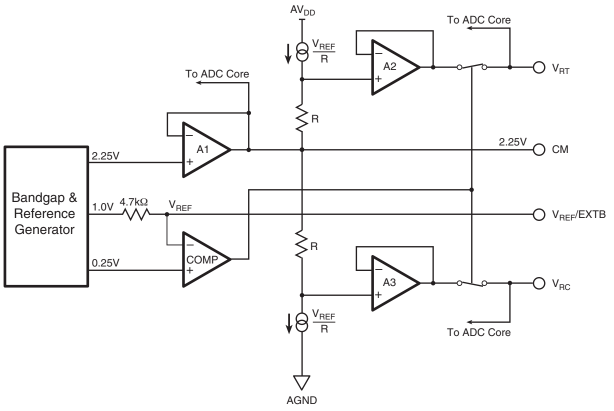


Figure 2: Equivalent Reference Circuit

Equivalent Input Circuit

Figure 3 shows a simplified, equivalent input circuit when the input is being sampled. The inputs, V_{IN}+ and V_{IN}-, drive the bottom plates of the sampling capacitors, CS+ and CS-, respectively. The top plates of the sampling capacitors are shorted to CM through sampling switches SWS+ and SWS-. A sampling of the input is accomplished by simultaneously opening SWS+ and SWS-. An internal clock driver circuit generates this control signal so that the sampling instance is defined at the rising edge of CLK input.

The SPT8120 incorporates two switches that connect $V_{IN}+$ and $V_{IN}-$ to CM during calibration. These switches are shown as SWC+ and SWC- in Figure 3. The typical on-resistance of the switches is about 900Ω each. This configuration enables the internal calibration to calibrate out the offset error of SHA and to achieve the superb specification for mid-scale error of the ADC. The user must ensure that both $V_{IN}+$ and $V_{IN}-$ are left open or driven to CM during calibration.

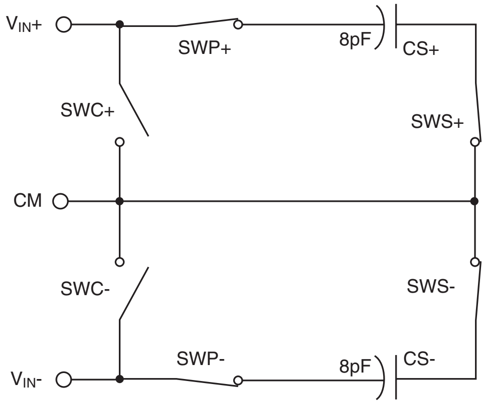


Figure 3: Equivalent Input Circuit

Typical Interface Circuit

Figure 5 shows a typical interface circuit reflecting the grounding and bypassing scheme used in the evaluation board. All bypass capacitors must be located as close to the package pins as possible. It is also important to keep a minimum lead distance between the input pins, $V_{IN}+$ and $V_{IN}-$, and the transformer.

It is recommended that the user follow the timing requirements for RESETB and CAL indicated in Figure 4. In this example, RESETB stays logic low for two full clock cycles. CAL must remain logic high for two or more clock cycles, and the time from RESETB returning high to the rising edge of CAL must be at least two clock cycles, based on the internal operation of the SPT8120. It has been verified that the timing specified in Figure 4 functions properly with the evaluation board. However, it should be noted that this time between RESETB going high and CAL going high also depends on the external system design and configuration. Once RESETB goes low for two clock cycles, the SPT8120 initializes its internal bias condition. The internal initialization takes place instantaneously. However, the amount of time it takes for the voltages at V_{RT}, V_{RC}, CM, V_{BS}, and V_{REF}/EXTB, to stabilize will vary depending on the external bypassing circuits at these pins. The user must ensure that the SPT8120 has reached a stable operation condition before initiating a calibration by driving CAL high. It is also a user's responsibility to make sure that all the power supplies have reached a stable condition before initiating the Reset/Cal sequence.

As in the case with any high-speed, high-resolution ADCs, the quality of clock input to the SPT8120 significantly affects its performance. A SHA with a sample clock jitter of t_J, sampling a full-scale input of frequency f_{IN}, has the SNR due only to the clock jitter given by:

$$\mathrm{SNR} = -20 \cdot \log 10\,(2p \cdot f_{IN} \cdot t_J)$$

For a 10MHz input with a 3ps clock jitter, SNR is limited to 74.5dB. It is therefore extremely important to drive the device with a clock signal having the lowest possible jitter.

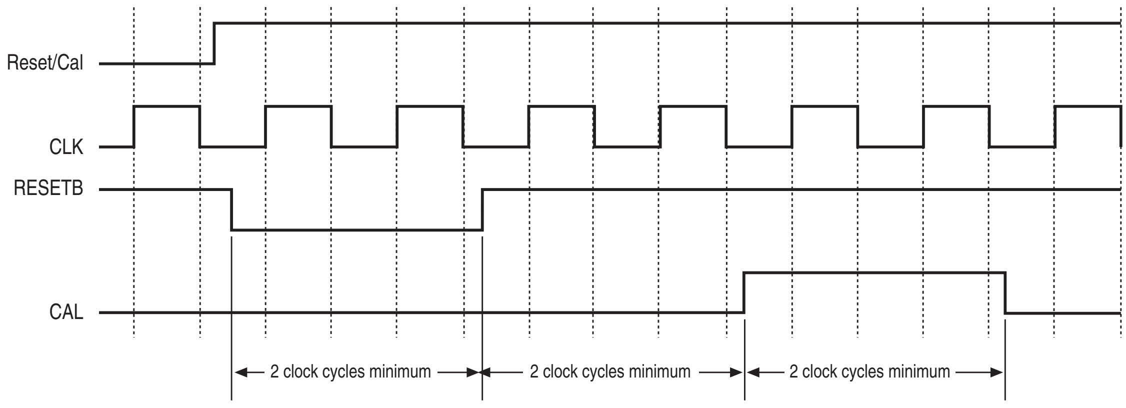


Figure 4: Reset/Cal Timing Diagram

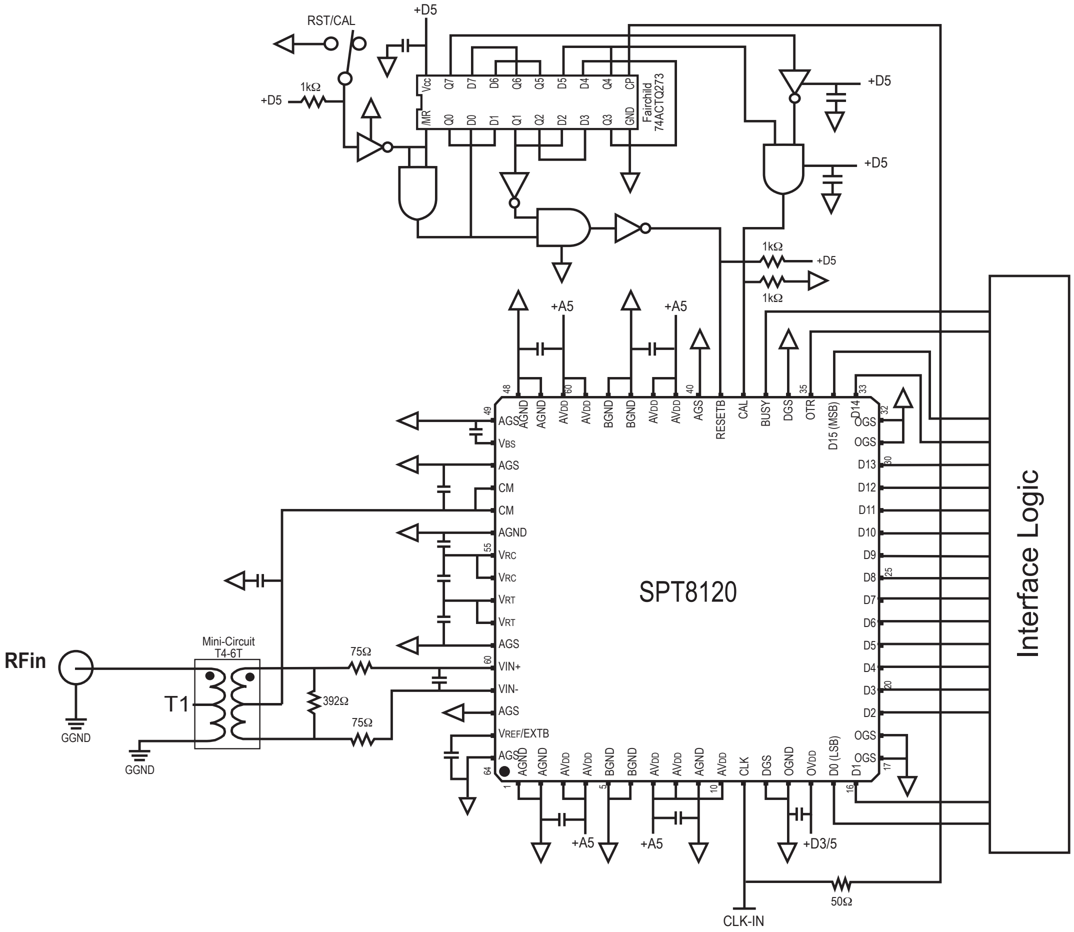
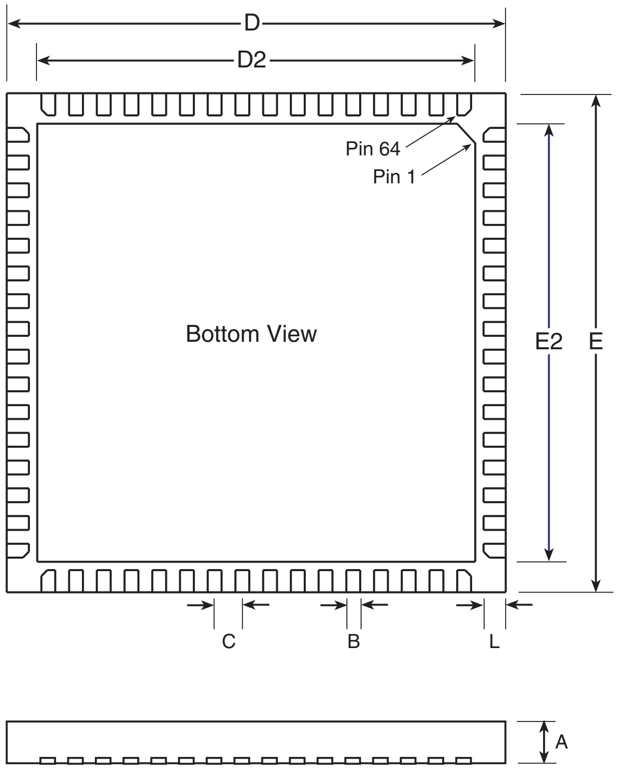


Figure 5: Typical Interface Circuit (see Application Note AN8120 for a detailed schematic)

Package Outline

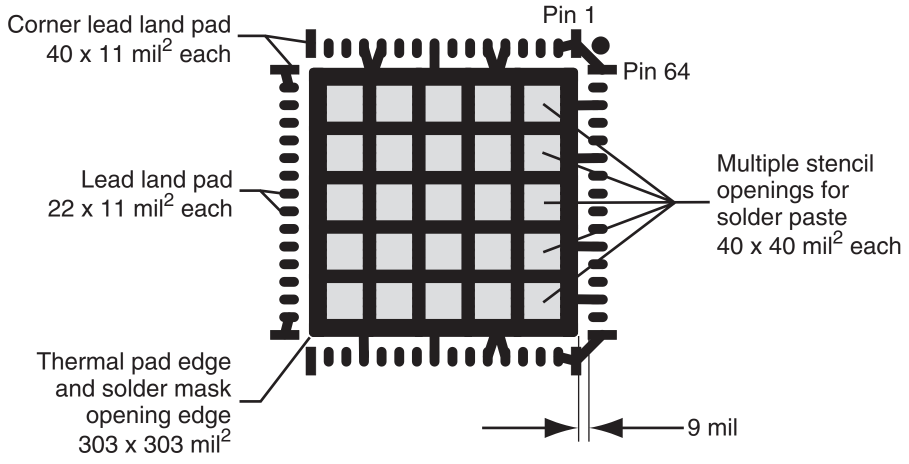
64-pin LPCC



Dimensions

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.028	0.031	0.70	0.80
B	0.009	0.011	0.230	0.280
C	0.020 BSC		0.50 BSC	
D	0.350	0.358	8.90	9.10
D2	0.303	0.311	7.70	7.90
E	0.350	0.358	8.90	9.10
E2	0.303	0.311	7.70	7.90
L	0.014	0.018	0.35	0.45

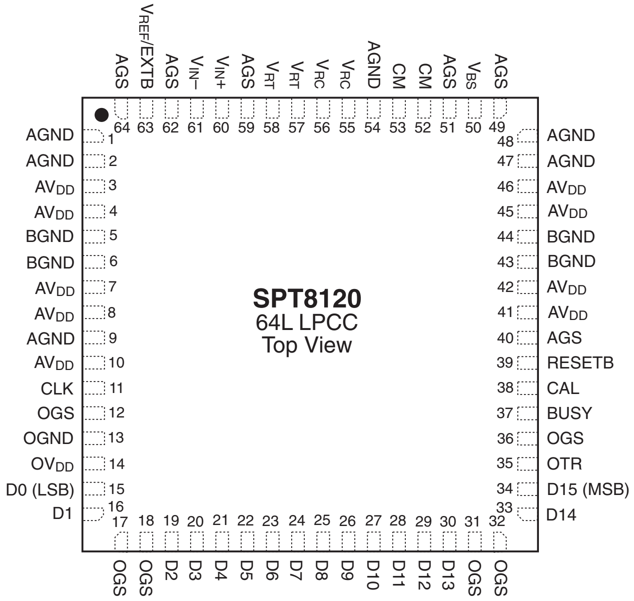
Recommended PCB Layout



Die Attach Pad or DAP is exposed at the bottom of the package. In the Package Outline above, DAP is shown as the square area of D2 and E2 (with a 45° cut at the corner of pin 1 and pin 64). The user must have a thermal pad equal in size to the exposed DAP on the PCB and connect it to AGND. An array of small solder paste openings should be used to attach DAP to the thermal pad. The total area of the openings should be approximately 50% of the thermal pad area. Fairchild recommends stainless steel stencils of 0.125mm to 0.150mm in thickness for solder paste applications. Refer to the Recommended PCB Layout figure above for the design of the thermal pad and solder paste.

Preliminary Data

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Description
AGND	1, 2, 6,9, 47, 48, 54	Ground
AVDD	3, 4, 7, 8, 10, 41, 42, 45, 46	+5V supply
AGS	40, 49, 51, 59, 62, 64	Analog ground sense. Connect to AGND.
BGND	5, 6, 43, 33	Ground
CLK	11	Clock input
OGND	13	Ground for BUSY, OTR, and Data Bit Outputs
OVDD	14	+3.3V to +5V supply for BUSY, OTR. and Data Bit Outputs
OGS	12, 17, 18, 31, 32, 36	OGND sense. Connect to OGND.
D0–D15	15, 16, 19–30, 33, 34	Data Bit Outputs. D0 = LSB, D15 = MSB
OTR	35	Out of Range Output. OTR goes High for the analog input above (over range) or below (underrange) the full-scale range. The corresponding Data Bit Outputs are all 1s for overrange, and all 0s for underrange.
BUSY	37	Busy Output; BUSY goes High when the SPT8120 goes into its internal calibration routine and remains High until it completes the calibration. The internal calibration routine takes approximately 74.5ms for 20MHz clock input. The SPT8120 ignores the analog input when BUSY is High. When BUSY is Low, it is ready to convert the analog input.
CAL	38	Calibration Start Input. Holding CAL High for more than two falling edges of CLK, while RESETB is High, initiates the SPT8120's internal calibration routine.

Pin Definitions (Continued)

Pin Name	Pin Number	Description
RESETB	39	Reset Input (active Low). Logic 0 on this asynchronous reset pin will set the internal digital state machine to its initial state and clear all internal calibration coefficients.
V_{BS}	50	Noise Reduction Pin. Connect a noise reduction capacitor of 4.7µF or larger from this pin to AGND.
CM	52, 53	Common Mode Level Output. +2.25V nominal. Connect a noise reduction capacitor of 4.7µF or larger from this pin to AGND.
V_{RC}	55, 56	Lower Reference. +1.25V nominal. This voltage sets the lower bound of analog input span. Connect a noise reduction capacitor of 4.7µF or larger from this pin to AGND.
V_{RT}	57, 58	Upper Reference. +3.25V nominal. This voltage sets the upper bound of analog input span. Connect a noise reduction capacitor of 4.7µF or larger from this pin to AGND.
$V_{IN}+$	60	Analog Input Pin (+). The nominal span at this pin is +1.25V to +3.25V.
$V_{IN}-$	61	Analog Input Pin (–). The nominal span at this pin is +3.25V to +1.25V.
V_{REF}/EXTB	63	Voltage Reference I/O Pin. +1.00V nominal. The voltage at this pin sets the span above and below CM for each analog input pin. Driving VREF/EXTB to 0V will disable internal buffers driving V_{RT} and V_{RC}, allowing the user to drive $V_{RT}$and V_{RC} externally. Connect a noise reduction capacitor of 4.7µF or larger from this pin to AGND.

Preliminary Data

Ordering Information

Model	Part Number	Package	Container	Pack Qty
SPT8120	SPT8120SIC	LPCC-64	?	?

Temperature range for all parts: -40°C to +85°C.

Preliminary Data

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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