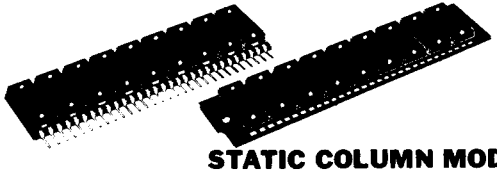


# MH1M09B2J-7,-8,-10/ MH1M09B2JA-7,-8,-10

## STATIC COLUMN MODE 1048576-WORD BY 9-BIT DYNAMIC RAM

## DESCRIPTION

The MH1M09B2J, JA is 1048576 word x 9 bit dynamic RAM and consists of nine industry standard 1M x 1 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required.

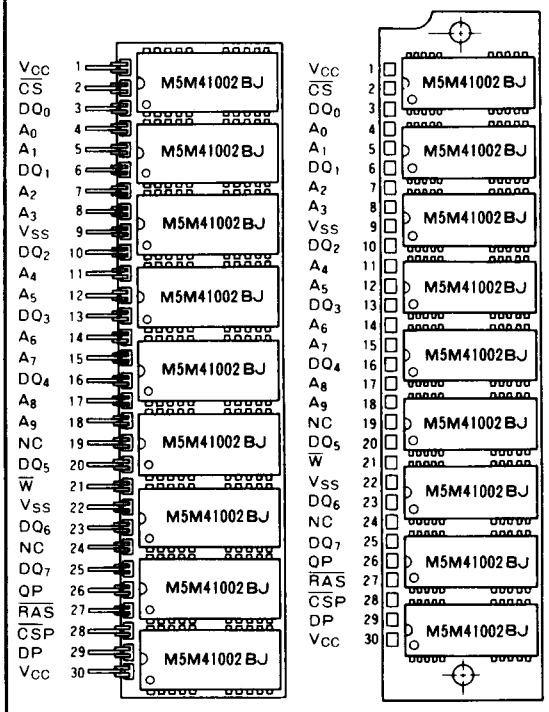
## FEATURES

- Performance ranges

| Type name | Access time (max) (ns) | Cycle time (min) (ns) | Power dissipation (typ) (mW) |
|---|---|---|---|
| MH1M09B2J-7<br>MH1M09B2JA-7 | 70 | 140 | 2070 |
| MH1M09B2J-8<br>MH1M09B2JA-8 | 80 | 160 | 1800 |
| MH1M09B2J-10<br>MH1M09B2JA-10 | 100 | 190 | 1575 |

- Utilizes industry standard 1M RAMs in SOJ
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation 24.8mW (max) CMOS input level
- Low operation power dissipation:
  MH1M09B2J-7, MH1M09B2JA-7 . . . 3.96W (max)
  MH1M09B2J-8, MH1M09B2JA-8 . . . 3.47W (max)
  MH1M09B2J-10, MH1M09B2JA-10 . . 2.97W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22$\mu$F x 9) decoupling capacitors
- 512 refresh cycles every 8ms, $A_9$ Pin is not need for refresh
- Common $\overline{CS}$ control for eight common Data-In and Data-Out lines.
- Separate $\overline{CS}$ (CSP) control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operation to prevent contention on Data-In and Data-Out.
- Bit nine (DP, QP) controlled by $\overline{CSP}$ is generally used for parity.

## PIN CONFIGURATION (TOP VIEW)



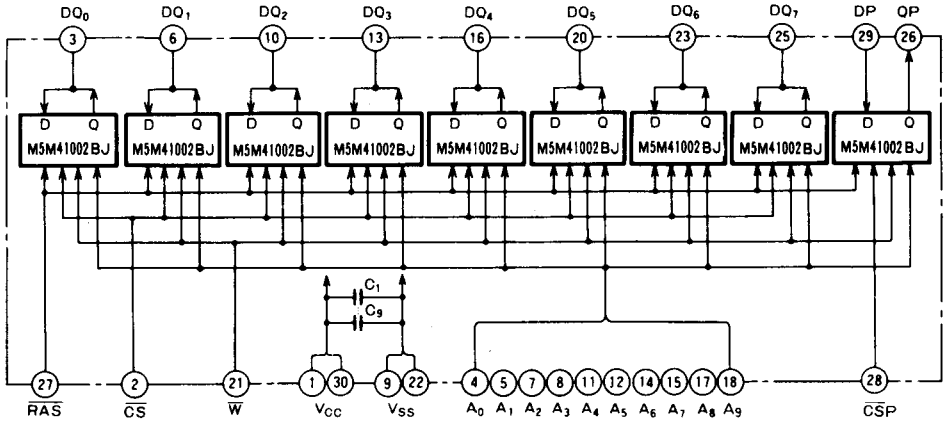

Outline
30N5A (MH1M09B2JA)
30N9A (MH1M09B2J)

NC NO CONNECTION

## APPLICATION

Main memory unit for computers, Refresh memory.

## BLOCK DIAGRAM



## FUNCTION

The MH1M09B2J, JA provide, in addition to normal read, and early write operations, a number of other functions, e.g., static Column mode. $\overline{RAS}$-only refresh and $\overline{CS}$ before $\overline{RAS}$ refresh. This input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | Input/Output | | Refresh | Remark |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CS}$ | $\overline{W}$ | Row address | Column address | Input | Output | | |
| Read | ACT | ACT | NAC | APD | APD | OPN | VLD | YES | Static column mode identical |
| Early write | ACT | ACT | ACT | APD | APD | VLD | OPN | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | APD | DNC | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | DNC | DNC | DNC | OPN | VLD | YES | |
| $\overline{CS}$ before $\overline{RAS}$ refresh | ACT | ACT | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −1～7 | V |
| $V_I$ | Input voltage | | −1～7 | V |
| $V_O$ | Output voltage | | −1～7 | V |
| $I_O$ | Output current | | 50 | mA |
| Pd | Power dissipation | Ta＝25°C | 9 | W |
| Topr | Operating temperature | | 0～70 | °C |
| Tstg | Storage temperature | | −40～120 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage all inputs | −1.0 | | 0.8 | V |

Note 1: All voltage values are with respect to $V_{SS}$.

## ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$＝−5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$＝4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | QP floating 0V≦$V_{OUT}$≦5.5V | −20 | | 20 | μA |
| $I_I$ | Input current | | 0V≦$V_{IH}$≦6.5V, Other input pins＝0V | −90 | | 90 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$ operating (Note 3, 4) | MH1M09B2-7 | $\overline{RAS}$, $\overline{CS}$ cycling $t_{RC}$＝$t_{WC}$＝min, output open | | | 720 | mA |
| | | MH1M09B2-8 | | | | 630 | |
| | | MH1M09B2-10 | | | | 540 | |
| $I_{CC2}$ | Supply current from $V_{CC}$, standby | | $\overline{RAS}$＝$\overline{CS}$＝$V_{IH}$, output open | | | 18 | mA |
| | | | $\overline{RAS}$＝$\overline{CS}$≧$V_{CC}$−0.5, output open | | | 4.5 | |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$ refreshing (Note 3) | MH1M09B2-7 | $\overline{RAS}$ cycling, $\overline{CS}$＝$V_{IH}$ $t_{RC}$＝min, output open | | | 720 | mA |
| | | MH1M09B2-8 | | | | 630 | |
| | | MH1M09B2-10 | | | | 540 | |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$ $\overline{CS}$ before $\overline{RAS}$ refresh mode (Note 3) | MH1M09B2-7 | $\overline{CS}$ before $\overline{RAS}$ refresh cycling $t_{RC}$＝min, output open | | | 720 | mA |
| | | MH1M09B2-8 | | | | 630 | |
| | | MH1M09B2-10 | | | | 540 | |
| $I_{CC7(AV)}$ | Average supply current from $V_{CC}$ static column mode (Note 3, 4) | MH1M09B2-7 | $\overline{RAS}$＝$V_{IL}$, $\overline{CS}$＝cycling $t_{SC}$＝min, output open | | | 630 | mA |
| | | MH1M09B2-8 | | | | 540 | |
| | | MH1M09B2-10 | | | | 450 | |

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC6(AV)}$ and $I_{CC7(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC7(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

## CAPACITANCE (Ta＝0～70°C, $V_{CC}$＝5V±10%, $V_{SS}$＝0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{I(A)}$ | Input capacitance, address inputs | $V_I$＝$V_{SS}$ f＝1MHz $V_i$＝25mVrms | | | 60 | pF |
| $C_{(DQ)}$ | Data input/data output capacitance | | | | 17 | pF |
| $C_{I(\overline{W})}$ | Input capacitance, write control input | | | | 75 | pF |
| $C_{I(\overline{RAS})}$ | Input capacitance, $\overline{RAS}$ input | | | | 75 | pF |
| $C_{I(\overline{CS})}$ | Input capacitance, $\overline{CS}$ input | | | | 70 | pF |
| $C_{I(\overline{CSP})}$ | Input capacitance, $\overline{CSP}$ input | | | | 15 | pF |
| $C_{I(DP)}$ | Input capacitance | | | | 15 | pF |
| $C_{O(QP)}$ | Output capacitance | $V_O$＝$V_{SS}$, f＝1MHz, $V_i$＝25mVrms | | | 12 | pF |

## SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 5)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MH1M09B2-7 | | MH1M09B2-8 | | MH1M09B2-10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CAC}$ | Access time from $\overline{CS}$ | (Note 6, 7) | | 20 | | 20 | | 25 | ns |
| $t_{RAC}$ | Access time from $\overline{RAS}$ | (Note 6, 8) | | 70 | | 80 | | 100 | ns |
| $t_{CAA}$ | Column Address access time | (Note 6, 9) | | 35 | | 40 | | 50 | ns |
| $t_{CLZ}$ | Output low impedance time from $\overline{CS}$ low | (Note 6) | 5 | | 5 | | 5 | | ns |
| $t_{OFF}$ | Output disable time after $\overline{CS}$ high | (Note 10) | 0 | 20 | 0 | 20 | 0 | 25 | ns |

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assume that $t_{RCD} \geq t_{RCD(max)}$, $t_{RAD} \leq t_{RAD(max)}$.

8: Assume that $t_{RCD} \leq t_{RCD(max)}$, $t_{RAD} \leq t_{RAD(max)}$. If $t_{RCD}$ or $t_{RAD}$ is greater than $t_{RCD(max)}$ or $t_{RAD(max)}$ then $t_{RAC}$ will increase by the amount that $t_{RCD}$ or $t_{RAD}$ exceeds $t_{RCD(max)}$ or $t_{RAD(max)}$.

9: Assume that $t_{RCD} - t_{RAD} \leq t_{CAA(max)} - t_{CAC(max)}$, and $t_{RCD} \geq t_{RCD(max)}$.

10: $t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

## TIMING REQUIREMENTS (For Read, Write, Static Column Cycles)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 11, 12)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MH1M09B2-7 | | MH1M09B2-8 | | MH1M09B2-10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{REF}$ | Refresh cycle time | | | 8 | | 8 | | 8 | ms |
| $t_{RP}$ | $\overline{RAS}$ high pulse width | | 60 | | 70 | | 80 | | ns |
| $t_{RCD}$ | Delay time, $\overline{RAS}$ low to $\overline{CS}$ low | (Note 13) | 20 | 50 | 25 | 60 | 25 | 75 | ns |
| $t_{CRP}$ | Delay time, $\overline{CS}$ high to $\overline{RAS}$ low | (Note 14) | 10 | | 10 | | 10 | | ns |
| $t_{CPN}$ | $\overline{CAS}$ high pulse width | (Note 15) | 30 | | 35 | | 35 | | ns |
| $t_{RAD}$ | Column address delay time from $\overline{RAS}$ low | (Note 16) | 15 | 35 | 20 | 40 | 20 | 50 | ns |
| $t_{ASR}$ | Row address setup time before $\overline{RAS}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{ASC}$ | Column address setup time before $\overline{CS}$ low or $\overline{W}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{RAH}$ | Row address hold time after $\overline{RAS}$ low | | 10 | | 15 | | 15 | | ns |
| $t_{CAH}$ | Column address hold time after $\overline{CS}$ low or $\overline{W}$ low | | 15 | | 20 | | 20 | | ns |
| $t_T$ | Transition time | (Note 17) | 3 | 50 | 3 | 50 | 3 | 50 | ns |

Note 11: The timing requirements are assumed $t_T = 5ns$.

12: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

13: $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD}$ is less than $t_{RCD(max)}$, access time is $t_{RAC}$. If $t_{RCD}$ is greater than $t_{RCD(max)}$, access time is $t_{RCD} + t_{CAC}$. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.

14: $t_{CRP}$ requirement is applicable for all $\overline{RAS}/\overline{CS}$ cycles.

15: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)}$ except for $t_{CP}$ of static column mode cycle.

16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$, access time is assumed by $t_{CAA}$ for read cycle.

17: $t_T$ is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

## Read and Refresh Cycles

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MH1M09B2-7 | | MH1M09B2-8 | | MH1M09B2-10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read cycle time | | 140 | | 160 | | 190 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width | | 70 | 10000 | 80 | 10000 | 100 | 10000 | ns |
| $t_{CS}$ | $\overline{CS}$ low pulse width | | 20 | 10000 | 20 | 10000 | 25 | 10000 | ns |
| $t_{CSH}$ | $\overline{CS}$ hold time after $\overline{RAS}$ low | | 70 | | 80 | | 100 | | ns |
| $t_{RSH}$ | $\overline{RAS}$ hold time after $\overline{CS}$ low | | 20 | | 20 | | 25 | | ns |
| $t_{RCS}$ | Read setup time before $\overline{CS}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{RCH}$ | Read hold time after $\overline{CS}$ high | (Note 18) | 10 | | 10 | | 10 | | ns |
| $t_{RRH}$ | Read hold time after $\overline{RAS}$ high | (Note 18) | 10 | | 10 | | 10 | | ns |
| $t_{RAL}$ | Column address to $\overline{RAS}$ setup time | | 35 | | 40 | | 50 | | ns |
| $t_{AH}$ | Column address hold time after $\overline{RAS}$ high | | 10 | | 10 | | 10 | | ns |
| $t_{RPC}$ | Precharge to $\overline{CS}$ active time | | 0 | | 0 | | 0 | | ns |

Note 18: Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

## Write Cycle

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MH1M09B2-7 | | MH1M09B2-8 | | MH1M09B2-10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | Write cycle time | | 140 | | 160 | | 190 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width | | 70 | 10000 | 80 | 10000 | 100 | 10000 | ns |
| $t_{CS}$ | $\overline{CS}$ low pulse width | | 20 | 10000 | 20 | 10000 | 25 | 10000 | ns |
| $t_{CSH}$ | $\overline{CS}$ hold time after $\overline{RAS}$ low | | 70 | | 80 | | 100 | | ns |
| $t_{RSH}$ | $\overline{RAS}$ hold time after $\overline{CS}$ low | | 20 | | 20 | | 25 | | ns |
| $t_{WCS}$ | Write setup time before $\overline{CS}$ low | (Note 19) | 0 | | 0 | | 0 | | ns |
| $t_{WCH}$ | Write hold time after $\overline{CS}$ low | | 15 | | 15 | | 20 | | ns |
| $t_{WH}$ | Write command hold time for output disable | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write pulse width | | 15 | | 15 | | 20 | | ns |
| $t_{DS}$ | Data setup time | | 0 | | 0 | | 0 | | ns |
| $t_{DH}$ | Data hold time after $\overline{CS}$ low | | 15 | | 15 | | 20 | | ns |

Note 19: When $t_{WCS} < t_{WCS(min)}$, Data input will contend with the data output because of the common I/O feature.

## Static Column Mode Cycle (Read, Early Write Cycle)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | MH1M09B2-7 | | MH1M09B2-8 | | MH1M09B2-10 | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{RSC}$ | SC read cycle time | 40 | | 45 | | 55 | | ns |
| $t_{WSC}$ | SC write cycle time | 40 | | 45 | | 55 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width | 110 | 100000 | 125 | 100000 | 155 | 100000 | ns |
| $t_{CS}$ | $\overline{CS}$ low pulse width | 20 | 10000 | 20 | 10000 | 25 | 10000 | ns |
| $t_{CP}$ | $\overline{CS}$ high pulse width | 10 | | 10 | | 10 | | ns |
| $t_{WI}$ | Write invalid time | 10 | | 10 | | 10 | | ns |
| $t_{WH}$ | Write command hold time for output disable | 0 | | 0 | | 0 | | ns |
| $t_{AOH}$ | Data hold time from address change | 10 | | 10 | | 10 | | ns |

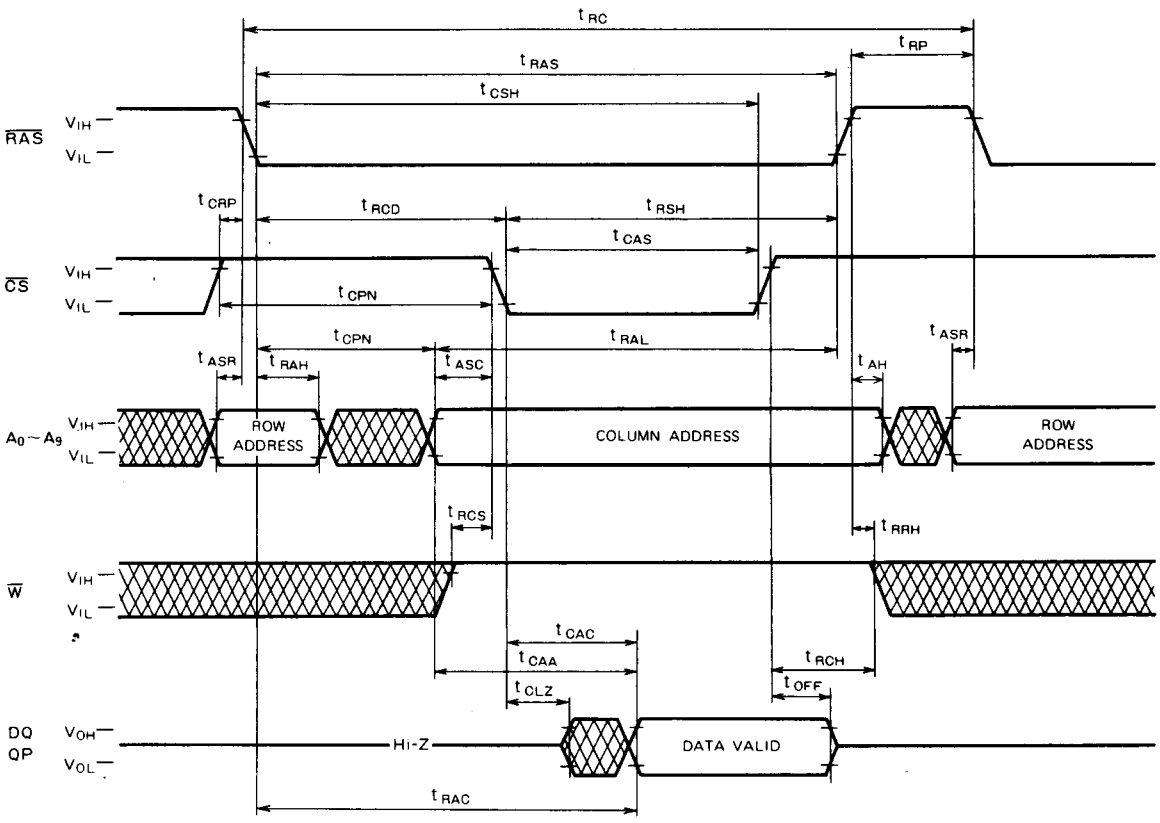
## $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle (Note 20)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | MH1M09B2-7 | | MH1M09B2-8 | | MH1M09B2-10 | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{CSR}$ | $\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh | 10 | | 10 | | 10 | | ns |
| $t_{CHR}$ | $\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh | 15 | | 15 | | 20 | | ns |
| $t_{RPC}$ | Precharge to $\overline{CS}$ active time | 0 | | 0 | | 0 | | ns |

Note 20: Eight or more $\overline{CS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CS}$ before $\overline{RAS}$ refresh mode.

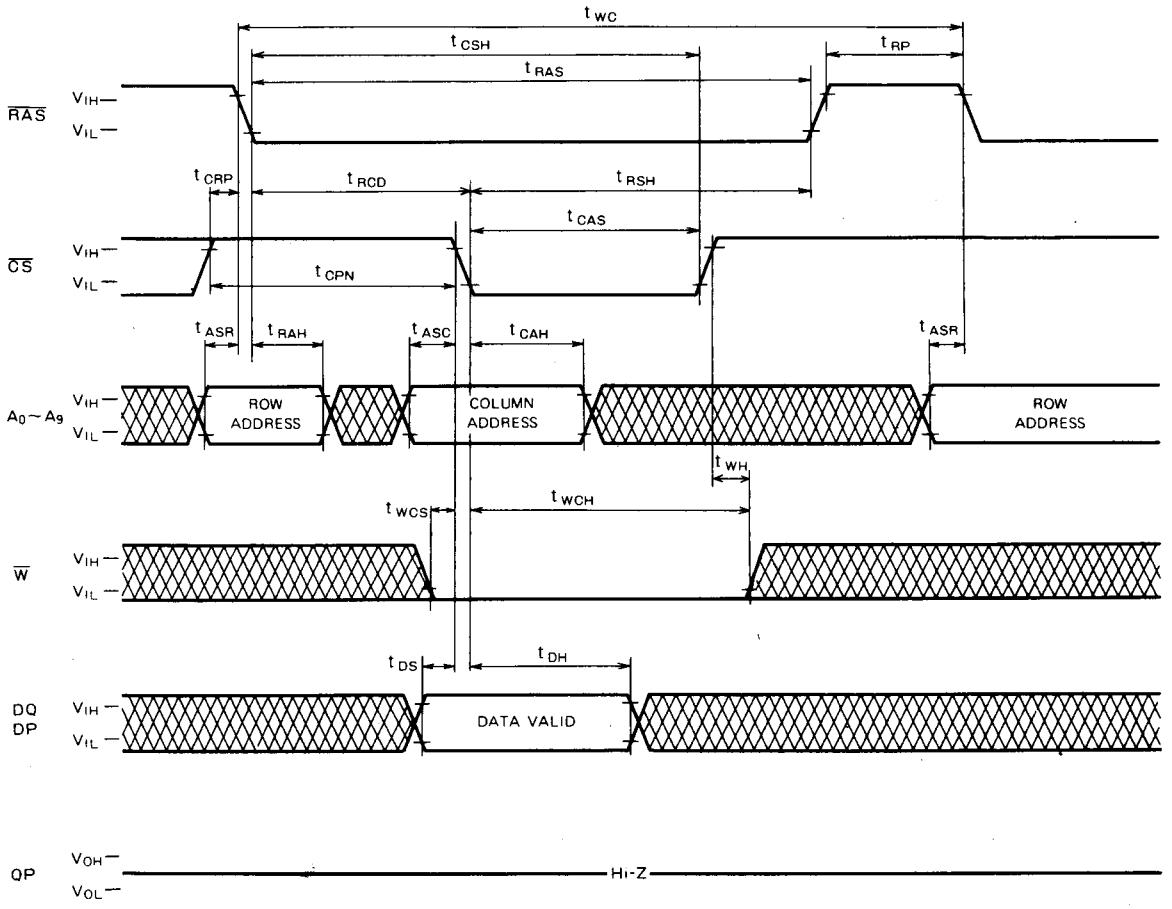
## Timing Diagrams (Note 21)

### Read Cycle

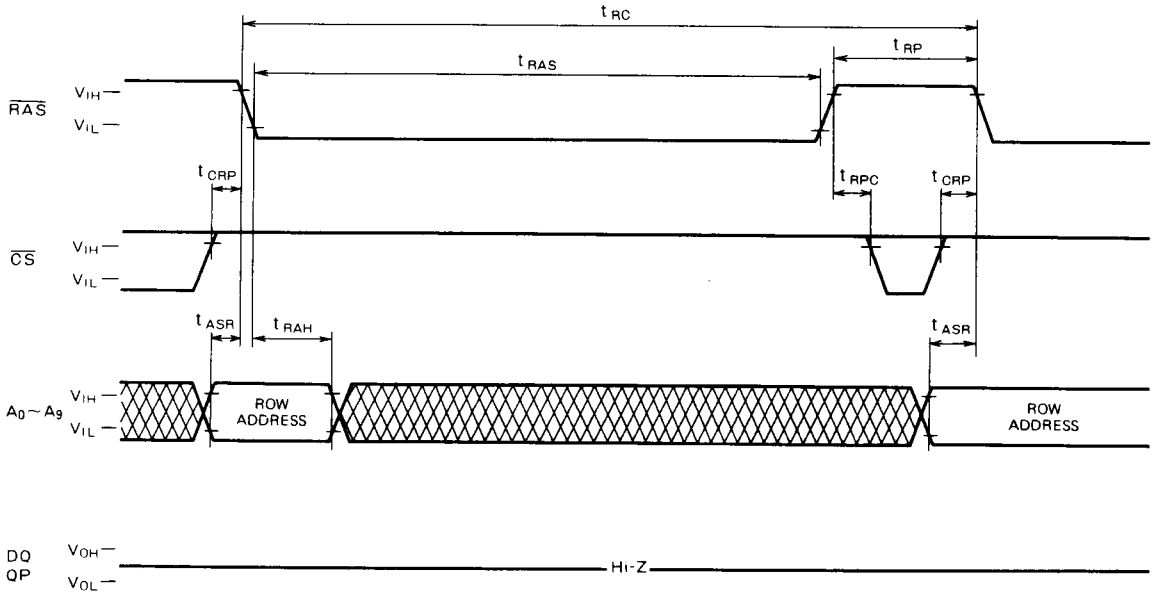



Note 21 Indicates the don't care input.

## Early Write Cycle

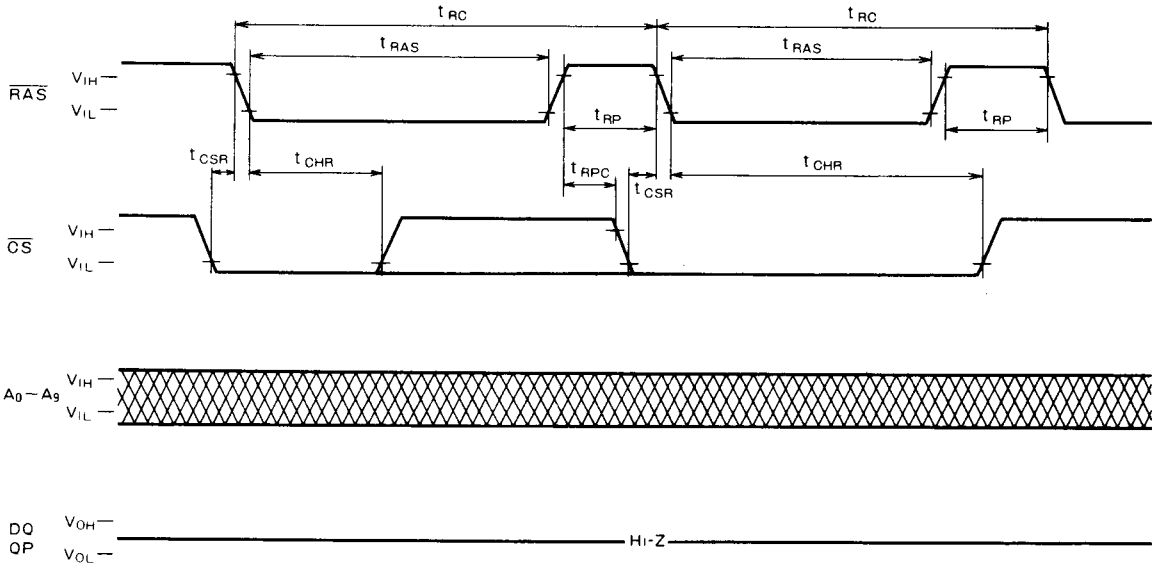


## $\overline{RAS}$ only Refresh Cycle (Note 22)



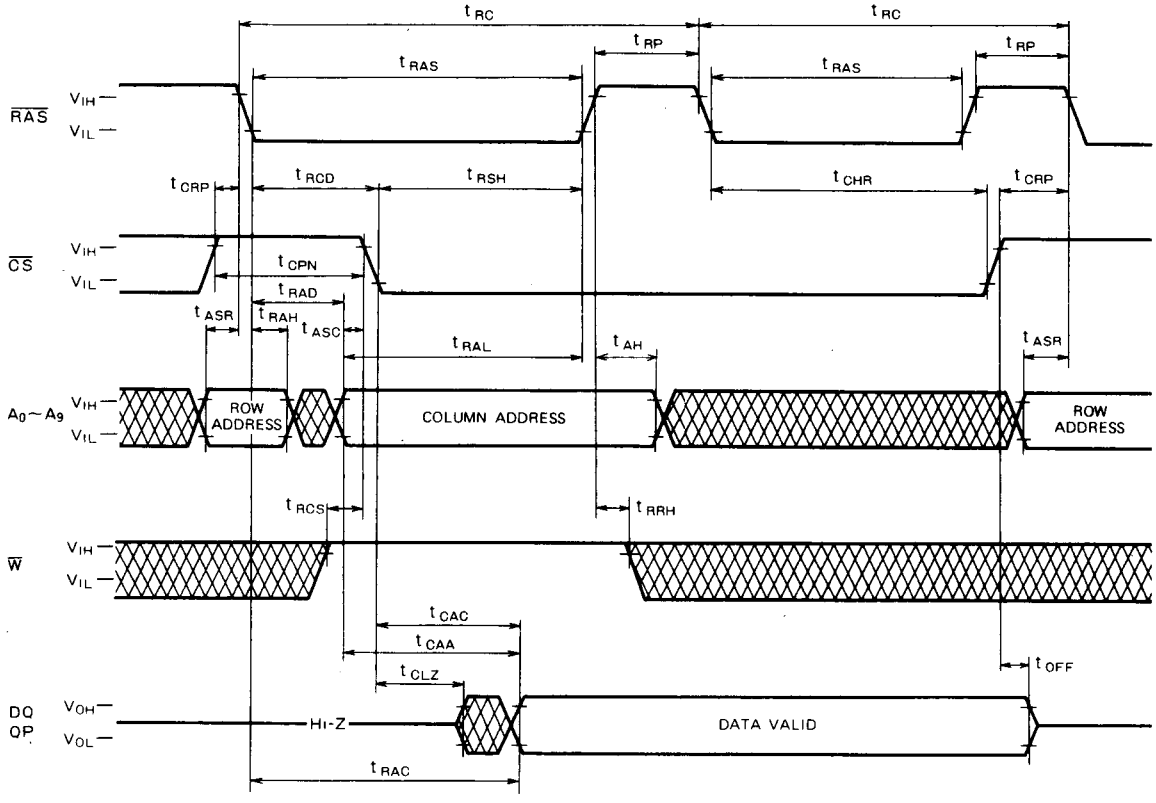

Note 22: $\overline{W}$, DP = don't care, $A_9$ may be $V_{IH}$ or $V_{IL}$.

## $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle (Note 23)

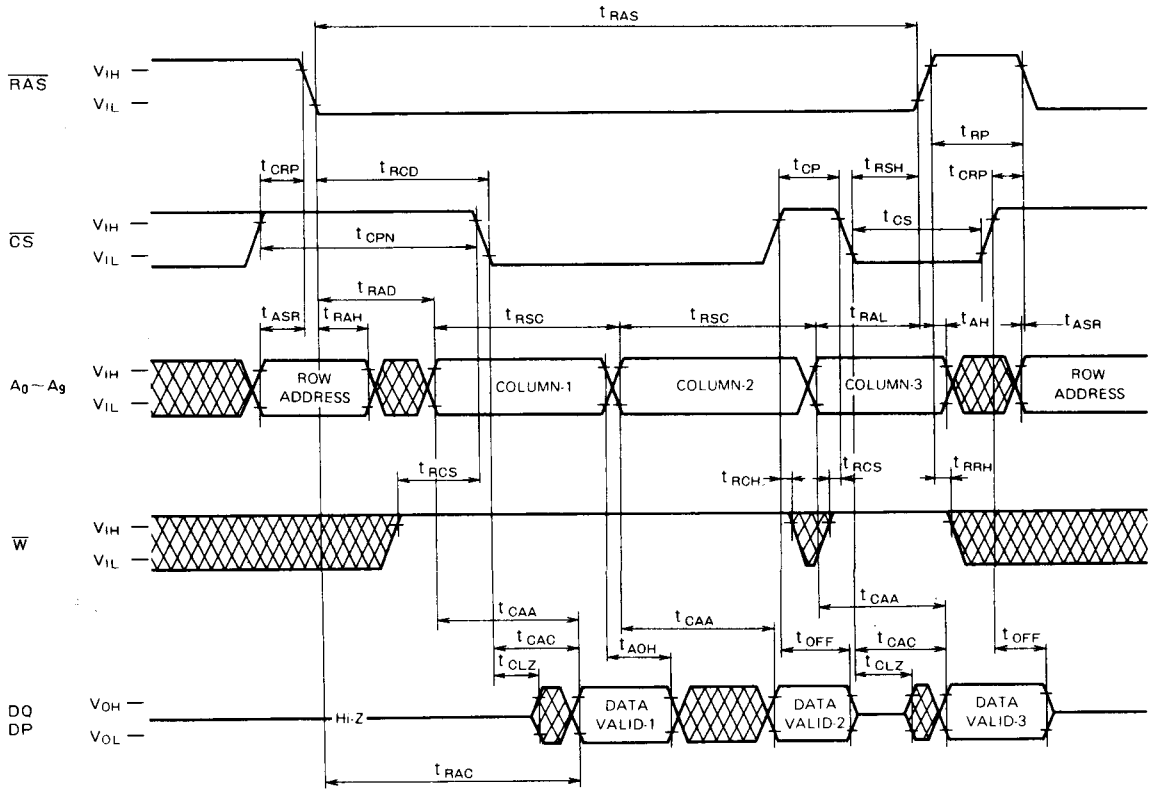



Note 23: $\overline{W}$, DP = don't care

## Hidden Refresh Cycle



## Static Column Mode Read Cycle



## Static Column Mode Early Write Cycle