Features

128Kx8 bits Monolithic CMOS Static Random Access Memory

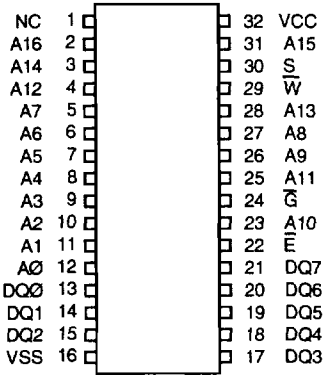
- Fast Access Times:
  70, 85 & 100ns
- Battery Back-up Operation
  2V Data Retention (EDI88130LP)
- $\overline{E}$, S & $\overline{G}$ Functions for Bus Control
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks

JEDEC Pinout

- 32 pin plastic Dual-in-line package, No. 11

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram



Pin Names

AØ-A16	Address Inputs
$\overline{E}$	Chip Enables
S	Chip Select
$\overline{W}$	Write Enable
G	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

128Kx8 Static RAM CMOS, Monolithic

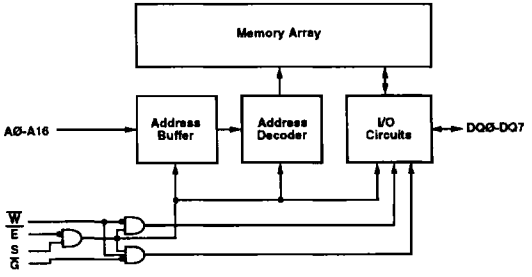
The EDI88130C is a ruggedized plastic, monolithic Static RAM organized as 128Kx8 bits.

The device has two chip enable lines which automatically power down the device when proper logic levels are applied. The second chip select (S) line can be used to provide system memory security during power down in non-battery backed up systems and simplify decoding schemes in memory banking where large multiple pages of memory are required.

Extended temperature testing is performed with the test patterns developed for use on EDI's fully compliant 128Kx8 SRAMs. EDI fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of a device change when it is operated beyond the commercial temperature range. Using commercial test methods will not guarantee a device that operates reliably in the field at temperature extremes. User's of EDI's ruggedized plastic benefit from EDI's extensive experience in characterizing SRAMs for use in military systems.

A low power version, EDI88130LP, offers a 2V data retention function for battery back-up applications.

EDI ensures Low Power devices will retain data in Data Retention mode by characterizing the device to determine the appropriate test conditions. This is crucial for systems operating at -40°C or below and using dense memoires such as 128Kx8s. EDI's ruggedized plastic dip is footprint compatible with EDI's full military ceramic dip EDI88130CXXCB.



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Power Dissipation	1 Watts
Output Current.	40 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$= VIL, II/O = 0mA S=VIH	-- --		95	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH &/or S≤ VIL, VIN≥ VIH or ≤ VIL	--		20	mA
Full Standby Power Supply Current	ICC3	$\overline{E} \geq$ VCC-0.2V&/or S ≤ VCC+0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	2	5	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±5	µA
Output Leakage Current	ILO	V I/O = 0V to VCC, $\overline{E} \geq$ VIH &/or S ≤ VIL	--	--	±5	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

*Typical: TA=25°C, VCC=5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Output Deselect	High Z	ICC1
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	High Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input (Except DQ Pins)	CI	6	pF
Control (DQ Pins)	CD/Q	8	pF

These parameters are sampled, not 100% tested.

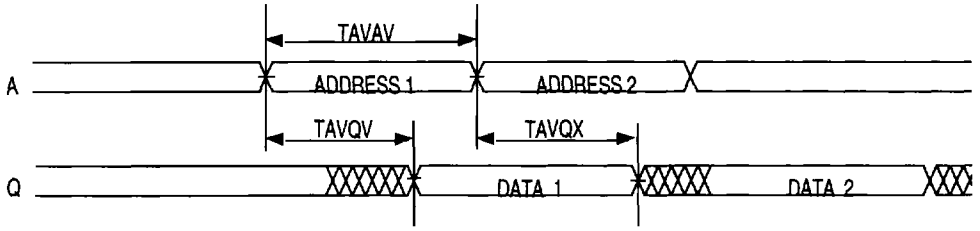
AC Characteristics Read Cycle

Parameter	Symbol JEDEC	Symbol Alt.	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Read Cycle Time	TAVAV	TRC	70		85		100		ns
Address Access Time	TAVQV	TAA		70		85		100	ns
Chip Enable	TELQV	TACS		70		85		100	ns
Access Time	TSHQV	TACS		70		85		100	ns
Chip Enable to	TELQX	TCLZ	3		3		3		ns
Output in Low Z (1)	TSHQX	TCLZ	3		3		3		ns
Chip Disable to	TEHQZ	TCHZ		30		35		40	ns
Output in High Z (1)	TSLQZ	TCHZ		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		35		35		35	ns

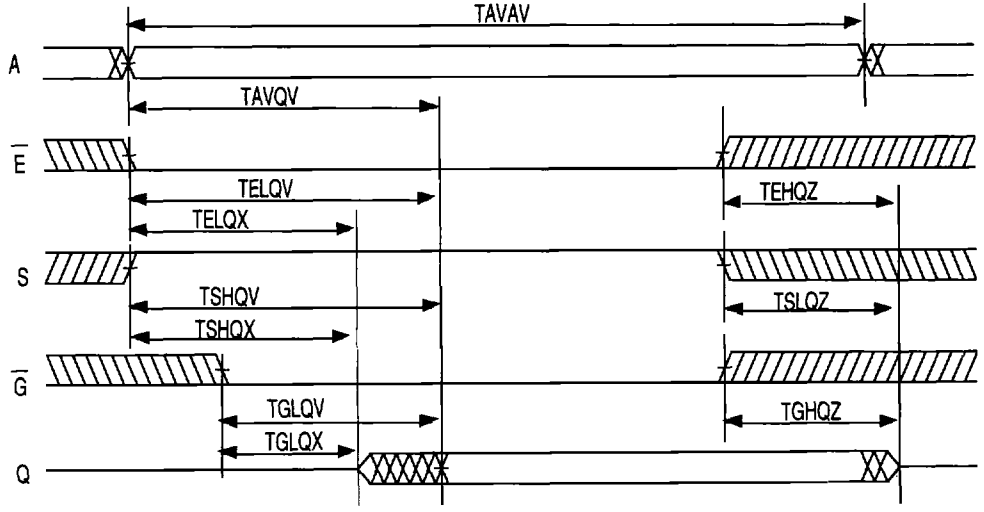
Note 1. Parameter guaranteed, but not tested.

5

Read Cycle 1 - W, S High; G, E Controlled



Read Cycle 2 - W High



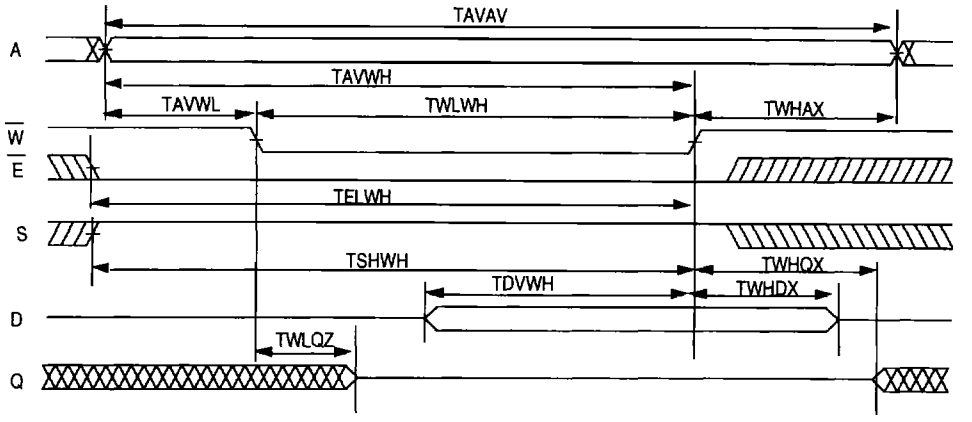
AC Characteristics Write Cycle

Parameter	Symbol JEDEC	Symbol Alt.	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Write Cycle Time	TAVAV	TWC	70		85		100		ns
Chip Enable to	TELWH	TCW	65		70		80		ns
End of Write	TELEH	TCW	65		70		80		ns
	TSHWH	TCW	65		70		80		ns
	TSHSL	TCW	65		70		80		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
	TAVSH	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	65		70		80		ns
Write Pulse Width	TWLWH	TWP	40		70		80		ns
	TWLEH	TWP	40		70		80		ns
	TWLSL	TWP	40		70		80		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
	TSLAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
	TSLDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	35	0	40	ns
Data to Write Time	TDVWH	TDW	30		35		40		ns
	TDVEH	TDW	30		35		40		ns
	TDVSL	TDW	30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		ns

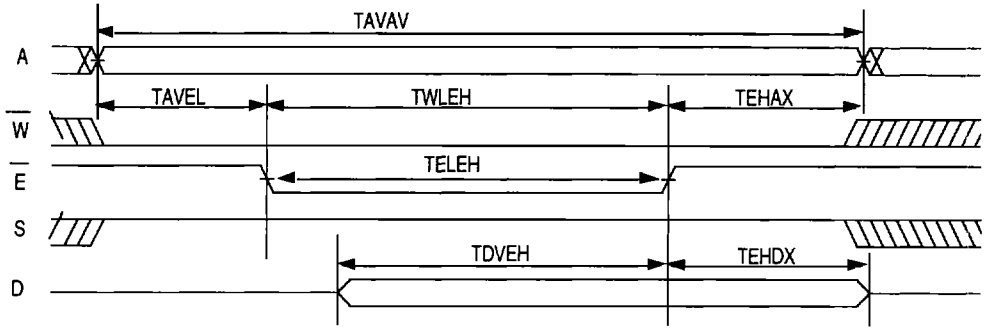
Note 1: Parameter guaranteed, but not tested.

5

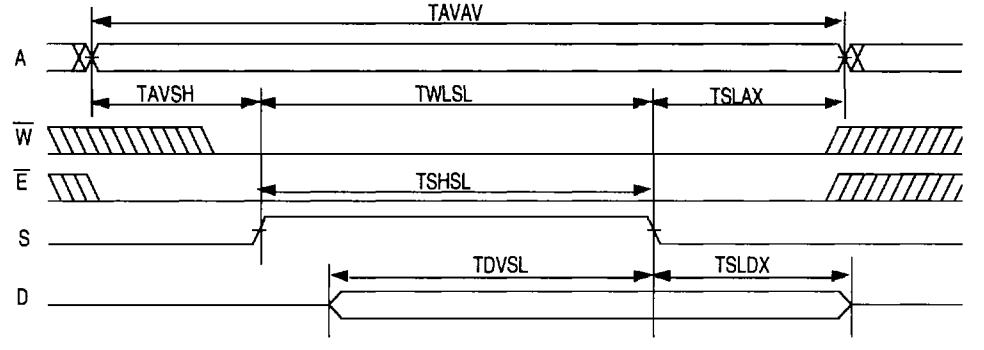
Write Cycle 1 - Late Write, W Controlled



Write Cycle 2 - Early Write, E Controlled



Write Cycle 3 - Early Write, S Controlled



Data Retention Characteristics

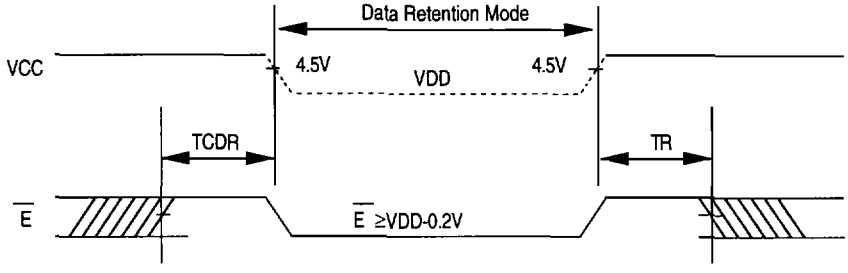
EDI88130LP Only

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥VDD -0.2V&/or S ≤ VSS +0.2V	--	--	400	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥ VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤ 0.2V	TAVAV*	--	--	ns

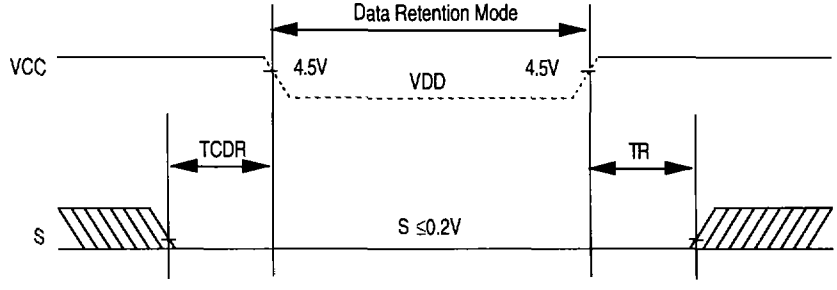
Note 1: Parameter guaranteed, but not tested.

*Read Cycle Time

Data Retention E Controlled



Data Retention S Controlled



5

Ordering Information

Military (-55°C to +125°C)

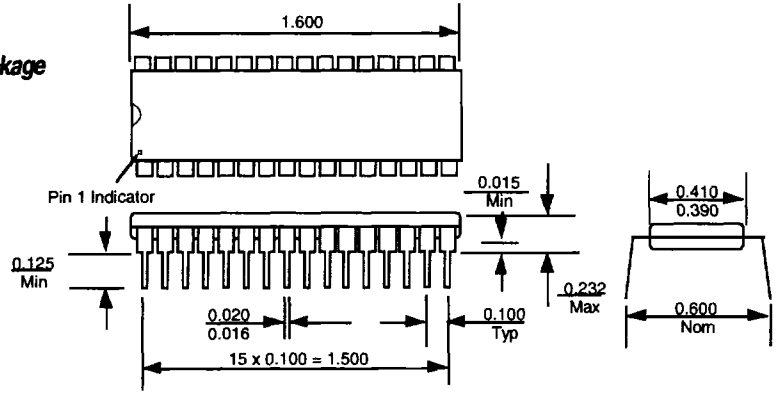
Part No.	Speed ns	Package No.
Standard Power		
EDI88130C70PM	70	11
EDI88130C85PM	85	11
EDI88130C100PM	100	11
Low Power		
EDI88130LP70PM	70	11
EDI88130LP85PM	85	11
EDI88130LP100PM	100	11

Industrial (-40°C to +85°C)

Part No.	Speed ns	Package No.
Standard Power		
EDI88130C70PI	70	11
EDI88130C85PI	85	11
EDI88130C100PI	100	11
Low Power		
EDI88130LP70PI	70	11
EDI88130LP85PI	85	11
EDI88130LP100PI	100	11

Package Description

Package No. 11
32 Pin Plastic
Dual-in-line Package
600 mils wide



Electronic Designs Incorporated
• One Research Drive • Westborough, MA 01581USA • 508-366-5151 • FAX 508-836-4850 •
Electronic Designs Europe Ltd. • Shelley House, The Avenue • Lightwater, Surrey GU18 5RF
United Kingdom • 01276 472637 • FAX: 01276 473748