128Mbit GDDR SDRAM

Revision 0.0
May 2005

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Revision History

Revision	Month	Year	History
0.0	May	2005	- *Target Spec* - Defined target specification

1M x 32Bit x 4 Banks Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL

1.0 FEATURES

- 2.5V ± 5% power supply for device operation
- 2.5V ± 5% power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - -. Read latency 3 (clock)
  - -. Burst length (2, 4, 8)
  - -. Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- Write Interrupted by Read function
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
- Lead free 144pin FBGA package (RoHS compliant)
- Maximum clock frequency up to 250MHz
- Maximum data rate up to 500Mbps/pin

2.0 ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4D263238I-VC40	250MHz	500Mbps/pin	SSTL_2	144FBGA
K4D263238I-VC50	200MHz	400Mbps/pin		

*K4D263238I-GC is the Leaded package part number.

3.0 GENERAL DESCRIPTION

FOR 1M x 32Bit x 4 Bank DDR SDRAM

The K4D263238I is 134,217,728 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 1,048,576 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 2.0GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

4.0 PIN CONFIGURATION (Top View)

	2	3	4	5	6	7	8	9	10	11	12	13
B	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
C	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
D	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
E	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
F	DQ17	DQ16	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ15	DQ14
G	DQ19	DQ18	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ13	DQ12
H	DQS2	DM2	NC	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	NC	DM1	DQS1
J	DQ21	DQ20	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ11	DQ10
K	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
L	$\overline{CAS}$	$\overline{WE}$	VDD	VSS	A10	VDD	VDD	RFU1	VSS	VDD	NC	NC
M	$\overline{RAS}$	NC	NC	BA1	A2	A11	A9	A5	RFU2	CK	$\overline{CK}$	MCL
N	$\overline{CS}$	NC	BA0	A0	A1	A3	A4	A6	A7	A8/AP	CKE	VREF

NOTE:
1. RFU1 is reserved for A12.
2. RFU2 is reserved for BA2.
3. VSS Thermal balls are optional.

PIN DESCRIPTION

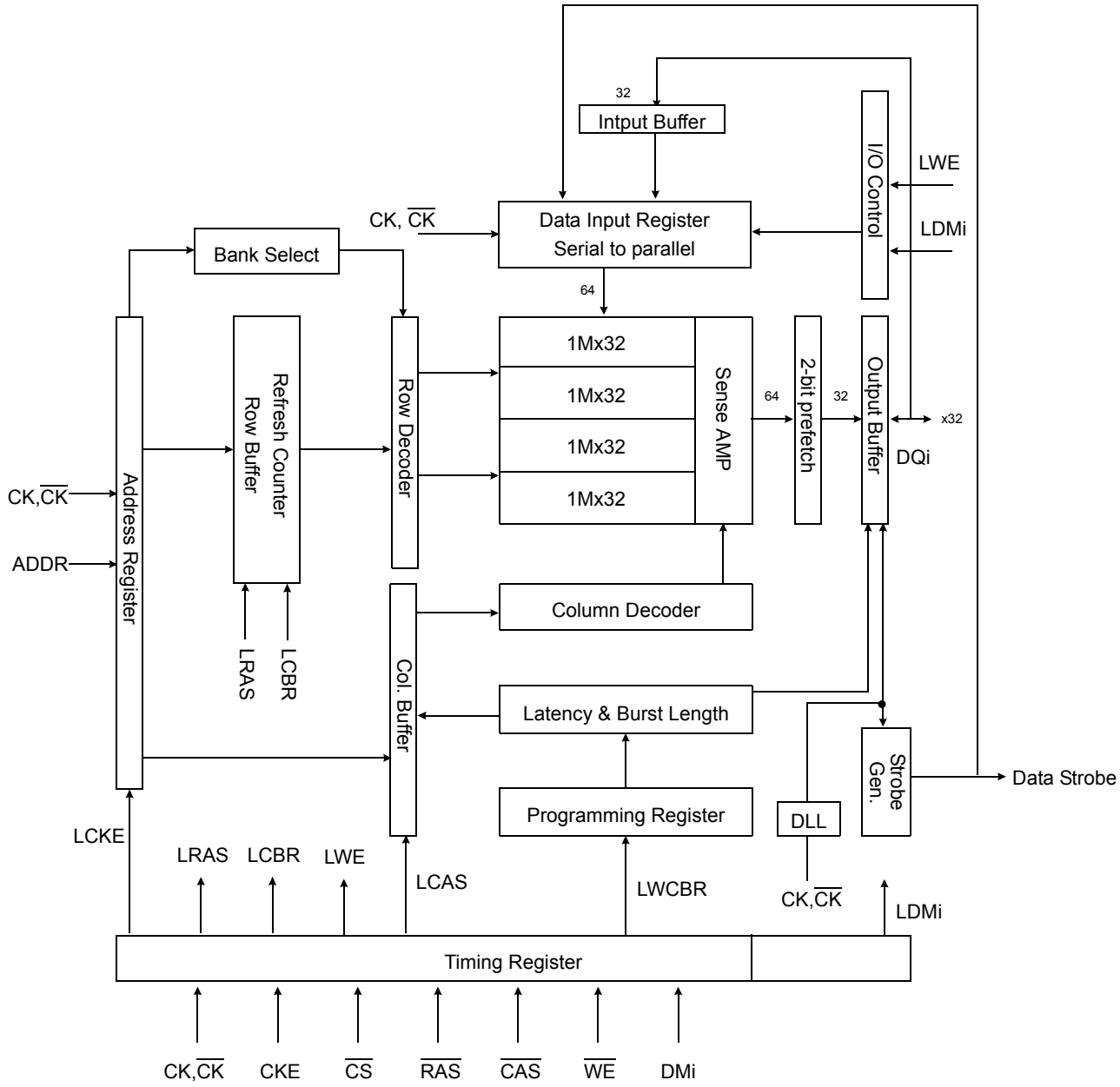
CK,$\overline{CK}$	Differential Clock Input	BA_0, BA_1	Bank Select Address
CKE	Clock Enable	A_0 ~A_{11}	Address Input
$\overline{CS}$	Chip Select	DQ_0 ~ DQ_{31}	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	V_{DDQ}	Power for DQ's
DQS	Data Strobe	V_{SSQ}	Ground for DQ's
DM	Data Mask	NC	No Connection
RFU	Reserved for Future Use	MCL	Must Connect Low

5.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$*1	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input	Latches row addresses on the positive going edge of the CK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Input	Latches column addresses on the positive going edge of the CK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Input	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQS	Input/Output	Data input and output are synchronized with both edge of DQS.
DM_0 ~ DM_3	Input	Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM_0 for DQ_0 ~ DQ_7, DM_1 for DQ_8 ~ DQ_{15}, DM_2 for DQ_{16} ~ DQ_{23}, DM_3 for DQ_{24} ~ DQ_{31}.
DQ_0 ~ DQ_{31}	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA_0, BA_1	Input	Selects which bank is to be active.
A_0 ~ A_{11}	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA_0 ~ RA_{11}, Column addresses : CA_0 ~ CA_7. Column address CA_8 is used for auto precharge.
V_{DD}/V_{SS}	Power Supply	Power and ground for the input buffers and core logic.
V_{DDQ}/V_{SSQ}	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Power Supply	Reference voltage for inputs, used for SSTL interface.
MCL	Must Connect Low	Must connect Low

*1 : The timing reference point for the differential clocking is the cross point of CK and $\overline{CK}$.
For any applications using the single ended clocking, apply V_{REF} to $\overline{CK}$ pin.

6.0 BLOCK DIAGRAM (1Mbit x 32I/O x 4 Bank)



7.0 FUNCTIONAL DESCRIPTION

7.1 Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
   - Apply V_{DD} before V_{DDQ} .
   - Apply V_{DDQ} before V_{REF} & V_{TT}
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,$\overline{CK}$), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL

*1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.

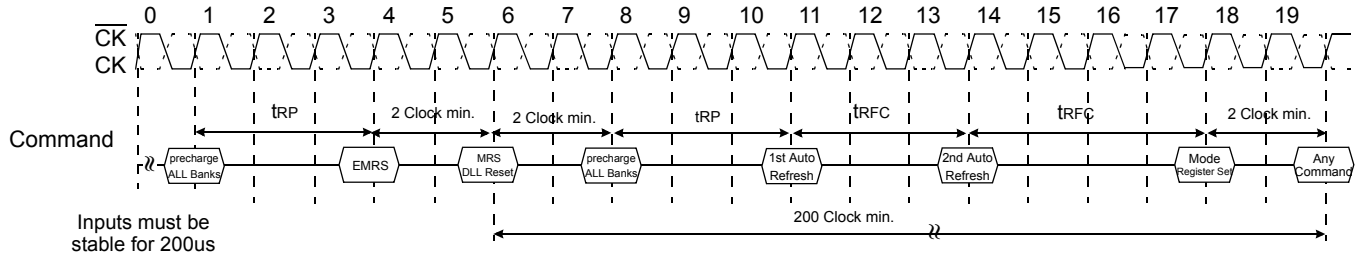
*1,2 7. Issue precharge command for all banks of the device.

8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

*2 Sequence of 6&7 is regardless of the order.

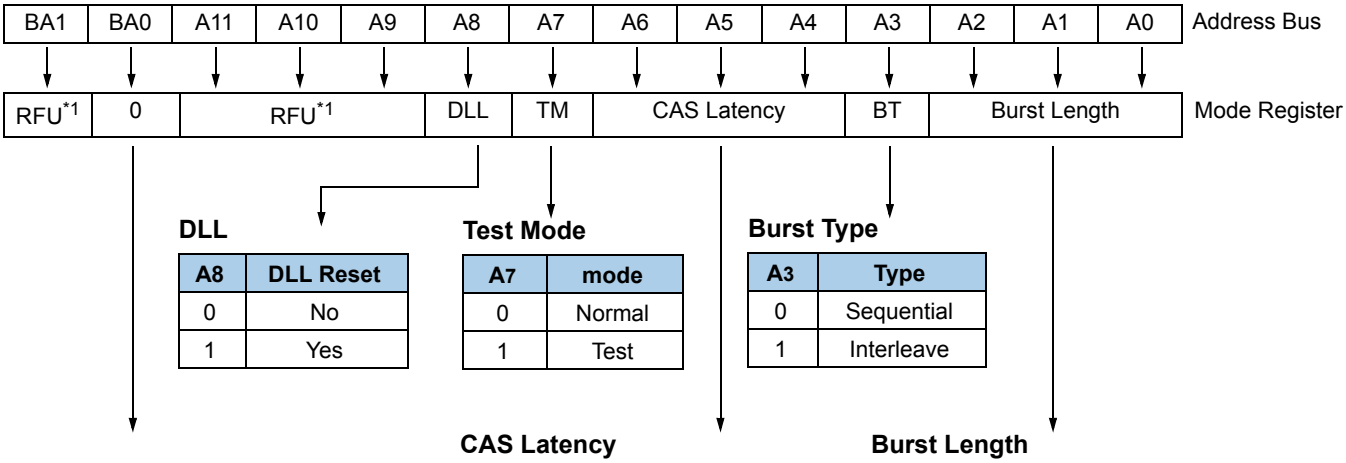
Power up & Initialization Sequence



*** When the operating frequency is changed, DLL reset should be required again.**
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.

7.2 MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$(The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{11} and BA_0, BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, CAS latency(read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_8 is used for DLL reset. A_7,A_8, BA_0 and BA_1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



DLL

A8	DLL Reset
0	No
1	Yes

Test Mode

A7	mode
0	Normal
1	Test

Burst Type

A3	Type
0	Sequential
1	Interleave

BA0	An ~ A0
0	MRS
1	EMRS

*1 : RFU(Reserved for future use)
should stay "0" during MRS cycle.

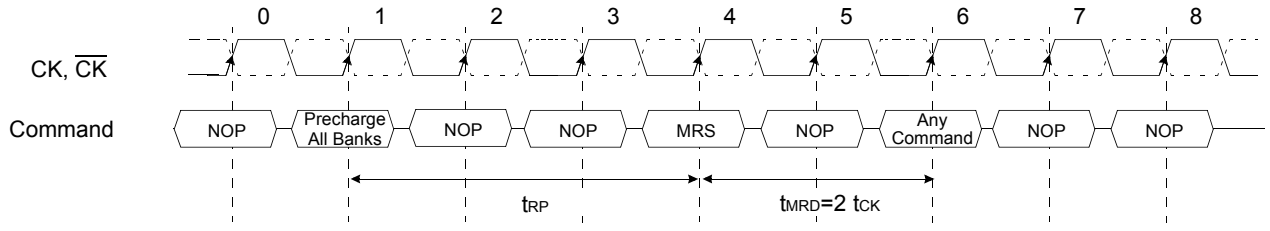
CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Type	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve

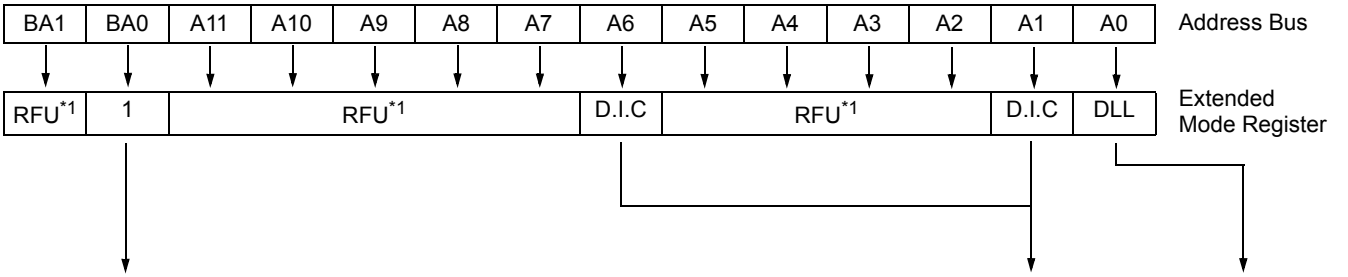
MRS Cycle



*1 : MRS can be issued only at all banks precharge state.
*2 : Minimum tRP is required to issue MRS command.

7.3 EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extend mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A11 and BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the extended mode register. A1 and A6 are used for setting driver strength to weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. “High” on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



BA_0	A_n ~ A_0
0	MRS
1	EMRS

A6	A1	Output Driver Impedence Control	
0	0	Full	100%
0	1	Weak	60%
1	0	N/A	Do not use
1	1	Matched	30%

A_0	DLL Enable
0	Enable
1	Disable

*1 : RFU(Reserved for future use) should stay "0" during EMRS cycle.

8.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9.0 AC & DC OPERATING CONDITIONS

9.1 POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	2.375	2.5	2.625	V	1
Output Supply voltage	V_{DDQ}	2.375	2.5	2.625	V	1
Reference voltage	V_{REF}	0.49*V_{DDQ}	-	0.51*V_{DDQ}	V	2
Termination voltage	V_{tt}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
Input logic high voltage	V_{IH}	V_{REF}+0.15	-	V_{DDQ}+0.30	V	4
Input logic low voltage	V_{IL}	-0.30	-	V_{REF}-0.15	V	5
Output logic high voltage	V_{OH}	V_{tt}+0.76	-	-	V	I_{OH}=-15.2mA
Output logic low voltage	V_{OL}	-	-	V_{tt}-0.76	V	I_{OL}=+15.2mA
Input leakage current	I_{IL}	-5	-	5	uA	6
Output leakage current	I_{OL}	-5	-	5	uA	6

Note :
1. Under all conditions VDDQ must be less than or equal to VDD.
2. V_{REF} is expected to equal 0.50*VDDQ of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the VREF may not exceed ± 2% of the DC value. Thus, from 0.50*VDDQ, VREF is allowed ± 25mV for DC error and an additional ± 25mV for AC noise.
3. Vtt of the transmitting device must track VREF of the receiving device.
4. VIH(max.)= VDDQ +1.5V for a pulse and it which can not be greater than 1/3 of the cycle rate.
5. VIL(min.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
6. For any pin under test input of 0V ≤ VIN ≤ VDD is acceptable. For all other pins that are not under test VIN=0V.

9.2 DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted (TA=0 to 65°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-40	-50		
Operating Current (One Bank Active)	I_{CC1}	Burst Lenth=2 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA, t_{CC}= t_{CC}(min)	TBD	TBD	mA	1, 2
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	TBD	TBD	mA	1, 2
Precharge Standby Current in Non Power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC}= t_{CC}(min).	TBD	TBD	mA	1, 2
Active Standby Current power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	TBD	TBD	mA	1, 2
Active Standby Current in in Non Power-down mode	I_{CC3N}	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), t_{CC}= t_{CC}(min) .	TBD	TBD	mA	1, 2
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA ,t_{CC}= t_{CC}(min), Page Burst, All Banks activated.	TBD	TBD	mA	1, 2
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RFC}$(min)	TBD	TBD	mA	1, 2,3
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	TBD		mA	1, 2

Note :
1. Measured with output open.
2. Current meassured at V_{DD}(max).
3. Refresh period is 32ms.

9.3 AC INPUT OPERATING CONDITIONS

Recommended operating conditions(Voltage referenced to V_{SS}=0V, V_{DD}/ V_{DDQ}=2.5V± 5%, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V_{IH}	V_{REF}+0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V_{IL}	-	-	V_{REF}-0.35	V	
Clock Input Differential Voltage; CK and $\overline{CK}$	V_{ID}	0.7	-	V_{DDQ}+0.6	V	1
Clock Input Crossing Point Voltage; CK and $\overline{CK}$	V_{IX}	0.5*V_{DDQ}-0.2	-	0.5*V_{DDQ}+0.2	V	2

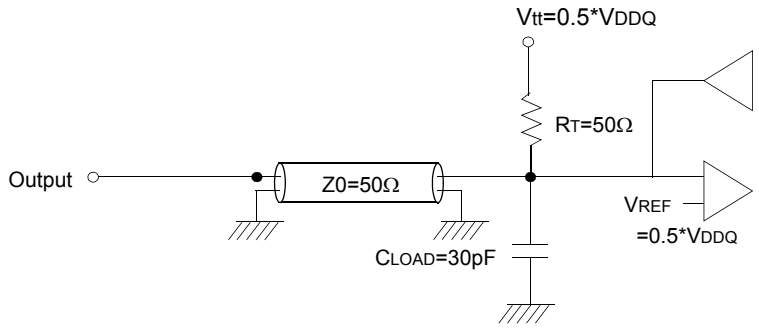
Note :
1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

9.4 AC OPERATING TEST CONDITIONS

(VDD/ VDDQ=2.5V± 5% , TA= 0 to 65°C)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	0.50*V_{DDQ}	V	1
CK and $\overline{CK}$ signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.35/V_{REF}-0.35	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Fig.1		

Note 1 : In case of differential clocks(CK and $\overline{CK}$), input reference voltage for clock is a CK and $\overline{CK}$'s crossing point.



(Fig. 1) Output Load Circuit

9.5 CAPACITANCE

(VDD=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, $\overline{CK}$)	C_{IN1}	1.0	5.0	pF
Input capacitance(A_0~A_{11}, BA_0~BA_1)	C_{IN2}	1.0	4.0	pF
Input capacitance(CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN3}	1.0	4.0	pF
Data & DQS input/output capacitance(DQ_0~DQ_{31})	C_{OUT}	1.0	6.0	pF
Input capacitance(DM0 ~ DM3)	C_{IN4}	1.0	6.0	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	0.1 + 0.01	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 + 0.01	uF

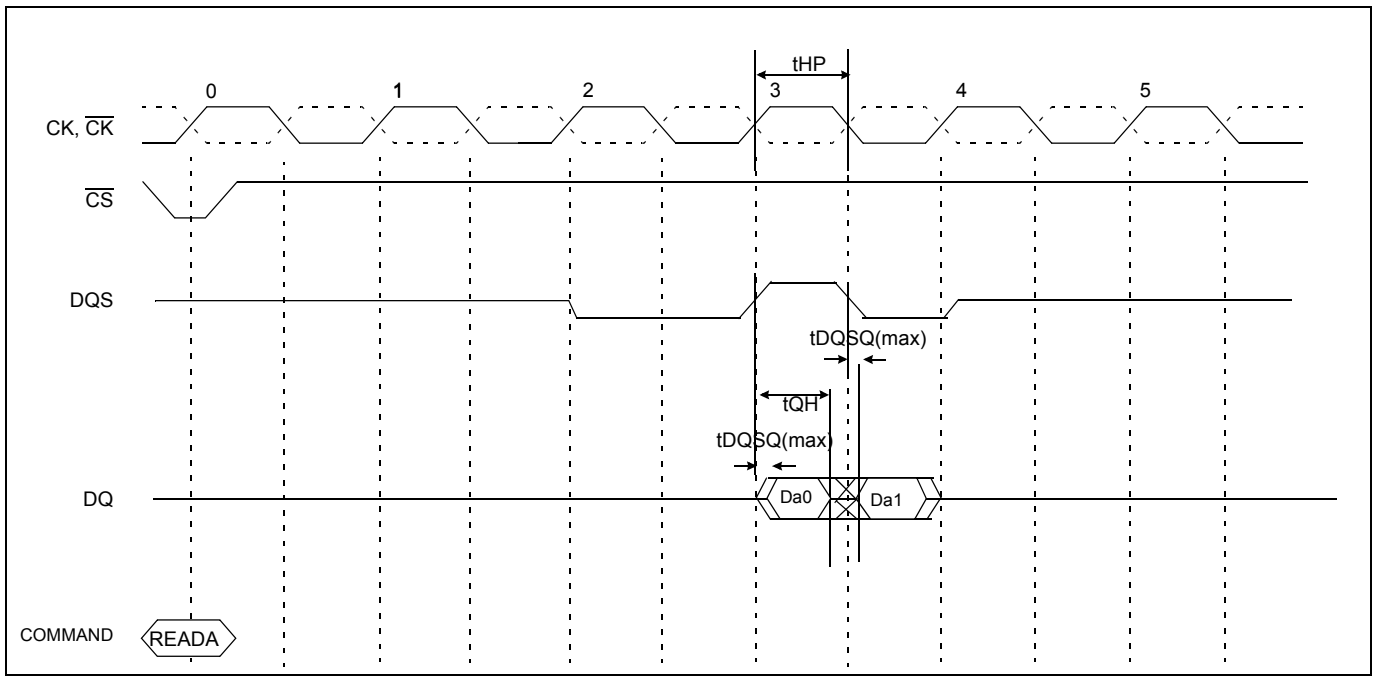
1. V_{DD} and V_{DDQ} pins are separated each other. All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. V_{SS} and V_{SSQ} pins are separated each other. All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

9.6 AC CHARACTERISTICS

Parameter		Symbol	-40		-50		Unit	Note
			Min	Max	Min	Max		
CK cycle time	CL=3	tCK	4.0	10	5.0	10	ns	
CK high level width		tCH	0.45	0.55	0.45	0.55	tCK	
CK low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQS out access time from CK		tDQSCK	-0.6	0.6	-0.7	+0.7	ns	
Output access time from CK		tAC	-0.6	0.6	-0.7	+0.7	ns	
Data strobe edge to Dout edge		tDQSQ	-	0.4	-	+0.45	ns	
Read preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.85	1.15	0.8	1.2	tCK	
DQS-In setup time		tWPRES	0	-	0	-	ns	
DQS-in hold time		tWPREH	0.35	-	0.25	-	tCK	
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	
DQS-In high level width		tDQSH	0.4	0.6	0.4	0.6	tCK	
DQS-In low level width		tDQSL	0.4	0.6	0.4	0.6	tCK	
Address and Control input setup		tIS	0.9	-	1.0	-	ns	
Address and Control input hold		tIH	0.9	-	1.0	-	ns	
DQ and DM setup time to DQS		tDS	0.4	-	0.45	-	ns	
DQ and DM hold time to DQS		tDH	0.4	-	0.45	-	ns	
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data output hold time from DQS		tQH	tHP-0.4	-	tHP-0.45	-	ns	

Note 1 :
- The JEDEC DDR specification currently defines the output data valid window(tDV) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of tDV(=0.35tCK) artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, tQH which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces tDV
- tQHmin = tHP-X where
  . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)
  . X=A frequency dependent timing allowance account for tDQSQmax

tQH Timing (CL3, BL2)



AC CHARACTERISTICS (I)

Parameter	Symbol	-40		-50		Unit	Note
		Min	Max	Min	Max		
Row cycle time	tRC	48	-	50	-	ns	2,5
Refresh row cycle time	tRFC	56	-	55	-	ns	5
Row active time	tRAS	32	100K	35	100K	ns	5
$\overline{RAS}$ to $\overline{CAS}$ delay for Read	tRCDRD	16	-	15	-	ns	5
$\overline{RAS}$ to $\overline{CAS}$ delay for Write	tRCDWR	8		10		ns	4
Row precharge time	tRP	16	-	15	-	ns	5
Row active to Row active	tRRD	12	-	15	-	ns	5
Last data in to Row precharge	tWR	18	-	20	-	ns	5
Last data in to Row precharge @Auto Precharge	tWR_A	3	-	3	-	tCK	3
Auto precharge write recovery + Precharge	tDAL	7	-	6	-	tCK	3,5
Last data in to Read command	tCDLR	2	-	2	-	tCK	1
Col. address to Col. address	tCCD	1	-	1	-	tCK	
Mode register set cycle time	tMRD	2	-	2	-	tCK	
Exit self refresh to read command	tXSR	200	-	200	-	tCK	
Power down exit time	tPDEX	3tCK+tIS	-	3tCK+tIS	-	ns	
Refresh interval time	tREF	7.8	-	7.8	-	us	

Note :
1. For normal write operation, even numbers of Din are to be written inside DRAM.
2. The number of clock of tRP is restricted by the number of clock of tRAS and tRP.
3. The number of clock of tWR_A is fixed. It can't be changed by tCK.
4. tRCDWR is equal to tRCDRD-2tCK and the number of clock can not be lower than 2tCK.
5. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer unconditionally.

AC CHARACTERISTICS (II)

(Unit : Number of Clock)

K4D263238I-VC40

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
250MHz (4.0ns)	3	12	14	8	4	2	4	3	7	tCK
200MHz (5.0ns)	3	10	11	7	3	2	3	3	6	tCK
166MHz (6.0ns)	3	9	9	6	3	2	3	2	6	tCK

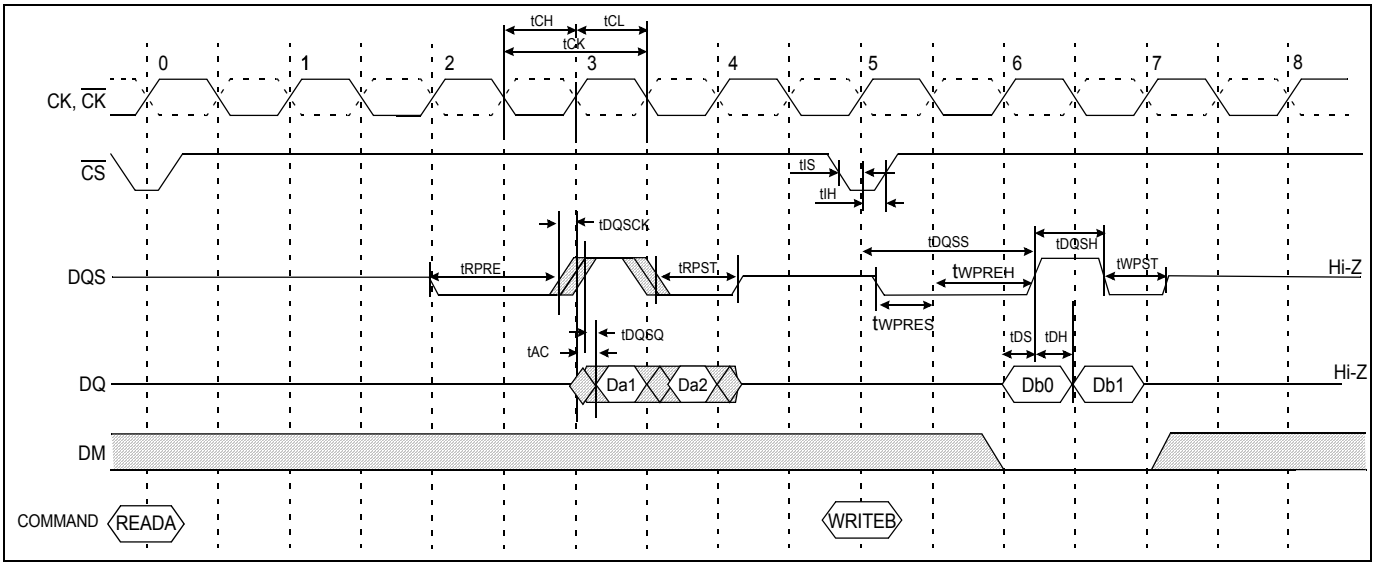
K4D263238I-VC50

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
200MHz (5.0ns)	3	10	11	7	3	2	3	3	6	tCK
166MHz (6.0ns)	3	9	9	6	3	2	3	2	6	tCK

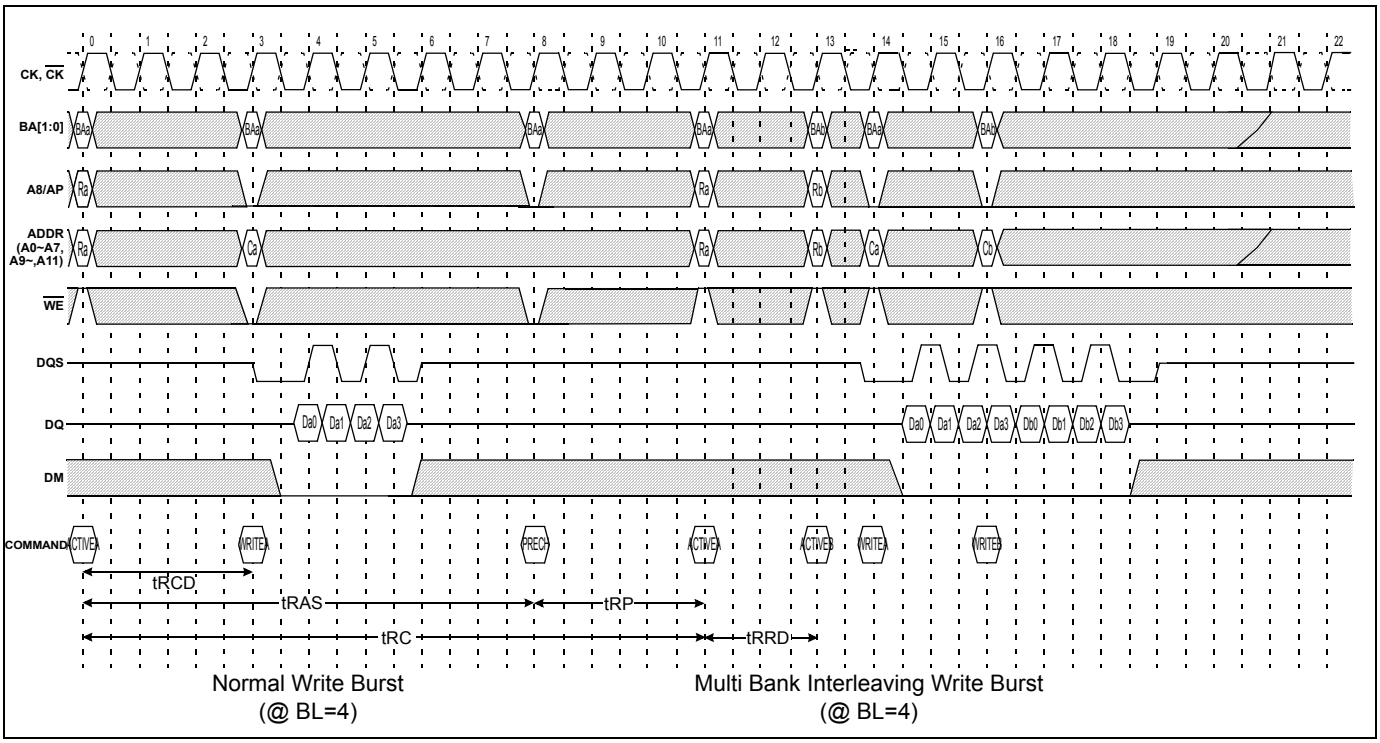
* 200/166MHz are supported in K4D263238I-VC40
* 166MHz is supported in K4D263238I-VC50

10.0 SIMPLIFIED TIMING

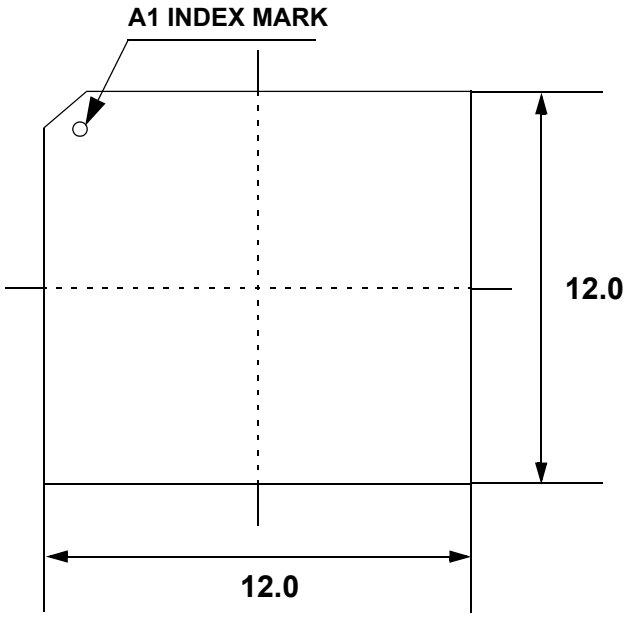
Simplified Timing @ BL=2, CL=3



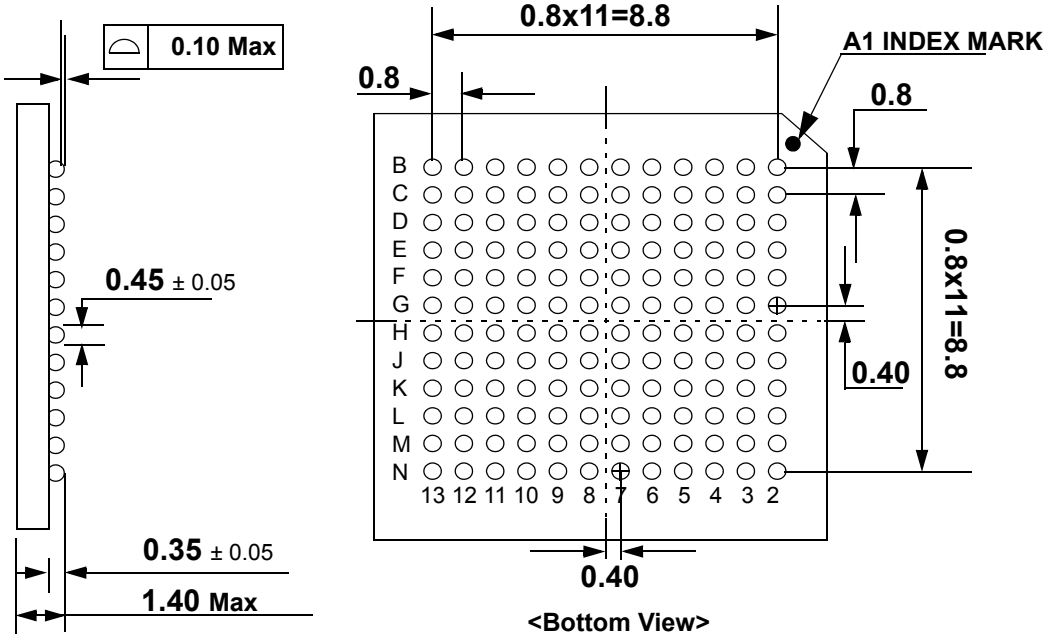
Simplified Timing(2) @ BL=4, CL=3



11.0 PACKAGE DIMENSIONS (144-Ball FBGA)



<Top View>



<Bottom View>

Unit : mm