19-2565; Rev 3; 6/05

5Gbps PC Board Equalizer

General Description

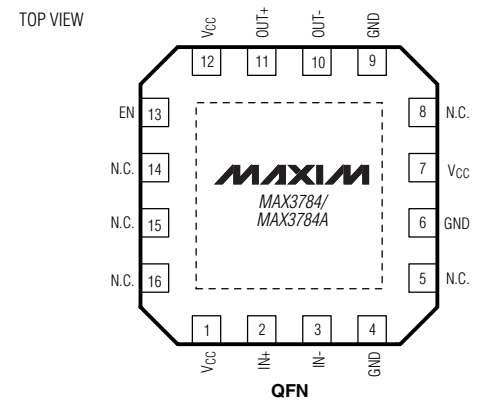
The MAX3784/MAX3784A 5Gbps equalizers provide compensation for transmission-medium losses in up to 40in of FR4. They are optimized for short-run length and balanced codes such as 8b10b, as found in multiplexed 1.25Gbps Ethernet systems and 4.25Gbps Fibre Channel.

The equalizers use differential CML data inputs and outputs. A standby mode reduces power consumption when the parts are not in use. The MAX3784/MAX3784A are available in a 4mm × 4mm, 16-pin QFN package that consumes only 185mW at +3.3V.

Features

- ♦ **Spans 40in (1m) of FR4 PC Board**
- ♦ **0.18UI Deterministic Jitter Up to 40in**
- ♦ **Low Power Consumption: 185mW (MAX3784)**
- ♦ **Equalization Reduces Intersymbol Interference**
- ♦ **Single +3.3V Supply**
- ♦ **Standby Mode**
- ♦ **Small 4mm × 4mm, 16-Pin QFN Package**

Pin Configurations



QFN

NOTE: THE EXPOSED PAD MUST BE SOLDERED TO SUPPLY GROUND FOR CORRECT THERMAL AND ELECTRICAL PERFORMANCE.

Pin Configurations continued at end of data sheet.

Applications

Chassis Life Extension

4.25Gbps Fibre Channel

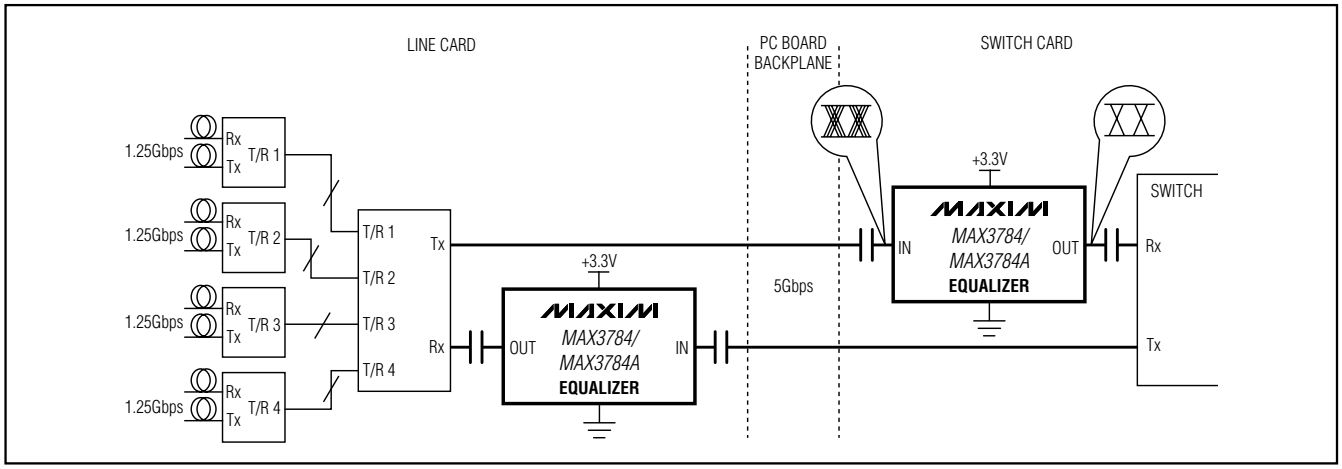
4x Multiplexed 1.25Gbps Ethernet (5Gbps)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3784UTE	0°C to +85°C	16 QFN	G1644-1
MAX3784UTE+	0°C to +85°C	16 TQFN	T1644-4
MAX3784AUTE	0°C to +85°C	16 QFN	G1644-1
MAX3784AUTE+	0°C to +85°C	16 TQFN	T1644-4

+Denotes lead-free package.

Typical Application Circuit



5Gbps PC Board Equalizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +6V
Input Voltage.....(-0.5V) to (V_{CC} + 0.5V)
Continuous Output Current.....-25mA to +25mA
Continuous Power Dissipation (T_A = +85°C)
16-Pin QFN (derate 25mW/°C above +85°C) 1600mW
Operating Ambient Temperature Range .....0°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Power		EN = low					30	mW
		EN = high				185	250	
Supply-Noise Tolerance		(Note 1)	10Hz < f < 100Hz			100		mV_{P-P}
			100Hz < f < 1MHz			40		
			1MHz < f < 2.5GHz			10		
Latency		From input to output				200		ps
CML RECEIVER INPUT								
Input Voltage Swing	V_{IN}	Measured differentially at point A in Figure 1			400		1000	mV_{P-P}
Return Loss		100MHz to 2.5GHz				15		dB
Input Resistance		Differential			80	100	120	Ω
EQUALIZATION								
Residual Deterministic Jitter, 5Gbps		Table 1 (Notes 2–5)	20in			0.13	0.21	UI_{P-P}
			40in			0.18	0.23	
Residual Deterministic Jitter, 2.5Gbps		Table 1 (Notes 2–5)	20in			0.08	0.14	UI_{P-P}
			40in			0.13	0.28	
Residual Deterministic Jitter, 1.25Gbps		Table 1 (Notes 2–5)	20in			0.04	0.07	UI_{P-P}
			40in			0.07	0.15	
Random Jitter		(Notes 5, 6)				1.3	1.9	ps_{RMS}
CML TRANSMITTER OUTPUT (into 100Ω ±1Ω)								
Output Voltage Swing	V_O	Differential swing, measured differentially at point C in Figure 1		MAX3784	400		600	mV_{P-P}
				MAX3784A	550		750	
Transition Time	t_f, t_r	20% to 80% (Notes 5, 8)			30	45	60	ps
Output Resistance		Single ended			40	50	60	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE CONTROL PIN						
Input High Voltage			1.5			V
Input Low Voltage					0.5	V
Input High Current		(Note 7)	-150		+10	µA
Input Low Current		(Note 7)	-150		+10	µA

Note 1: Allowed supply noise during jitter tests.

Note 2: Test pattern. This is a combination of K28.5± characters running at the full bit rate and at one-quarter the bit rate. This simulates the multiplexing of four each 1.25Gbps Ethernet data streams.

Pattern (hex) 100 bits	
00 FFFF F0F0 FF 0000 0F0F 3EB05	(quarter rate K28.5+, quarter rate K28.5-) (K28.5± 00 1111 1010 11 0000 0101)

Note 3: Difference in deterministic jitter between reference points A and C in Figure 1.

Note 4: Signal source amplitude range is 400mV$_{P-P}$ to 1000mV$_{P-P}$ differential. Signal is applied differentially at point A as shown in Figure 1. The deterministic jitter at point B must be from media-induced loss and not from clock-source modulation. Deterministic jitter is measured at the 50% vertical level of the signal at point C.

Note 5: Guaranteed by design and characterization.

Note 6: Test pattern is K28.5 with 40in trace.

Note 7: On-chip pullup resistor of 40kΩ (typ). Negative current indicates equalizer sources current.

Note 8: Using 00 0001 1111 or equivalent pattern. Measured over entire input voltage range, max and min media loss and within 2in of output pins.

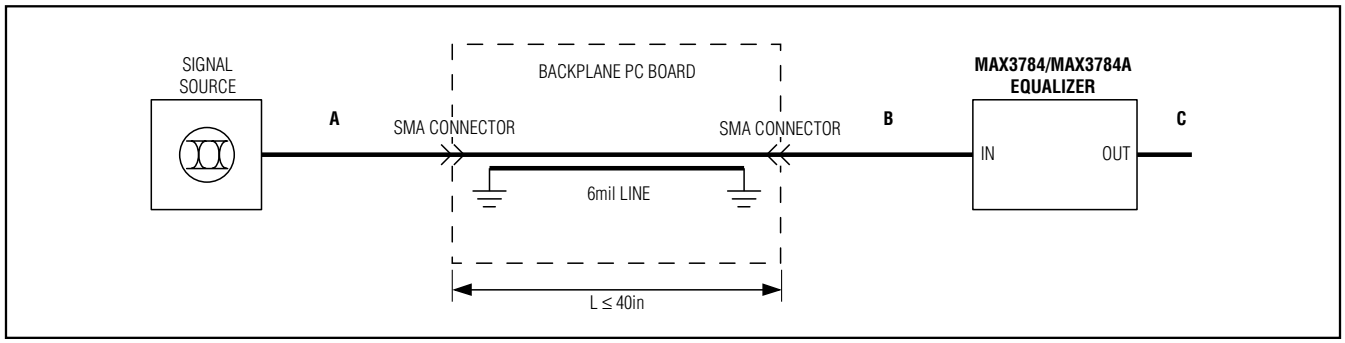


Figure 1. Test Conditions

Table 1. PC Board Assumptions (PC board material is FR4)

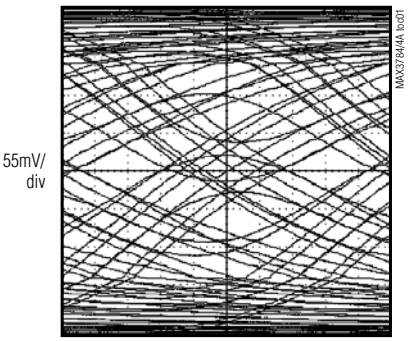
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmission Line	Edge-coupled stripline		6		mils
Relative Permittivity	FR4 or similar	4.4		4.5	—
Loss Tangent	FR4 or similar	0.02		0.022	—
Metal Thickness	0.7 mils (0.5oz copper)		0.7		mils
Impedance	Differential	90	100	110	Ω

5Gbps PC Board Equalizer

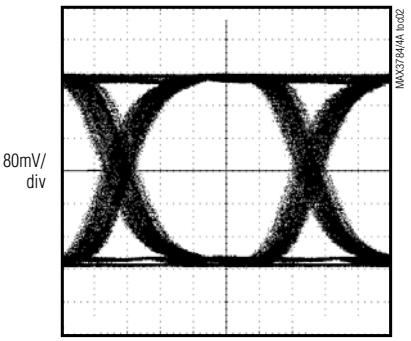
Typical Operating Characteristics

(V_{CC} = +3.3V, measurements done at 5Gbps, 800mV$_{P-P}$ board input with 100-bit pattern from Note 2 of the *EC Table*, T_A = +25°C, unless otherwise noted.)

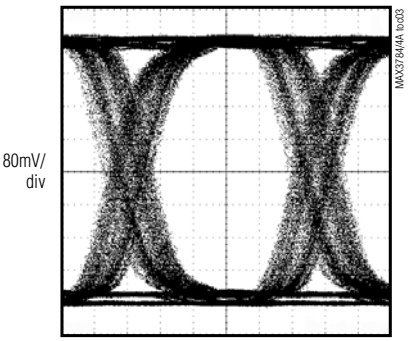
EQUALIZER INPUT EYE DIAGRAM BEFORE EQUALIZATION AT 5Gbps (40in, FR4, 6mil STRIPLINE)



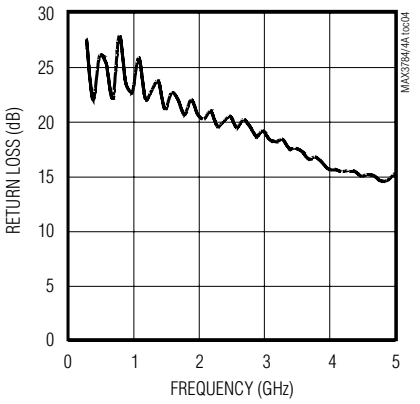
EQUALIZER OUTPUT EYE DIAGRAM AFTER EQUALIZATION AT 5Gbps (40in, FR4, 6mil STRIPLINE, MAX3784)



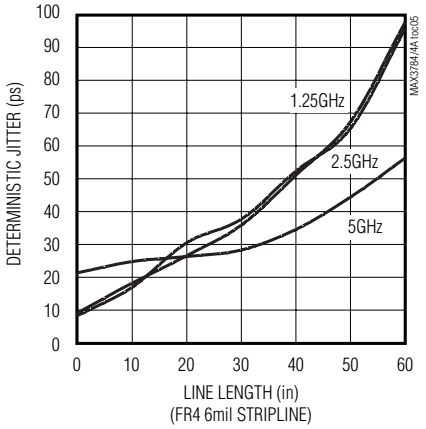
EQUALIZER OUTPUT EYE DIAGRAM AFTER EQUALIZATION AT 5Gbps (40in, FR4, 6mil STRIPLINE, MAX3784A)



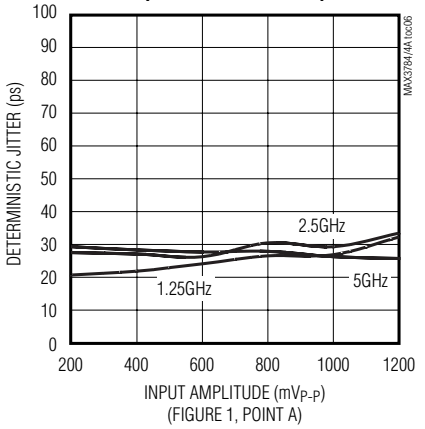
DIFFERENTIAL RETURN LOSS



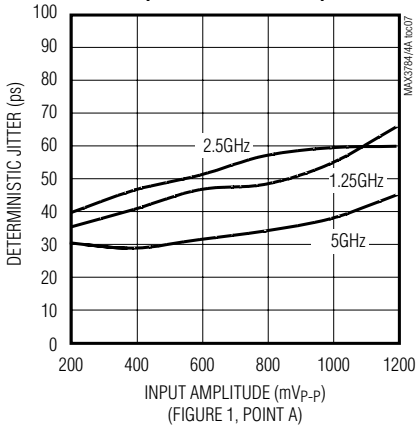
DETERMINISTIC JITTER vs. LINE LENGTH



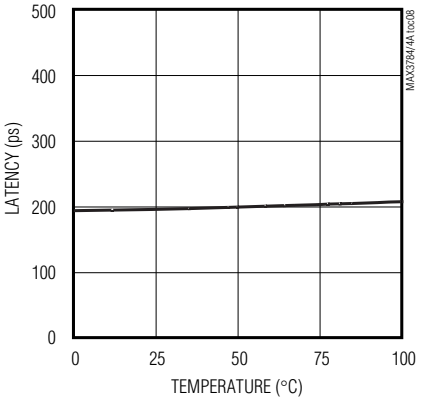
DETERMINISTIC JITTER vs. AMPLITUDE (20in FR4 STRIPLINE)



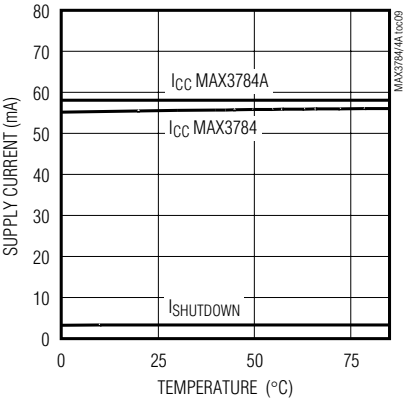
DETERMINISTIC JITTER vs. AMPLITUDE (40in FR4 STRIPLINE)



LATENCY vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 7, 12	V_{CC}	+3.3V Supply Voltage
2	IN+	Positive Input, CML
3	IN-	Negative Input, CML
4, 6, 9	GND	Supply Ground
5, 8, 14, 15, 16	N.C.	No Connection. Leave unconnected.
10	OUT-	Negative Output, CML
11	OUT+	Positive Output, CML
13	EN	Enable Equalizer. A logic high or open selects normal operation. A logic low selects low-power standby mode.
EP	Exposed Pad	Connect to Ground. The exposed pad must be soldered to the circuit board ground plane for proper thermal and electrical performance.

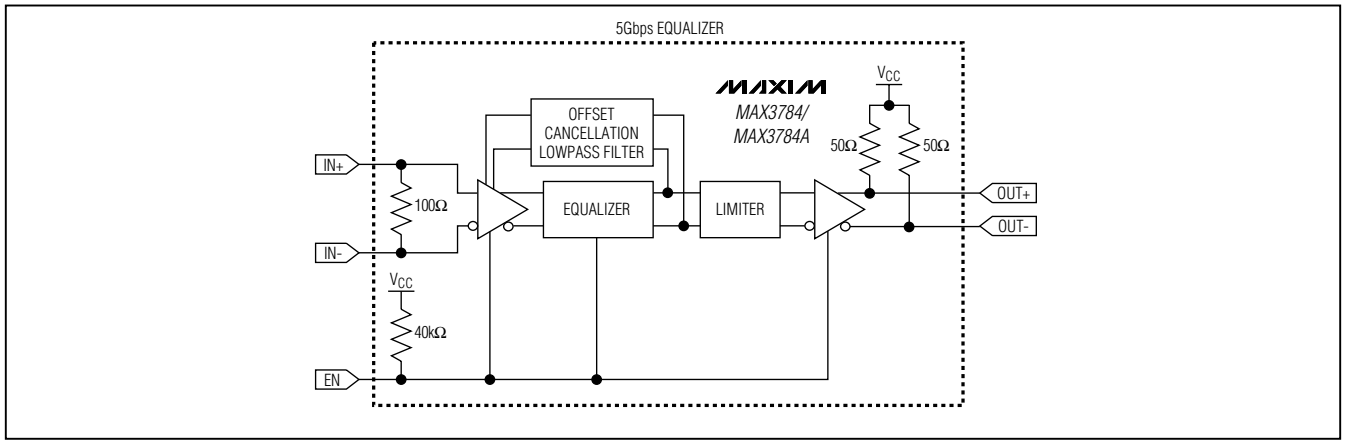


Figure 2. Functional Diagram

Detailed Description

General Theory of Operation

The MAX3784/MAX3784A adaptive equalizers extend the reach of transmission lines in high-frequency backplane interconnect applications. They can be used for 4.25Gbps Fibre Channel, 4x 1.25Gbps Ethernet (5Gbps) and other NRZ, 8b10b or short (≤ 20 bits) CID data types. Internally, the MAX3784/MAX3784A are comprised of an equalizer control loop and limiting output driver. The equalizer block reduces intersymbol interference (ISI), compensating for frequency-dependent media-induced loss. The equalization control detects the spectral contents of the input signal and provides a control voltage to the equalizer core, adapting it to different media. The equalizer operation is optimized for short-run, DC-balanced transmission codes.

Standby Mode

Standby saves power when the equalizer is not in use. The EN logic input must be set high or open for normal operation. Logic low at EN forces the equalizer into the standby state.

CML Input and Output Buffers

The input and output buffers are implemented using current-mode logic (CML). Equivalent circuits are shown in Figures 3 and 4. For details on interfacing with CML, see Maxim Application Note HFAN-1.0: *Interfacing Between CML, PECL, and LVDS*. The common-mode voltage of the input and output is above +2.5V. AC-coupling capacitors are required when interfacing this part with devices terminated in voltages such as +1.8V. Values of 0.10µF or greater are recommended.

5Gbps PC Board Equalizer

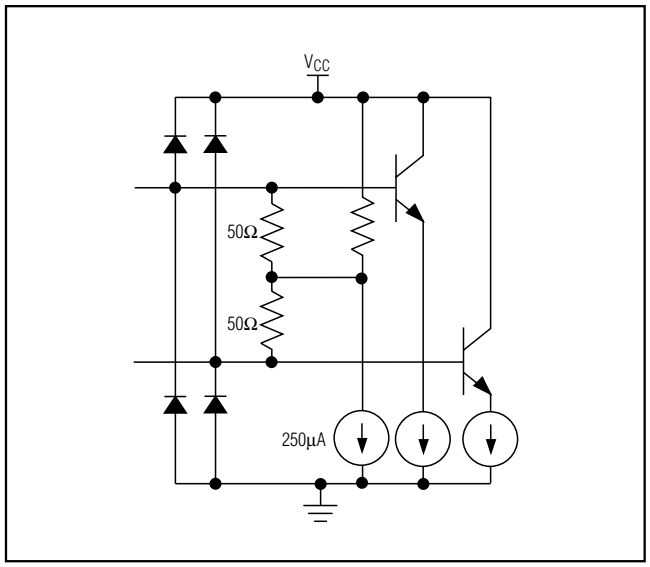


Figure 3. CML Input Equivalent Circuit

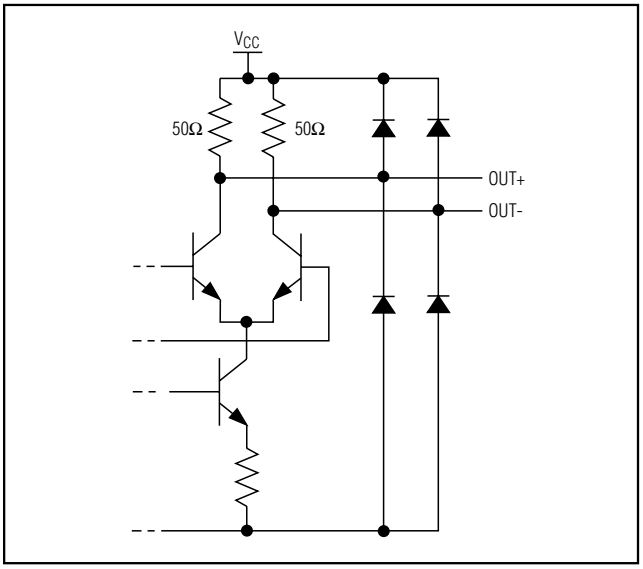


Figure 4. CML Output Equivalent Circuit

Applications Information

Alternate Data Rates

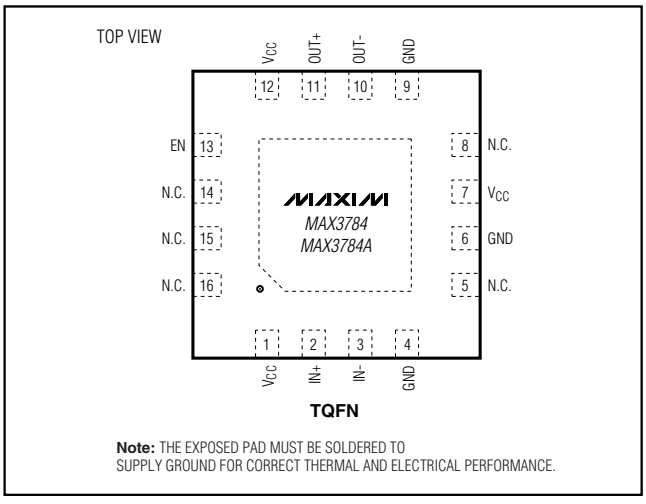
The MAX3784/MAX3784A is optimized for automatic operation at 5Gbps. Equalization at other data rates, such as 1.25Gbps and 2.5Gbps, is possible. See the *Typical Operating Characteristics* for Deterministic Jitter vs. Line Length and Deterministic Jitter vs. Amplitude for typical performance at these data rates.

Layout Considerations

Circuit board layout and design can significantly affect the MAX3784/MAX3784As' performance. Use good high-frequency design techniques, including minimizing ground inductance and connections and using controlled-impedance transmission lines for the high-frequency data signals. Route signals differentially to reduce EMI susceptibility and crosstalk. Solder the exposed pad to supply ground for proper thermal and electrical operation.

Place power-supply decoupling capacitors as close as possible to the V_{CC} pins.

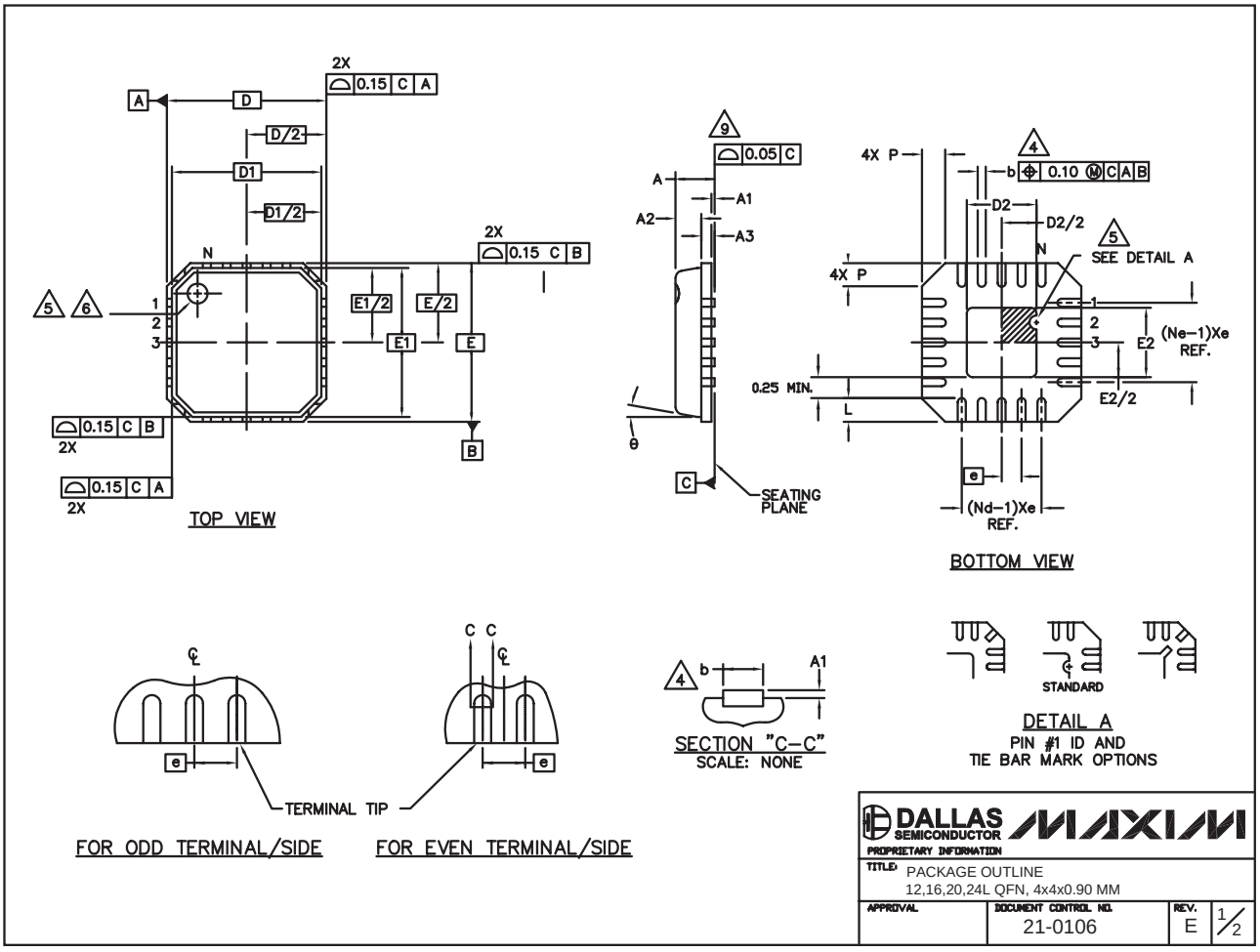
Pin Configurations (continued)



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12,16,20, 24L QFN.EPS



5Gbps PC Board Equalizer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. THIS PACKAGE OUTLINE APPLIES TO PUNCHED QFN (STEPPED SIDES).

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0°	–	12°	
P	0.24	0.42	0.60	

SYMBOL	PITCH VARIATION A			NOTE	SYMBOL	PITCH VARIATION B			NOTE	SYMBOL	PITCH VARIATION C			NOTE	SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
e		0.80 BSC			e		0.65 BSC			e		0.50 BSC			e		0.50 BSC		
N		12		3	N		16		3	N		20		3	N		24		3
Nd		3		3	Nd		4		3	Nd		5		3	Nd		6		3
Ne		3		3	Ne		4		3	Ne		5		3	Ne		6		3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.50	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

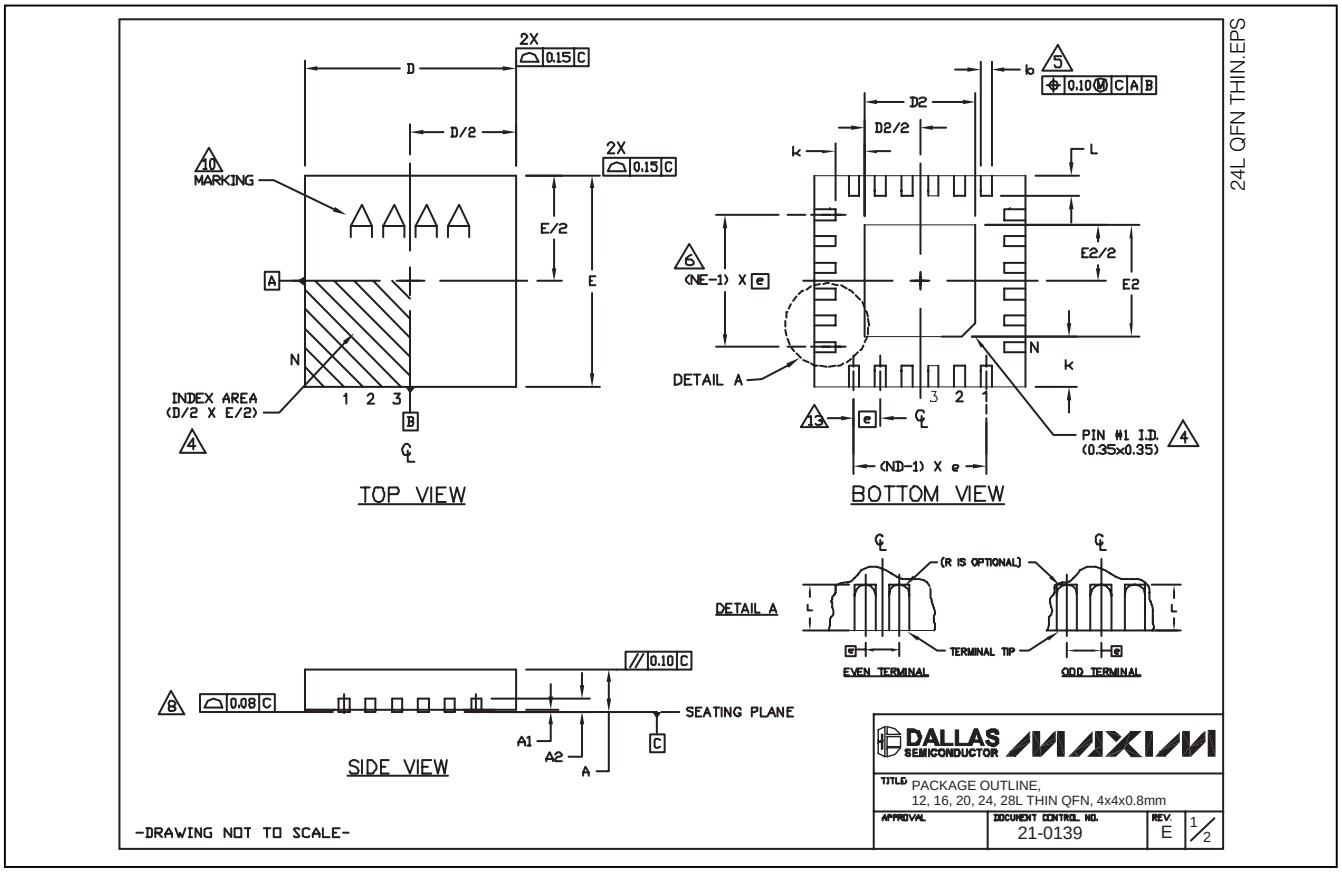
PKG. CODE	EXPOSED PAD VARIATION					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1244–2	1.95	2.10	2.25	1.95	2.10	2.25
G1644–1	1.95	2.10	2.25	1.95	2.10	2.25
G2044–3	1.95	2.10	2.25	1.95	2.10	2.25
G2044–4	1.55	1.70	1.85	1.55	1.70	1.85
G2444–1	1.95	2.10	2.25	1.95	2.10	2.25

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 12,16,20,24L QFN, 4x4x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO. 21-0106	REV. E	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



5Gbps PC Board Equalizer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2

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