LOGIC DEVICES INCORPORATED

L7710

High-Speed FFT Processor

FEATURES

- 100 MHz Operation
- Computes up to a 1024 Point Complex FFT in 18 µs* using a single Processor
- 4 Programmable Complex FFT Point Sizes: 16 Point (240 ns), 64 Point (1.2 µs), 256 Point (3.4 µs), and 1024 Point (18 µs)**
- Supports Both Forward and Inverse Fast Fourier Transforms
- Configurable as a FIR Filter with up to 1024 Complex Taps
- Contains Seven Built-In Windowing Functions in ROM
- Window Buffer (2K x 16-bit) enables Users to Program their own Complex Window Functions through Independent Address and Data Input Lines
- Standby Modes result in Significant Power Savings while simultaneously Retaining Internal Memory Data
- 16-bit Fixed Point Data Precision (96 dB Dynamic Range) on Output with 20-bit Internal Computation Precision
- 224K-bit Internal RAM
- 1.5M-bit Internal Function ROM
- 3.3 Volt Power Supply
- 5 Volt Tolerant I / O
- Package Styles Available:
  - 160-pin Plastic Quad Flatpack
  - 160-pin Flatpack

* *1024 Complex FFT Computation time based on XY Mode with 25% Input Overlap. 1024 Complex FFT with No Overlap and Averaged Linear or Decibel Power is computed in 24 µs.*

** *All Computation times based on XY Mode with 25% Input Overlap.*

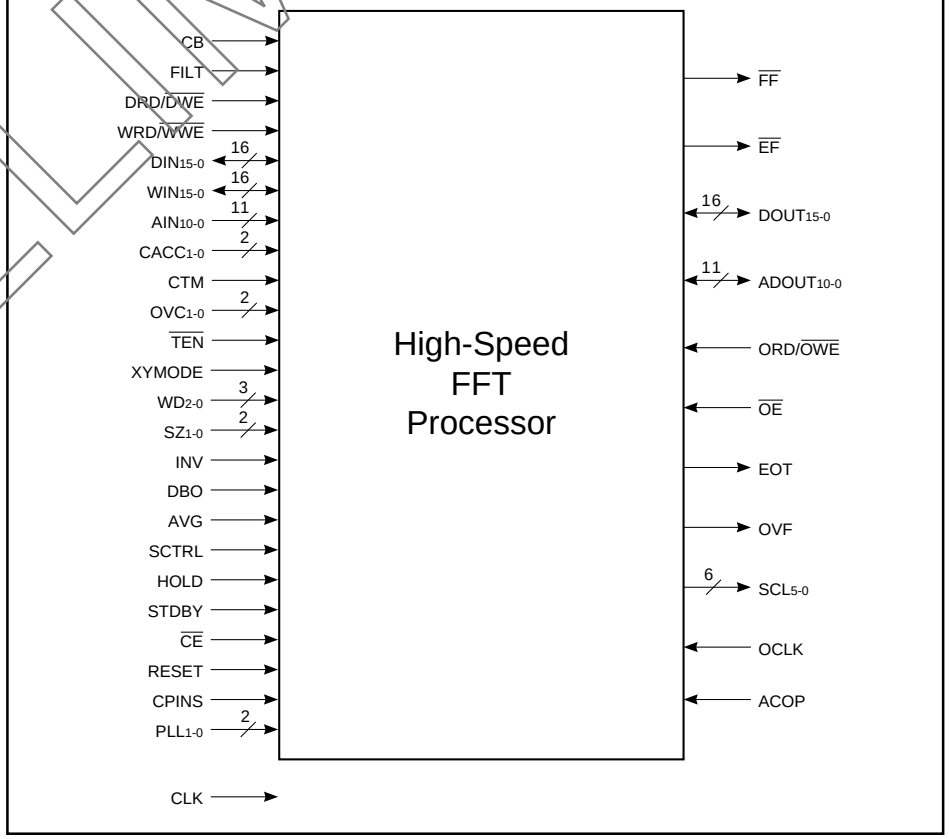
DESCRIPTION

The **L7710**, a high-speed Fast Fourier Transform Processor, allows extremely fast FFT computations to take place within a single monolithic device. All data buffering and working storage required for up to a 1024 point complex FFT operation are on-chip. This eliminates the need for expensive, high-speed external memories while decreasing internal computation time.

The core transform processor is comprised of a DragonFly™ processor which computes 4-point complex transforms in approximately 10ns when the pipeline is fully loaded. It consists of several multipliers and adders in parallel to achieve this high, sustained computation throughput rate. Input data and twiddle factor coefficients are presented to the processor core every 10ns and output is clocked out at the same rate giving the processing performances indicated.

Several programmable options are available on the device to perform FIR filtering, forward / inverse transform, complex input data windowing, transform overlap, and exponential averaging of the output. The 20-bit block floating point precision is achieved with scaling logic. Exact user specified scaling is also an option through the use of a scaling register. The data interface to the device appears to the user as if it were a synchronous SRAM with all appropriate signals.

L7710 BLOCK DIAGRAM



Some applications of the L7710 in the telecommunication field are: Wireless Base Stations, Satellite Communications, Software Defined Radios, Cable Modems and OFDM Applications. Some sample instrumentation applications include: Digital Spectrum Analyzers, Modulation Analyzers, and Distortion Analyzers.

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+3.3 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers and input memory latches.

OCLK — Output Clock

The rising edge of OCLK strobes the output buffer memory and the following flags: EF, OVF and EOT.

Inputs

DIN_{15-0} — Data Input

DIN_{15-0} is the 16-bit registered bidirectional data input port. The direction is dependent on $CACC_{1-0}$ (Table 5) and the DRD / DWE pin. Data is latched on the rising edge of CLK, provided DRD / DWE is held LOW. The data format is two's complement.

AIN_{10-0} — Data/Window Input Address

AIN_{10-0} is the input address bus for DIN_{15-0} and WIN_{15-0} and is controlled by $CACC_{1-0}$ (Table 5).

WIN_{15-0} — Window Input

WIN_{15-0} is the 16-bit registered data input port. This input port is actually bidirectional. Depending on the value present on $CACC_{1-0}$ and WRD / WWE, this port may act as an output port.

FIGURE 1. INPUT AND WINDOW DATA FORMATS

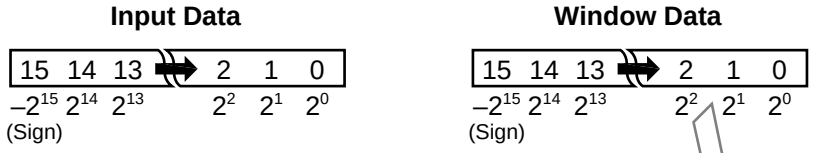
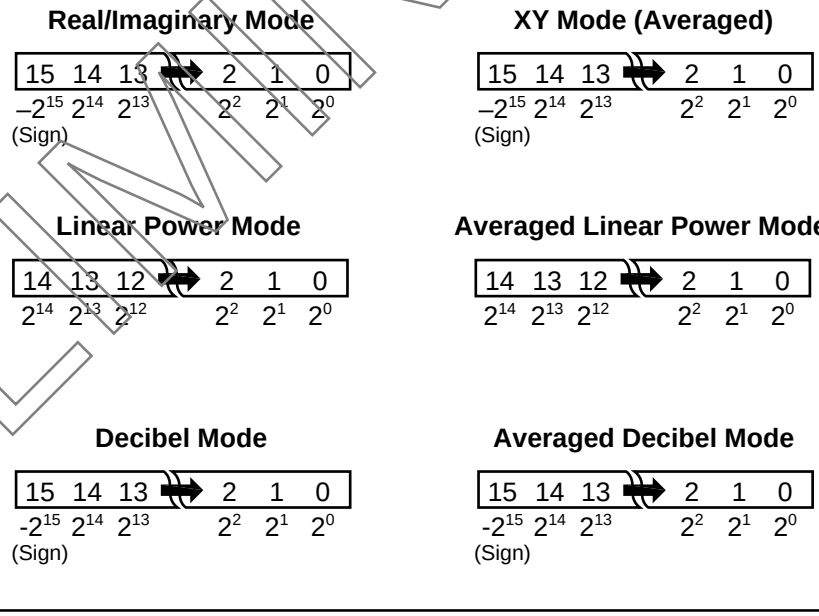


FIGURE 2. INPUT AND WINDOW ADDRESS FORMATS

FIGURE 3. DATA OUTPUT FORMATS



Data is latched on the rising edge of CLK, provided WRD / WWE is held LOW. The data format is two's complement.

Outputs

$DOUT_{15-0}$ — Data Output

$DOUT_{15-0}$ is the 16-bit registered data output port. See Figure 3.

$ADOUT_{10-0}$ — Data Output Address

$ADOUT_{10-0}$ is the registered bidirectional address bus for $DOUT_{15-0}$. In Continuous Mode (CTM=1), the LF7710 outputs data output address information automatically and sequentially. To read out data from $DOUT_{15-0}$ in any order, present addresses to $ADOUT_{10-0}$ while in Non-Continuous Mode (CTM=0).

Table 1. Overlap Mode

OVC1-0	Configuration
0 0	No Overlap
0 1	25%
1 0	50%
1 1	75%

Table 2. Window Mode

WD2-0	Configuration
0 0 0	Rectangular Window
0 0 1	Bartlett
0 1 0	Hamming
0 1 1	Hanning
1 0 0	Trapezoidal
1 0 1	Blackman-Harris
1 1 0	Welch
1 1 1	Buffer

Table 3. PLL Mode

PLL1-0	Bus Options
0 0	x1
0 1	x2
1 0	x3
1 1	x4

SCL5-0 — Output Scaling Factor

SCL5-0 is the registered output scaling factor for the current transform being read from the output buffer. The scale factor becomes valid with the first data read after an EOT.

EOT — End of Transform

The EOT signal goes HIGH when the transform has completed and goes LOW again when either a new TEN is pulsed in Non-Continuous Mode or the window stage of the next transform is completed in Continuous Mode.

OVF — Overflow Flag

When OVF goes HIGH, this indicates an internal data overflow. OVF will not go HIGH if SCALE has been set to the default mode, all zeros. In this mode, the device performs block floating point which acts as an automatic internal scale to prevent overflow. If SCALE is set to any value other than 0, the user should monitor OVF.

Table 4. Tranform Length Control

SZ1-0	Transform Length	DF Passes	PLL CLKS/Pass
0 0	16	2	19
0 1	64	3	31
1 0	256	4	79
1 1	1024	5	271

Table 5. Address Line Control (CTM = 0 & CB =0)

CACC1-0	Active Loading Location	Active Corresponding Data Bus
0 0	Control Register	WIN15-0
0 1	Window RAM	WIN15-0
1 0	Data Input RAM	DIN15-0
1 1	Data Input & Window RAM	DIN15-0 & WIN15-0

Table 6. Address Line Control (CTM = 1 & CB=0)

CACC1-0	Active Loading Location	Active Corresponding Data Bus
0 0	Control Register	WIN15-0
0 1	Window RAM	WIN15-0
1 0	N/A	N/A
1 1	Window RAM	WIN15-0

Table 7. Buffer Reset (CB=1)

CACC1-0	Location to be Cleared
0 0	Control Register
0 1	Window RAM
1 0	Input RAM
1 1	Output RAM

Table 8. Standby Modes

STDBY	HOLD	Operation
0	0	Normal Operation
0	1	Output Buffer Held
1	0	Soft Standby
1	1	Hard Standby

FF — Full Flag

FF will go LOW indicating that the data input buffer is full. FF will be HIGH at all other times. FF will automatically become HIGH upon system reset.

EF — Empty Flag

EF will go LOW indicating that the data output buffer is empty. EF will be HIGH at all other times. EF will automatically become LOW upon system reset.

Controls

CTM — Continuous Transform Mode

When CTM is LOW, Non-Continuous Transform operation is possible. When TEN is pulsed LOW, the transform starts (or restarts if the previous transform was in mid-computation). When CTM is HIGH, Continuous Transform Mode is enabled, which places the device in synchronous operation. While in Continuous

TABLE 9. VALID COMBINATIONS OF OVERLAP MODES (OVC1-0) AND PLL MODES (PLL1-0) FOR CTM=1

Full Complex Transform	
OVC1-0	**PLL1-0 Mode x1 (100 MHz)**
00	Valid Operation
01	Valid Operation
10	Valid Operation
11	Valid Operation
OVC1-0	**PLL1-0 Mode x2 (50 MHz)**
00	Data Starvation
01	Data Starvation
10	Valid Operation
11	Valid Operation
OVC1-0	**PLL1-0 Mode x3 (33 MHz)**
00	Data Starvation
01	Data Starvation
10	Data Starvation
11	Valid Operation
OVC1-0	**PLL1-0 Mode x4 (25 MHz)**
00	Data Starvation
01	Data Starvation
10	Data Starvation
11	Valid Operation

TECHNICAL NOTE:

When operating in Continuous Transform Mode, (CTM=1), Data Startvation is only possible if the Automatic Continuous Operation pin is disabled, (ACOP=0). In this case, the core FFT processor, will continuously run, without regard to the state of the input and output buffers, and it is up to the user to properly throttle the core using the HOLD pin.

When ACOP = 1 however, Data Starvation is not possible, because the core is automatically throttled based on the states of the input and output buffers. In this case, the core will wait for the input buffer, reading the data as it becomes available. Then it will run until both output buffers are full. Once both output buffers are full, the core will automatically halt, until an output buffer becomes available to write. In this case, the input buffer may become full, halting the user from writting the input buffer based on their output read rate. This possibility can be calculated based on the following formula:

$$FFT_{TIME} = \frac{\text{Input Latency}}{CLK} + \frac{\text{Input Clock Boundary Latency} + \text{Caculation Passes}\left(\text{Calculation Length}\right)}{PLL_{CLK}} + \frac{\text{Output Clock Boundary Latency} + \text{Output Latency}}{OCLK}$$

***** See Calulating Transform Time

The above formula should also be used to calculate the ideal PLL factor for continuous operation.

Transform Mode, the part acts like a "Data Pump." Data MUST be made available on the input buffers when expected and likewise, output will be shifted out in a FIFO-like autonomous fashion. Note: In either mode, the user should follow the recommended combinations of Overlap Modes (OVC1-0) and PLL Modes (PLL1-0) in order to avoid unexpected data on the output. See Table 9.

TEN — Transform Enable Control

When the device is in Continous Transform Mode (CTM=1), TEN should be held LOW. When the device is in Non-Continuous Mode (CTM=0), TEN can be pulsed LOW to start a transform. Should TEN be pulsed LOW in the middle of a transform computation, the transform will restart.

HOLD — Hold Output Buffer Data

Holds output buffer contents steady while HOLD is held HIGH. When HOLD is held LOW, the output buffer allows data to be changed. When the device is in Standby Mode, the data in all the buffers is static, regardless of the status of HOLD. If HOLD and STDBY are HIGH, the device is in a "hard standby mode". Refer toTable 8 for standby modes.

SCTRL — Scale Control

When SCTRL is LOW, scaling is automatically handled internally through block floating point. When SCTRL is HIGH, scaling is achieved through the scaling registers and is under user control.

DBO — Linear Power/dB Output

When DBO is HIGH, dB Output format is selected. When DBO is LOW, Linear Power format is selected. See Table 10.

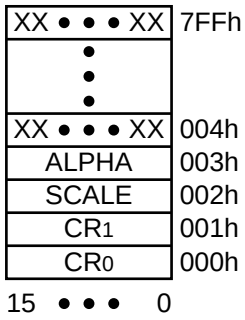
XYMODE — XY Mode

When XYMODE is HIGH, the device is in XY Mode. The output mode can be either Real / Imaginary or XY Mode (Averaged) depending on the value of AVG. If XYMODE is LOW the device is in Power Mode. The output can be in one of the following modes: Linear Power, Decibel, Averaged Linear Power, and Averaged Decibel Power. See Table 10.

AVG — Average Real and Imaginary

When AVG is enabled, Exponential Window Averaging on Power is performed. See Table 10.

FIGURE 4. CONTROL REGISTER MAP (CACC1-0=00)



FILT — FFT/FIR Operation Mode

When FILT is held LOW, the device is in FFT Mode. When FILT is held HIGH, the device is in FIR Mode.

WD2-0 — Window Configuration

WD2-0 is the 3-bit Window Configuration mode select which determines the type of Window used and is selected from the seven predefined configurations stored in the Window Configuration ROM or the user-definable Window RAM. See Table 2.

INV — Forward/Inverse Transform Control

When INV is LOW, Forward Transform is selected. When INV is HIGH, Inverse Transform is selected. This signal controlled internally when the device is in Filter Mode.

SZ1-0 — Complex Transform Length

SZ1-0 is the 2-bit Transform Length selector and is selected from the four predefined configurations. See Table 4.

OVC1-0 — Overlap Control

OVC1-0 is the 2-bit Overlap Control which determines the type of overlap used and is selected from the four predefined configurations. See Table 1.

PLL1-0 — PLL Mode

PLL1-0 is the 2-bit PLL mode selector and is selected from the four pre-defined configurations. When using the PLL, PLL clock rates over f_{PLL} are not guaranteed. See Table 3.

CACC1-0 — Control Access

CACC1-0 determines the active buffer loading location (i.e. Control Register, Window RAM and / or Data Input RAM) depending on the value of CTM. It also determines the buffer location to be cleared depending on the value of CB. For instance, in order for the user to read the Control Register 1, CACC1-0 should be set to 00. The value 001h would then be loaded through AIN10-0. Data from Control Register 1 would then be made available at WIN15-0. Refer to Tables 5-7 for CACC1-0 mapping. See Figure 4 for the Control Register Map. See Figures 5 and 6 for Control Register 0 and 1 Internal Mapping.

CPINS — Control Pins

CPINS changes control from the external control pins to the control registers. If CPINS is HIGH, control of the device is determined by the external control pins. If CPINS is LOW, control of the device is determined by the internal control registers.

OE — Output Enable

Data is available on the output port (DOUT15-0) on the falling edge of CLK while OE is held LOW. When OE is HIGH, DOUT15-0 is placed in a high-impedance state. CLKOUT is not affected by OE.

FIGURE 5. CONTROL REGISTER 0 MAP

0	0	EOT	OVF	INV	WD2	WD1	WD0	FILT	AVG	XYMODE	DBO	SCTRL	HOLD	TEN	CTM
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RESERVED BITS: 15, 14

EOT AND OVF ARE READ-ONLY BITS, THE REST ARE READ-WRITEABLE

FIGURE 6. CONTROL REGISTER 1 MAP

0	0	0	0	0	0	PLL1	PLL0	0	0	OVC1	OVC0	0	0	SZ1	SZ0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RESERVED BITS: 15 - 10, 7, 6, 3, 2

ALL BITS ARE READ/WRITABLE

FIGURE 7. INPUT BUFFER MEMORY MAP

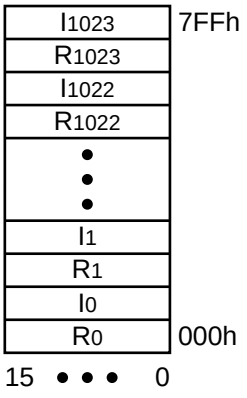


FIGURE 8. WINDOW BUFFER MEMORY MAP

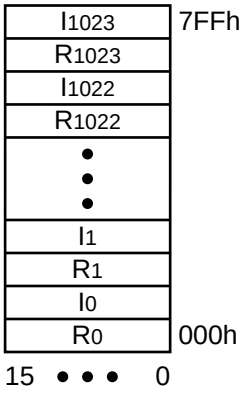


FIGURE 9. OUTPUT BUFFER MEMORY MAP XY MODE (XYMODE=1)

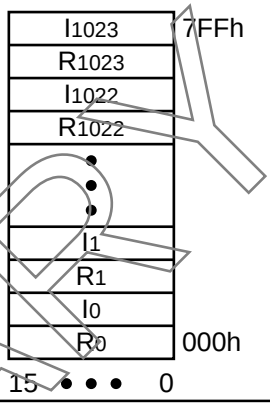
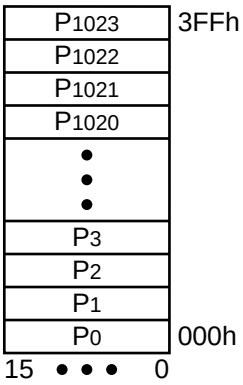


FIGURE 10. OUTPUT BUFFER MEMORY MAP POWER MODE (XYMODE=0)



DRD/DWE — Data Read/Write Enable

If DRD / DWE is held LOW while CE is held LOW, data on DIN15-0 is written to the corresponding location associated with CACC1-0 on the rising edge of CLK. If DRD / DWE is HIGH while CE is LOW, DIN15-0 is placed in an output mode in order to read data. If CE is HIGH, DIN15-0 is tri-stated.

WRD/WWE — Window Read/Write Enable

If WRD / WWE is held LOW while CE is held LOW, data on WIN15-0 is written to the corresponding location associated with CACC1-0 on the rising edge of CLK. If WRD / WWE is HIGH while CE is LOW, DIN15-0 is placed in an output mode in order to read data. If CE is HIGH, DIN15-0 is tri-stated.

CE — Chip Enable

If CE is LOW, DIN15-0 and WIN15-0 are active as either input or output ports determined by DRD / DWE and WRD / WWE. If CE is HIGH, both ports are tri-stated. Only WIN15-0 is affected when CTM=1.

CB — Clear Buffer

Clears the Input Buffer, Output Buffer, Control Register or Window Buffer to all zeros when pulsed HIGH for one clock cycle depending on the value present at CACC1-0. Refer to Table 7 for buffer selection.

STDBY — Standby Mode

By asserting STDBY to HIGH, the device is placed in a standby state. Power consumption drops, because the FFT engine has been powered down. The data in all the buffers is static, regardless of the status of HOLD. If both STDBY and HOLD are held HIGH, additional power savings is achieved by powering down the PLL (hard standby mode). To return from the hard standby state, the user must drop HOLD to a logic LOW and wait at least a **t**PLL time in order to allow the PLL to restart before dropping STDBY. Refer to Table 8 for standby modes.

ACOP — Automatic Continuous Operation

The ACOP signal automatically controls the FFT engine based on the user read-rate of the output buffer when in Continous Transfer Mode. ACOP allows the device to guarantee succesive completed transforms without loss of output data and user intervention, i.e. HOLD and / or STDBY going HIGH. When both ACOP and CTM are HIGH, the output buffer will not be written over until the empty flag, EF, is asserted. However, the input buffer may go full, i.e. the FF flag is asserted, waiting for the user to read the output buffer. The HOLD signal is not necessary when ACOP and CTM are active, except for standby modes. ACOP is not valid when CTM is low.

RESET — System Reset

The RESET signal resets all pointers to the buffers with the exception of the control registers. All values inside Control Registers 0, 1, Alpha and Scale are reset to zero.

USER ACCESSIBLE RESOURCES

Continuous Transform Mode

In Continuous Transform Mode (CTM=1), the device DIN15-0 is clocked synchronously with CLK. The L7710 expects new data on every CLK when DRD / DWE is LOW until the input buffer is full, signified by the FF Flag. Transforms are continuosly ran as long as data is available and TEN is LOW.

For example, if the PLL mode is x2 (PLL1-0=01), and overlap is in 50% overlap (OVC1-0=10) and the clock input is 50 MHz, then synchronous data should be clocked into the device at a 50 MHz input rate according to the input memory map and the size of the transform specified.

There will be 2N (N is specified by SZ1-0 in Table 4) locations which are automatically sequenced for both input and output, beginning with zero, and appear at their respective address lines. This allows the device to be directly interfaced to a parallel type A / D converter at the input or to a parallel DAC, Digital Signal Processor or DMA controller at the output.

Output data is memory mapped according to the output mode selected (see Figure 10). Output is streamed through the use of an onboard FIFO to the DOUT15-0 pins, following an address present on ADOUT10-0 for the given address setup time and OE asserted LOW. Illegal combinations of PLL Modes and OVC Modes with CTM=1 are shown in Table 9.

Addresses of input data are automatically generated in consideration of the overlap mode. EOT will be generated after the first output is received into the internal output buffer. This is designed to prevent user access prior to any post transform computations, such as log or averaging operations.

Non-Continuous Transform Mode

In non-continuous mode (CTM=0), the user has direct control over addressing the input and output data. The user is free to place data anywhere in the 2K input memory map by writing to its corresponding memory location directly according the input buffer memory map (See Figure 7).

Data on the DIN15-0 and WIN15-0 pins is latched into the buffer memories via the use of DRD / DWE and WRD / WWE along with CE. With CE held LOW, DRD / DWE or WRD / WWE (or both) are used to latch the data into the corresponding internal buffers at the address specified by the individual address lines, AIN10-0.

Once data has been clocked into the device, a logic LOW on TEN will start transform operations. On completion of the transform, EOT will go HIGH indicating results are available on the output data bus.

Addresses of desired output locations are driven via an external device (e.g. DSP or DMA controller). Between EOT and the next TEN assertion, new input data, as well as any new window data, can be entered into the device with timing based on t_{CYC}. The Input and Window buffers may be written before the completion of the prevous transform, but only upon completion of the windowing pass by the processor core. Since there are no flags to indicate completion of the windowing pass, the user must be mindful of the number of clock cycles.

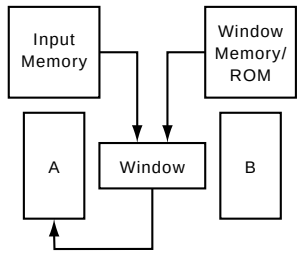
The user must be aware that if the overlap control is in any mode other than (OVC10=00) then aged data (located at lower addresses) is overwritten by more recent data prior to EOT assertion. For example, in 25% overlap mode (OVC10=01) and a 1024 point complex transform (SZ10=11); real and imaginary points 768 and higher (600h-7FFh) are copied to the first 256 real and imaginary locations of the buffer (000h-1FFh). (See Figure 7 for the Input Buffer Memory Map). In this example, the user should start addressing the most recent data beginning at 200h (point 256 and higher).

TABLE 10. OUTPUT MODES FOR COMBINATIONS OF AVG, XYMODE AND DBO

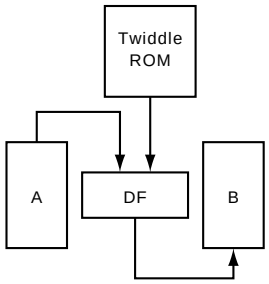
AVG	XYMODE	DBO	DF Passes	Output Modes
0	0	0	1	Linear Power Mode (Refer to Figure 10)
0	0	1	1	Decibel Mode (Refer to Figure 10)
0	1	0	0	Real/Imaginary Mode (Refer to Figure 9)
0	1	1	X	Invalid Mode
1	0	0	2	Averaged Linear Power Mode (Refer to Figure 10)
1	0	1	2	Averaged Decibel Power Mode (Refer to Figure 10)
1	1	0	1	XY Mode (Averaged) (Refer to Figure 9)
1	1	1	X	Invalid Mode

Figure 12. Eight Stages Of The 1024 Point FFT Data Flow

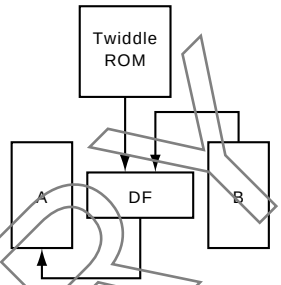
Stage 1. (271 Cycles)



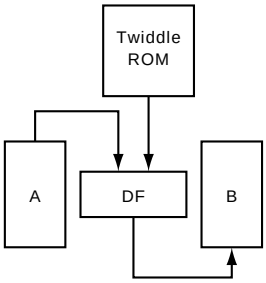
Stage 2. (271 Cycles)



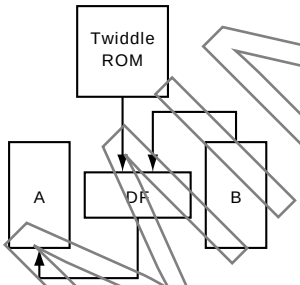
Stage 3. (271 Cycles)



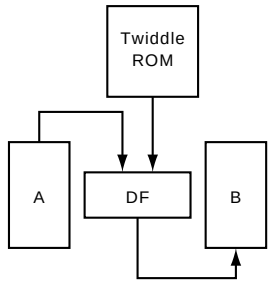
Stage 4. (271 Cycles)



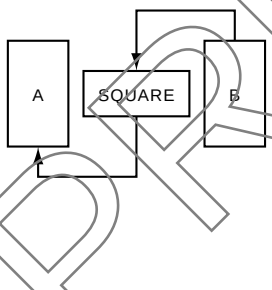
Stage 5. (271 Cycles)



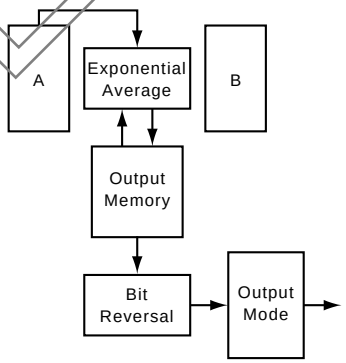
Stage 6. (271 Cycles)



Stage 7. (271 Cycles)



Stage 8. (271 Cycles)



Control Register Mapping

By setting CACC1-0 to 00 and CB to 0, the window buffer is disabled and causes the first four locations to be treated as "configuration" registers. Control Registers 0 and 1 are found in the corresponding first two locations 000h and 001h (See Figure 4). Figures 5 and 6 show the mapping format of Control Registers 0 and 1. Control Register 0 consists of 16 bits which are readable and writable with the exception of EOT which is read-only.

Control Register 1 also consists of 16 bits, however 10 bits are reserved. All 6 of the non-reserved bits are read / writeable. See the Signal Definitions for descriptions for each bit.

The SCALE control register at location 002h is for input "power-of-two" scaling. The device scales each stage of the processing by a fixed value of 2^0 to 2^4, in the event the user does not wish to use the block-floating point scaling provided by the hardware.

Warning: Internal computations *may* overflow if the user is not careful about input scaling. When SCALE is set to other than 0 (which is the default reset state), the device will not automatically scale internally to prevent an overflow condition. Should an overflow condition occur, the overflow flag (OVF) will go HIGH.

The ALPHA control register at location 003h is the value associated with exponential averaging of the output. The equation is:

$$\alpha \cdot \text{OUTPUT} + (1-\alpha) \cdot \text{LAST\_OUTPUT}$$

This register is a positive value in the range of 0000h-7FFFh (representing a positive fractional magnitude between 0.0 and 1.0). When the ALPHA register is non-zero, it is used to compute the "moving average" represented by the equation above.

Operational Modes - FFT

This device has three operation modes, functioning as an FFT, IFFT or as an FIR filter. In FFT mode (FILT=0, INV=0), an FFT is executed according to the size specified by SZ_{1-0} bits as is shown in Table 4.

Data is loaded into the unit (according to the status of CTM) and only to 2N memory locations, N being the transform size. Data up to the first 2N input memory locations will be pre-multiplied (complex) by the user window specifed. Upon application of the TEN, the input data is fed through the window pass of the L7710. The L7710 then processes the data through the DragonFly processor core. The Twiddle Factor numbers for the DragonFly processor are built into the L7710 ROM.

The number of stages required by the L7710 is dependent upon the FFT size. Table 4 shows the number of DragonFly passes required for each of the transform lengths. Each pass requires (N / 4 + 15) clock cycles to complete the DragonFly.

To maintain optimum data flow, the L7710 has two working storage buffers as shown in Figure 12. These storage buffers allow the input and output buffers to be continously accessed by the user while the calculations are in progress. Transform results are output according to the output format chosen by the user (Table 10) and in like manner to the input, occupy the first 2N output buffer locations. Depending on the ouput format chosen, the L7710 may require additional computational passes for Power (Linear and dB) and Averaging calculations. Figure 12 shows Stages 7 and 8 as these computational passes.

Output Modes

For the Linear Power and Decibel Modes, the L7710 requires one extra stage (Figure 12) to complete all the computations in the sum of the squares calculations. The square root and the decibel calculations are done during the output buffering.

The L7710 will also require an extra stage if averaging (AVG=1) is selected. Refer to Control Register Mapping for the equation of ALPHA, the exponential value associated with averaging.

The L7710 does the bit reversal mapping as the user reads the output buffer. Figures 9 and 10 show the output memory maps for Power and XY modes.

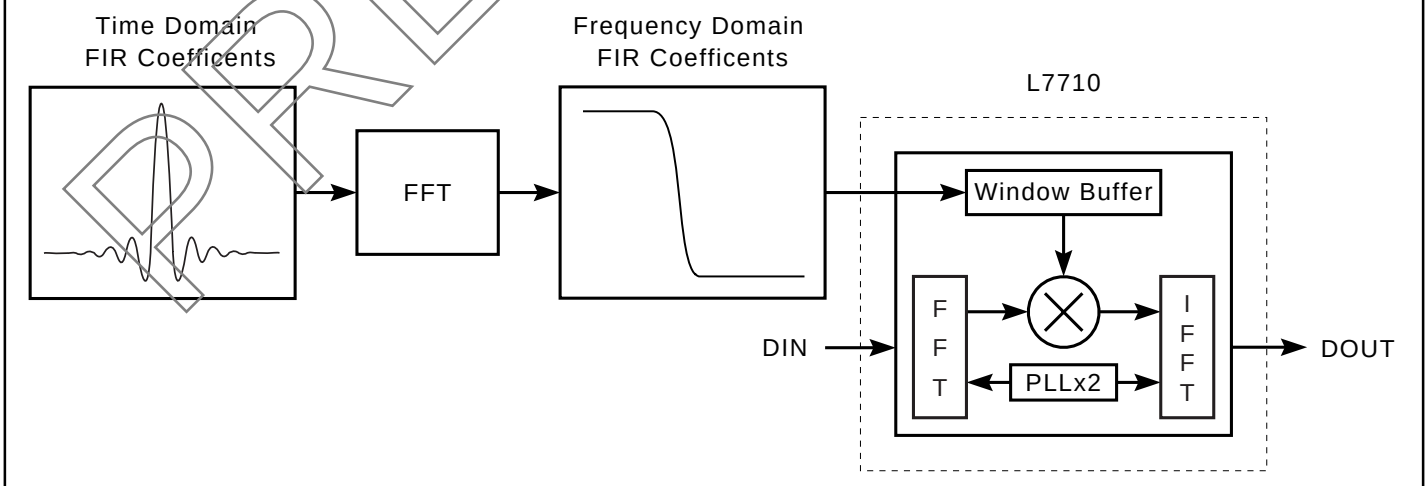
IFFT MODE

In IFFT Mode (Filt=0, INV=1), an IFFT is executed according to the following formula:

IFFT = conj(fft(conj(data)))

The L7710 completes all conjucating internally. The frequency domain data is available in the output buffer at the assertion of EOT. The IFFT requires the same number of calculation passes as

FIGURE 13. FIR MODE



an FFT. The conjucations do not require any extra calculation passes or clock cycles.

All data formats and controls are equivalent to the FFT mode.

FIR MODE

In FIR mode (FILT=1), a FIR filter is implemented. The filter takes a little more than twice as long to operate since it must, of necessity, perform two transforms, an FFT and an inverse FFT. After the first FFT transform is completed, the results are multiplied by the data found in the window buffer. The window buffer acts as coefficient storage for the filter. Finally, a second inverse transform is executed and the operation is complete. The results on the output buffer are the filtered data. The data is output in a similar fashion to that of the FFT output, however, the EOT will not be asserted until the second transform is completed. The INV pin and register is toggled internally by the device and must be set to zero in this mode. Since the window buffer is used for coefficient storage, the user is limited to using one of the built-in window functions for the first FFT pass.

Calculating And Loading Coefficients

The coefficients used by the L7710 in the FIR Filter Mode are calculated by taking the FFT of the normal impulse response coefficients. This is required, because the L7710 will filter in the frequency domain. Since the L7710 handles all the bit reversal requirements, the control FILT=1 must be set before the coefficients are loaded, and the coefficients must be loaded in normal sequence. See Figure 13.

Data Handling and Formats

The data is input according the SZ_{1-0} and the status of CTM up to 2N locations, N being the filter size.

To acheive continuous operation in Filter Mode, the L7710 PLL should be set to at least a 2x factor of CLK and CLK and OCLK should be tied together.

Data Handling Formats

There are a variety of output modes which affect the presentation of output data and in some cases, its format. For example, in Real / Imaginary mode (XYMODE=1), at the completion of a transform, data appears at the output buffer as interleaved real and imaginary (See Figure 10) and in 16-bit two's complement format (See Figure 3). In Linear Power mode, data is presented to the first half (N) output buffer locations and is in 15-bit magnitude format. In Decibel Output mode (DBO=1), data is presented to the output buffer in negative magnitude format (16 bits wide but bit 15 is always 1) indicating a maximum of 0 dB at 0 and descending negatively from there.

In the continuous mode (CTM=1), the address lines are driven from the device and are sequenced from 0 to 2N memory locations for XYMODE=1 or N memory locations for power mode (XYMODE=0).

Calculating Transform Time

The formula for calculating the tranform time as shown in Table 9:

Input Latency is the pipelined data path registers before the input ram. This data path requires 2 CLK cycles.

The Input Clock Boundary Latency is the syncronization of the CLK with the PLL_{CLK}. This latency is dependent on a syncronization circuit and may require 2 or 3 PLL_{CLK} cycles because of the ambiguity of the asyncronous clock boundary.

The number of calculation passes is dependent on the transform length. This one more than the number of DrangonFly passes because of the window pass plus the additional output mode passes required. See Tables 4 and 10.

The calculation length is the transform size / 4 + 15. See Table 4.

The PLL_{CLK} is equal to CLK times the PLL_{CLK} multiply factor. See Table 3.

The Output Clock Boundary Latency is the syncronization of the PLL_{CLK} with the ØCLK. This latency is dependent on a syncronization circuit and may require 2 or 3 OCLK cycles because of the ambiguity of the asyncronous clock boundary.

Output Latency is the pipelined data path registers after the ouptut RAM. This data path requires 5 CLK cycles.

Example 1.

1K FFT in XYMODE in Non-Continuous Transfer Mode at 100MHz.
CLK=PLL_{CLK}=OCLK

FFT_{TIME} = 2 / CLK + (2+(6*271)) / PLL_{CLK}) + (2+5) / OCLK = 16.37 µs

Example 2.

1K FFT in Averaged dB Power Mode in Continuous Transfer Mode at 50MHz
CLK=OCLK & PLL_{CLK} = CLKx2

FFT_{TIME} = 2 / CLK + (2+(8*271)) / PLL_{CLK}) + (2+5) / OCLK = 21.88 µs

TABLE 11. PIN CONFIGURATIONS

Pin	FFT Mode	IFFT Mode	FIR Mode
Filt	0	0	1
INV	0	1	0
WD	User	User	≠7
PLL	Table 9	Table 9	≥2x

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to 5.5 V
Signal applied to high impedance output ..... –0.5 V to 5.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA
ESD (MIL-STD-883E Method 3015.7) ..... > 2000 V

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	3.00 V ≤ **V**CC ≤ 3.60 V
Active Operation, Military	–55°C to +125°C	3.00 V ≤ **V**CC ≤ 3.60 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±10	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			800	mA
ICC2	**V**CC Current, Quiescent	Soft Standby, PLL Running (Note 7)			10	mA
ICC3	**V**CC Current, Quiescent	Hard Standby, PLL Disabled (Note 7)			2	mA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L7710					
						10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time					10	
t_{PW}	Clock Pulse Width					4	
t_S	Input Setup Time					3	
t_H	Input Hold Time					0	
t_D	Output Delay						7
t_{ENA}	Three-State Output Enable Delay (Note 11)						10
t_{DIS}	Three-State Output Disable Delay (Note 11)						10

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L7710					
						12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time					12	
t_{PW}	Clock Pulse Width					5	
t_S	Input Setup Time					4	
t_H	Input Hold Time					0	
t_D	Output Delay						8
t_{ENA}	Three-State Output Enable Delay (Note 11)						12
t_{DIS}	Three-State Output Disable Delay (Note 11)						12

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above **V**CC will be clamped beginning at –0.6 V and **V**CC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a X MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except **t**ENA / **t**DIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For **t**ENABLE and **t**DISABLE measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and **V**CC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. INPUT CIRCUIT

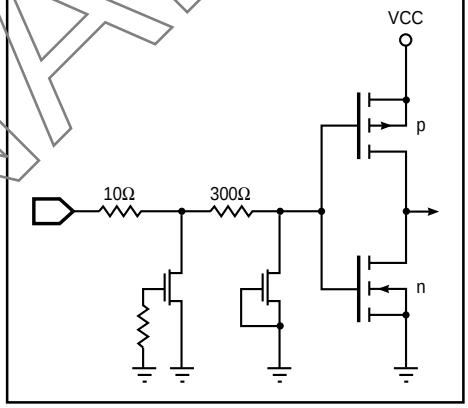


FIGURE B. OUTPUT CIRCUIT

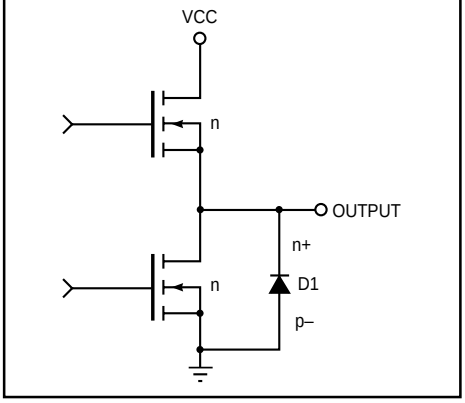
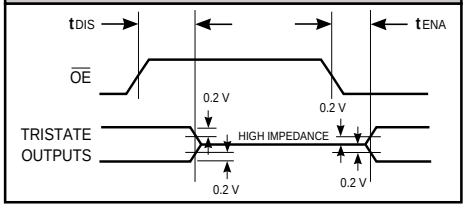
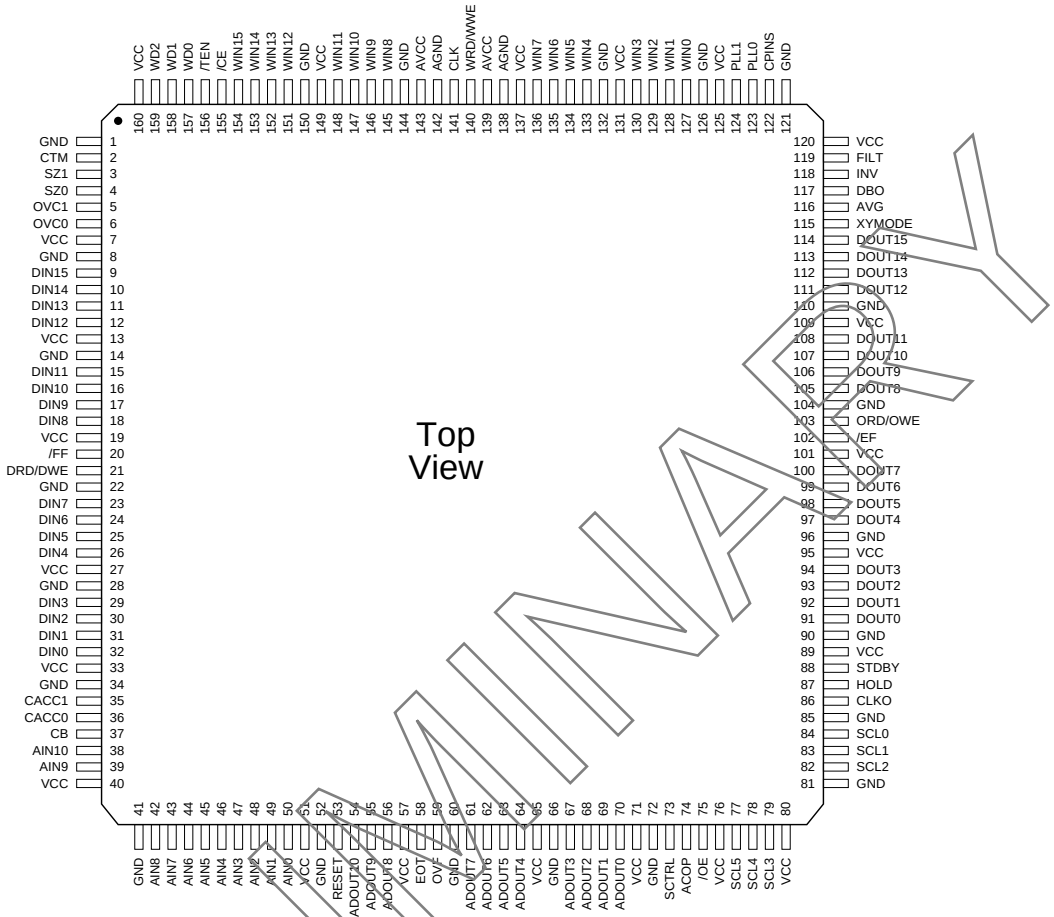


FIGURE C. THRESHOLD LEVELS



ORDERING INFORMATION

160-pin



Speed	Plastic Quad Flatpack (Q6)	Flatpack (F4)
	0°C to +70°C — Commercial Screening	
10 ns	L7710QC10	
	–40°C to +85°C — Industrial Screening	
10 ns	L7710QI10	
	–55°C to +125°C — MIL-STD-883 Compliant	
12 ns		L7710FMB12