



GIGABIT ETHERNET SERDES TRANSCEIVER

PRELIMINARY
IDT77V7101
77V7111

Features

- ◆ IEEE 802.3z Gigabit Ethernet compatible
- ◆ 1.25 Gbps full duplex transmission and reception in a single IC
- ◆ Direct connection to Twinax cable
- ◆ Automatic equalization of 25m Twinax
- ◆ Optical interface through fiber module
- ◆ 10-bit parallel TX and RX interfaces based on EIA/TIA X3T11
- ◆ Signal Detect, internal or external
- ◆ Code Group Realignment with Disable
- ◆ Internal Loopback mode
- ◆ 62.5MHz recovered clock (V7101) or 125MHz recovered clock (V7111)
- ◆ Low power 3.3V CMOS
- ◆ Few external components required
- ◆ 64-pin 10mm and 14mm packages
- ◆ Pin-outs are compatible with industry standard devices

Applications

- ◆ IEEE 802.3z Gigabit media interfaces:
 - 1000BASE-CX 150Ω Twinax
 - 1000BASE-LX Optical
 - 1000BASE-SX Optical
- ◆ Provides the PMA function of the PHY
- ◆ 100Ω STP interface
- ◆ High speed custom serial interface
- ◆ Backplane serial link
- ◆ Bus extension

Description

The IDT77V7101/7111 is a monolithic 1.25 Gigabits per second (Gbps) Ethernet Serializer/Deserializer (SerDes) Transceiver. It is designed to provide the Physical Medium Attachment (PMA) portion of the IEEE 802.3z PHY layer.

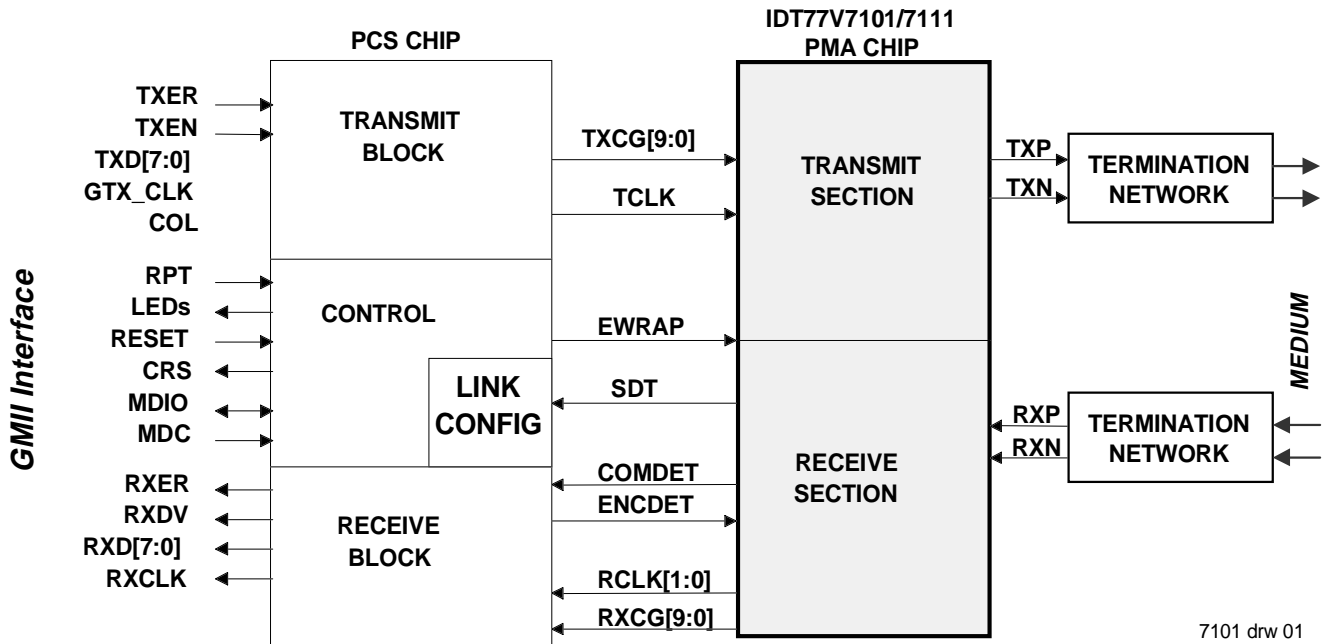


Figure 1. Typical Application Block Diagram

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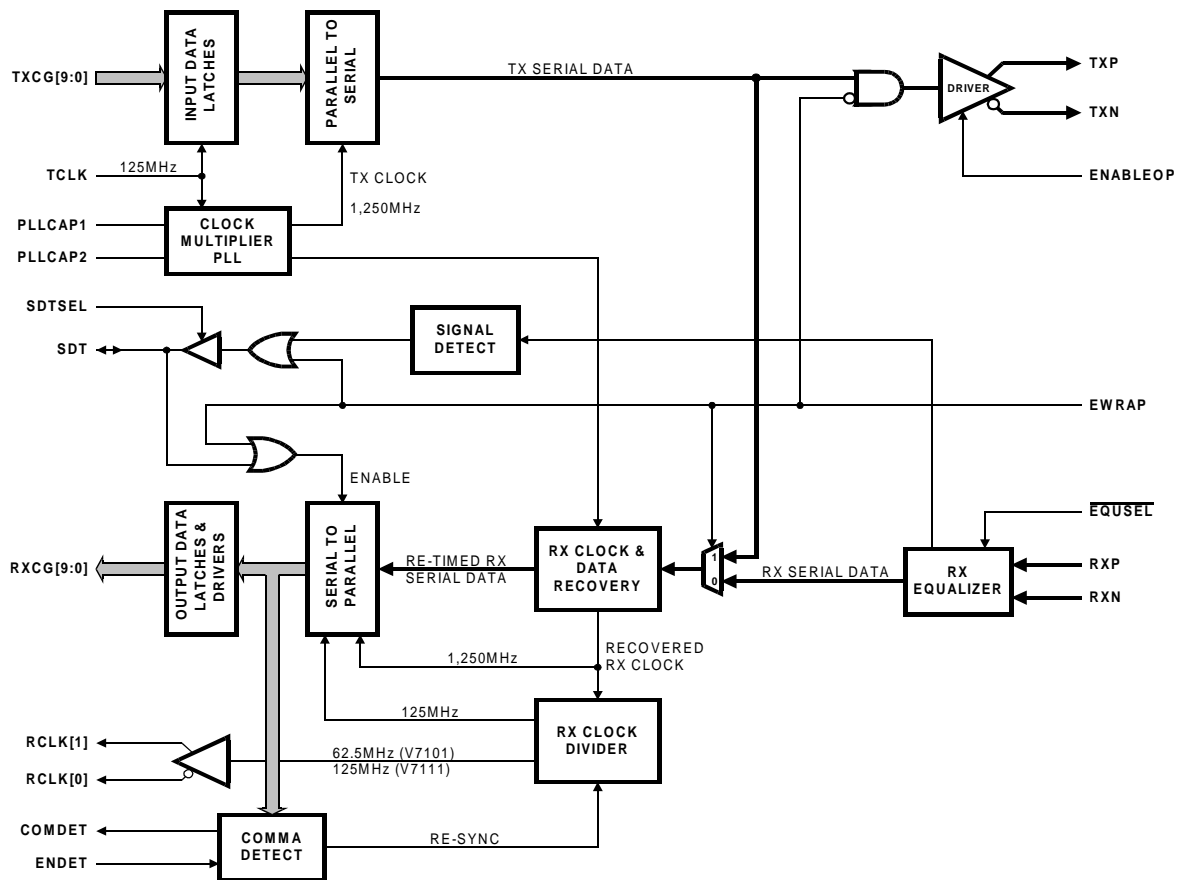


Figure 2. IDT77V7101/7111 Internal Block Diagram

Functional Description

Overview

Figure 1 shows a block diagram of a typical application. The parallel interface connects to a Physical Coding Sublayer (PCS) chip. The serial inputs and outputs connect directly to twinax cables for electrical transmission, or to a fiber optic module for optical transmission.

Figure 2 shows an internal block diagram of the IDT77V7101/7111. The TXCG[9:0] inputs receive parallel 10-bit transmit code groups, already encoded in 8B/10B format by the PCS chip. The code groups are latched on the rising edges of the incoming 125MHz reference clock (TCLK). Then they are serialized, and the bit stream is retimed by an internal PLL that multiplies TCLK up to 1.25GHz. This data stream is transmitted through PECL drivers into the cable or fiber optic module.

The 77V7101/7111 receives serial data from the cable or fiber optic module, equalizing up to 30m of twinax cable loss. It deserializes the data into 10-bit receive code groups, and recovers a receive clock (RCLK) from the data stream. RCLK is used to clock-out the receive code groups to the PCS chip.

RCLK is available in two variants. In the 77V7101, RCLK is output at 62.5MHz. In the IDT77V7111, RCLK is output at 125MHz. In both cases, RCLK is output in two complementary phases as RCLK[0] and RCLK[1]. At 62.5MHz, RCLK[0] and RCLK[1] are used to clock out alternating code groups. At 125MHz, RCLK[1] provides rising-edge clocking of all receive code groups, while RCLK[0] provides falling-edge clocking of all receive code groups.

A Signal Detect I/O pin has been provided. It is normally configured as an output when copper media are used to signal the PCS chip that a minimum receive signal level has been detected. For fiber optic media, it can be configured as an input, allowing the fiber module to perform signal detection.

Transmit Clock (TCLK)

The user-supplied 125MHz transmit reference clock (TCLK) is used for several functions. As the transmit code group clock, its rising edges directly strobe the 10-bit input data latch to sample the transmit code group bus, TXCG[9:0]. Therefore, its edges must be properly aligned to the incoming parallel transmit data.

TCLK also serves as the frequency reference for the Transmit PLL Clock Multiplier, which uses it to synthesize the internal clock signals necessary for 1.25 Gbps signaling.

Transmit Data Path

It is assumed that the original 8-bit user data to be transmitted has already been 8B/10B-encoded into 10-bit transmit code groups by external PCS logic before being sent to the IDT77V7101/7111 for transmission. The incoming code groups are received on the Transmit Code Group bus, TXCG[9:0], and are sampled on the rising edges of TCLK by the input data latch. Figure 6 shows the timing relationship

between the clock and the parallel data, and the “AC Electrical Characteristics” section shows the timing requirements for these signals.

The parallel transmit data is sent to the parallel-to-serial converter. This uses the internal clock signals synthesized by the transmit PLL to convert the 10-bit transmit data from parallel to serial format, and to retime each bit at 1250MHz. The least significant bit TXCG[0] is transmitted first.

The Transmit Line Driver transmits the serial data in differential form onto the transmit half of the chosen medium. The Line Driver can connect directly to copper media such as 150Ω twinax cable (through DC-blocking capacitors), or through a fiber optic transceiver module to fiber optic cable.

The Line Driver is a source-follower that provides a voltage-mode differential PECL-level-compatible output. It has a differential source impedance of approximately 30Ω. ENABLEOP must be held to a logic high level for normal operation. When ENABLEOP is held low, the Line Driver output is set to a high impedance state.

Refer to the “Medium Attachment” section below for more information on connecting the line driver to various media.

Receive Equalization

The 77V7101/7111 has an equalization circuit at the receiver input to compensate the signal distortion caused by up to 25m of unequalized 150Ω twinax cable. For operation over short cables or long internally equalized cables, the equalizer can be either enabled or disabled.

Users may wish to disable it in cases where crosstalk or reflections rather than electrical line length are the major causes of signal impairment, such as when the serial link runs through a crowded backplane or poorly matched connector rather than a long unequalized cable. Doing so can improve the tolerance of these impairments. The equalizer can also be disabled for the same reason when interfacing to fiber optic transceivers or to short or internally-equalized cables.

Clock Recovery

After the serial input signal has passed through the front end’s equalizing amplifier, a receive clock must be recovered with which to sample the incoming data stream. Clock recovery is automatic, with no user intervention such as PLL training necessary. The internal Receive PLL locks the phase of its VCO to that of the incoming data to produce a bit-clock. This bit-clock is then divided down to become the internal 125MHz code-group clock (ICLK). Finally, the recovered receive clock is output as complementary signals (180° out of phase with each other) at RCLK[0] and RCLK[1] at 62.5MHz in the 77V7101, and at 125MHz in the 77V7111. In the 77V7101, the 62.5MHz RCLK[0] and RCLK[1] signals are used to clock out alternating 125MHz code groups. In the 77V7111, 125MHz RCLK[1] or RCLK[0] signals provide rising-edge or falling-edge clocking of all receive code groups, respectively.

Data Recovery

Following equalization and buffering, the receive serial data stream is retimed by the recovered bit-clock, then converted from serial to parallel form using both bit- and code-group-clocks. Parallel receive data is clocked into the output data latch by the internal 125MHz code-group-clock, and output at the Receive Code Group bus, RXCG[9:0]. RCLK[1:0] are used to clock out the data from RXCG[9:0] as described in “Clock Recovery” above.

Code Group Alignment

A code group alignment function detects the presence of comma+ characters (0011111xxx) in the receive data stream. If ENDET=1, each occurrence of a comma+ causes realignment of the bit positions of the received comma+ code group to match the standard 8B/10B format. Realignment may be achieved by dropping bits from the data stream when necessary. Comma+ characters are always clocked out by the rising edge of RCLK[1]. In the case of the 77V7101 this may entail stretching RCLK[1:0] half a cycle (nominally 8ns). Subsequent code groups retain this bit and clock alignment unless shifted by errors. If ENDET=0, realignment and clock stretching are disabled.

The COMDET output is an indicator for the detection of comma+ characters. When ENDET is high and a comma+ character is detected, COMDET will go high for half an RCLK period in the 77V7101, or one clock period in the 77V7111, following the rising edge of RCLK[0]. Otherwise, it will remain low.

Proper operation of COMDET, RCLK[1:0], and the code group alignment function requires that comma+ characters not be received back-to-back, as per standard 8B/10B encoding.

Signal Detect

The Signal Detect pin SDT is a bi-directional pin controlled by SDTSEL. When SDTSEL is high, SDT is an output that remains high when the receive signal amplitude exceeds the Signal Detect threshold VSD, and receive data will be output normally at RXCG[9:0]. (Note that this does not indicate that a compliant 1000BASE-X signal is being received.) A receive signal amplitude below the threshold causes the SDT output to remain low, and the RXCG[9:0] outputs to all be forced to logic 1. This helps prevent the generation of random data at the receiver outputs in the absence of valid incoming data.

When SDTSEL is low, SDT becomes a PECL input to allow external devices such as fiber optic modules to perform the Signal Detect function. Signal detection should cause the external device to drive SDT to PECL logic 1, while insufficient signal amplitude should drive SDT to PECL logic 0. As before, a logic 0 at SDT will cause RXCG[9:0] outputs to all be forced to logic 1.

Internal Loopback

Loopback mode permits testing most of the internal circuitry without using an external medium, and is enabled by holding EWRAP high. Transmit code groups sent to the TXCG[9:0] inputs are processed normally by the transmit circuitry, then looped back through the receive circuitry to the RXCG[9:0] outputs as if they were incoming serial data. At the loopback point, transmit serial data is diverted from before the Line Driver, and replaces the equalizer output as the input to the clock and data recovery circuits. Nearly all the internal circuits except for the Line Driver and Receive Equalizer are exercised, with all internal Serializer, Deserializer, and clock functions occurring at their normal rates.

Loopback mode holds the Line Driver output at PECL logic 1. For normal operation, EWRAP must be held low.

Medium Attachment

(Serial Interface)

Figure 3 and Figure 4 show typical methods of connecting either twinax or fiber optic links. In both cases 150Ω bias resistors are connected from TXP and TXN to ground. AC-coupling of transmitter output to cable is used, as required by IEEE 802.3z. The optional series resistors RSER may be added to help absorb reflections due to mismatched loads. Typical

values range from 0-50Ω. The amount of output attenuation desired should also be considered when setting these values. Load terminations, transmission lines (including traces) and connectors should be selected or designed to have matching impedances.

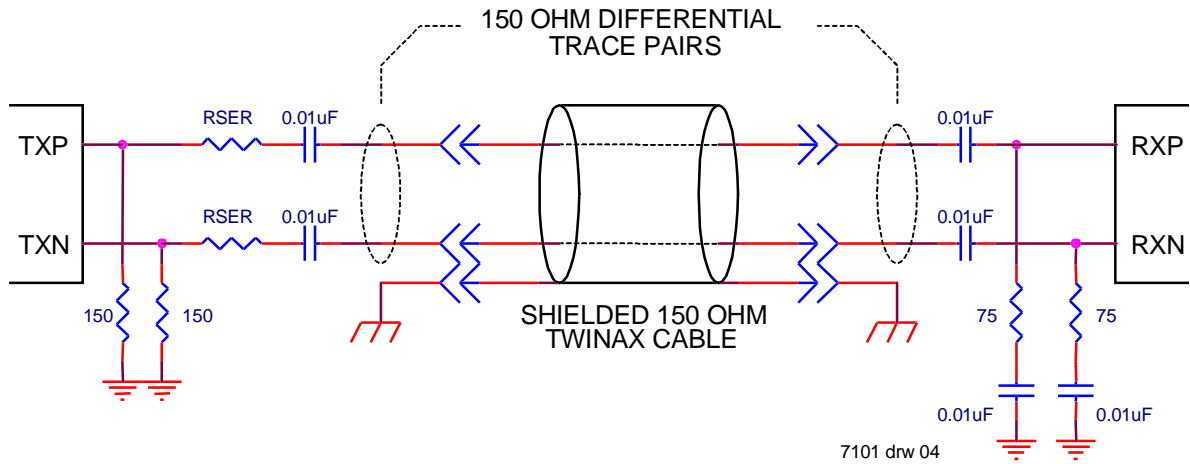


Figure 3. Typical 1000BASE-CX Medium Attachment (150Ω Twinax half link shown)

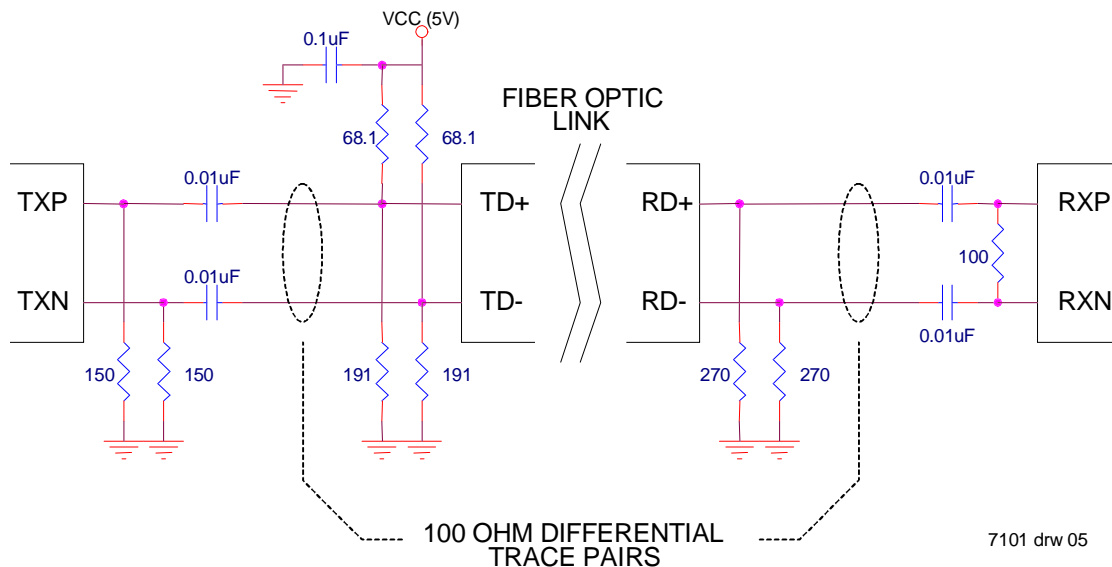


Figure 4. Typical 1000BASE-LX/SX Medium Attachment (Fiber Optic half link shown)

NOTES:

1. The optional series RSER resistors may be added to help absorb reflections due to mismatched loads. Typical values range from 0-50Ω, depending on the characteristic impedance of the transmission lines and the amount of acceptable attenuation.
2. Termination circuits at the fiber optic module are typical values for a module running on a 5V supply, with 100Ω differential impedance at each load end. Modules with other supply voltages may require adjustment of these circuit values to achieve the recommended input voltages. Follow fiber optic module manufacturer's recommendations for setting input voltages, receiver bias resistors, and termination impedance.

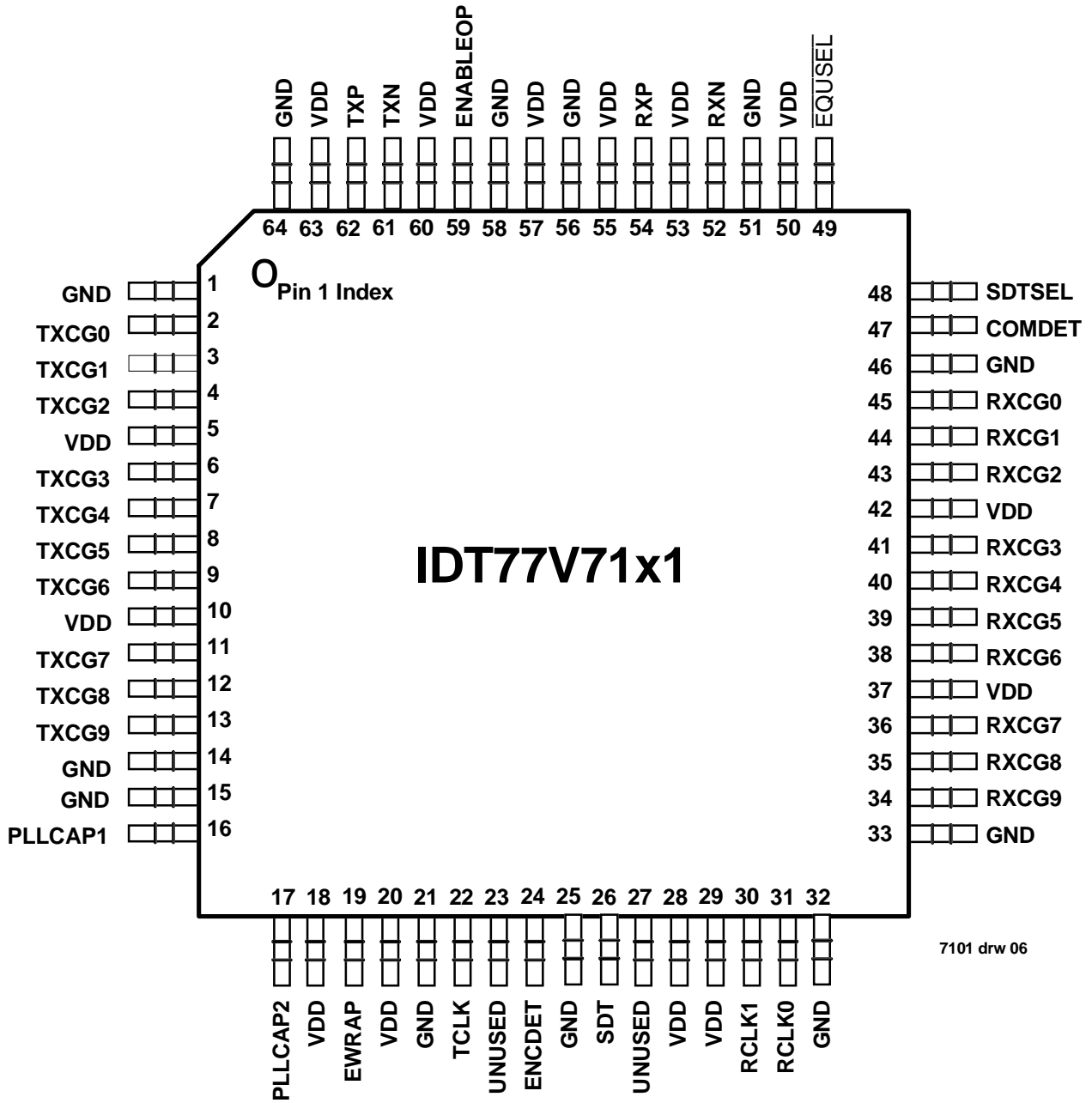


Figure 5. Pin Assignments

Pin Descriptions

Transmit-Side Signals

Pin #	Name	Type	Description
22	TCLK	TTL Input	The transmit code group clock, 1/10 the serial baud rate, whose rising edges are used to sample the incoming transmit code groups (TXCG[9:0]). TCLK is also the reference clock used by the transmit PLL to synthesize the high-speed serial data clock.
13,12,11,9, 8,7,6,4,3,2	TXCG[9:0]	TTL Inputs	The PMA chip's transmit code group input port, accepting 10-bit parallel transmit data already encoded in 8B/10B format. This bus is clocked into the chip on the rising edge of TCLK. TXCG[0] is the least significant bit and the first to be transmitted.
62,61	TXP, TXN	HS Output	The high-speed + and - serial data differential outputs to the cable or fiber optic transmitter. For output = "1", TXP > TXN.

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Receive-Side Signals

Pin #	Name	Type	Description
54, 52	RXP, RXN	HS Input	The high-speed serial data differential inputs from the twisted-pair cable or fiber optic receiver. For input = "1", RXP > RXN.
34,35,36,38, 39,40,41,43, 44,45	RXCG[9:0]	TTL Outputs	The PMA chip's receive code group output port, presenting 10-bit receive data on alternate rising edges of RCLK[0] and RCLK[1] (V7101), or on all rising edges of RCLK[1] (V7111). If ENCDDET = 1, comma + code groups are realigned and forced to be clocked by RCLK[1]. RXCG[9:0] are forced high when SDT = 0. RXCG[0] is the least significant bit and the first to be received.
30 31	RCLK1 RCKLO	TTL Outputs	The complementary receive clock outputs, recovered from the received serial data. The V7101 RCLK[1:0] outputs are 1/20 the serial baud rate, and clock-out alternate receive code groups from RXCG[9:0] on their rising edges. If ENCDDET = 1. RCLK[1] clocks all comma + characters. The V7111 RCLK[1:0] outputs are 1/10 the serial baud rate, and RCLK[1] provides all positive-edge clocking.

7101 tbl 02

Control Signals

Pin #	Name	Type	Description
47	COMDET	TTL Output	When ENCDDET = 1 and a comma + character is detected in the receive bit stream. COMDET will go high for half an RCLK period in the V7101, or one clock period in the V7111, following the rising edge of RCLK[0].
59	ENABLEOP	TTL Input	A high level on this pin is required to activate the Line Driver, which otherwise remains in a high impedance state. An internal 50k pull-up resistor prevents "floating". Hold ENABLEOP high for normal operation.
24	ENCDDET	TTL Input	A logic 1 input enables code group realignment on comma + reception. A logic 0 input keeps current word alignment and disables COMDET. An internal 50k pull-up resistor prevents "floating".
49	$\overline{\text{EQUSEL}}$	TTL Input	Mode Select input for Equalizer. If $\overline{\text{EQUSEL}} = 0$, equalization is on. If $\overline{\text{EQUSEL}} = 1$, equalization is off. Equalization may be turned on for all cable lengths. An internal 50k pull-down resistor prevents "floating". Hold $\overline{\text{EQUSEL}}$ low for normal operation.
19	EWRAP	TTL Input	"Enable Wrap," this signal must be at a logic low level for normal operation. A high logic level forces the transmit data to be looped back from TXCG[9:0] to RXCG[9:0], exercising most of the internal circuitry. An internal 50k pull-down resistor prevents "floating". Hold EWRAP low for normal operation.
16 17	PLLCAP1 PLLCAP2	Analog	A .001 μ F capacitor is connected between these pins to set the loop filter characteristics of the transmit PLL.
26	SDT	Bi-directional PECL Input TTL Output	Signal Detect, with direction controlled by SDTSEL. If SDTSEL is high, SDT is a TTL output, where a logic 1 indicates that the receiver input level is above the internal "signal detect" threshold. if SDTSEL is low, SDT becomes a PECL input, enabling signal detection by external devices such as fiber optic transceivers. In any case, a logic 0 at SDT forces all RXCG[9:0] signals high, while a logic 1 allows normal operation.
48	SDTSEL	TTL Input	Signal Detect direction control. If SDTSEL = 0, SDT is a PECL level input. If SDTSEL = 1, SDT is a TTL output. (See SDT description above.) An internal 50k pull-up resistor prevents "floating". Hold SDTSEL high for normal operation.
23	UNUSED	TTL Input	This pin must be connected to VCC.
27	UNUSED	Output	This pin should be left unconnected.

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Power Supply Pins

Pin #	Name	Type	Description
5,10,18,20, 28,29,37,42, 50,53,55,57, 60,63	VDD	Power	Positive supply pins.
1,14,15,21, 25,32,33,46, 51,56,58,64	GND	Power	Ground supply pins.

7101 tbl 04

Electrical Specifications

Absolute Maximum Ratings⁽¹⁾

Parameter	Min.	Max.	Unit
DC Supply Voltage (V _{DD})	-0.5	+5	V
Terminal Voltage with respect to GND	-0.5	+5	V
Terminal Voltage with respect to V _{DD}		+0.5	V
Storage Temperature Range	-40°	+150°	Celsius

7101 tbl 05

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	DC supply voltage	3.15	3.3	3.45	V
T _A	Ambient Temperature	0		70	°C

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DC Electrical Characteristics (Includes all I/O pins except TXP, TXN, RXP, RXN)

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Unit
V _{IH} , TTL ⁽²⁾	TTL Input High Voltage		2.0		V _{DD} + 0.5	V
V _{IL} , TTL ⁽²⁾	TTL Input Low Voltage		-0.3		0.80	V
V _{IH} , PECL ⁽³⁾	PECL Input High Voltage	SDTSEL is low	V _{DD} - 1.165		V _{DD} + 0.5	V
V _{IL} , PECL ⁽³⁾	PECL Input Low Voltage	SDTSEL is low	-0.3		V _{DD} - 1.475	V
I _{IH}	Input High Current	V _{DD} = 3.45V, V _{IN} = 2.4V			40	μA
I _{IL}	Input Low Current	V _{DD} = 3.5V, V _{IN} = 0.4V	-600			μA
V _{OH}	Output High Voltage	V _{DD} = 3.15V, I _{OUT} = -400μA	2.2		V _{DD}	V
V _{OL}	Output Low Voltage	V _{DD} = 3.15V, I _{OUT} = 1mA	0		0.5	V
C _{IH}	Input Capacitance				4	pF
I _{DD}	Transceiver V _{DD} Supply Current	T _A = 25°		180		mA
V _{DD}	DC supply voltage		3.15	3.3	3.45	V
P _D	Power dissipation			570	890	mW

7101 tbl 07

NOTE:

- Test conditions are Recommended Operating Conditions unless otherwise noted.
- Not for SDT.
- For SDT only, when SDTSEL is logic low.

AC Electrical Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Unit
f _{BD} ⁽²⁾	Serial Baud Rate		1000	1250	1360	MBaud
f _{REF}	TCLK Reference Frequency			f _{BD} /10		MHz
f _{TOL}	TCLK Frequency Tolerance		-100		+100	ppm
t _{DC, TC}	TCLK Duty Cycle		40		60	%
t _{JT}	TCLK Jitter				40	ps RMS
t _{R, TC}	TCLK Rise Time	0.8V to 2.0V	0.7		2.4	ns
t _{F, TC}	TCLK Fall Time	2.0V to 0.8V	0.7		2.4	ns
f _{RCLK}	RCLK Frequency (77V7101)			f _{BD} /20		MHz
	RCLK Frequency (77V7111)			f _{BD} /10		MHz
t _{R, RC}	RCLK Rise Time	0.8V to 2.0V, C _L = 10pF	0.7		2.4	ns
t _{F, RC}	RCLK Fall Time	0.8V to 2.0V, C _L = 10pF	0.7		2.4	ns
t _{DC, RC}	RCLK Duty Cycle	1.4V to 1.4V, C _L = 10pF	40		60	%
t _{A-B}	RCLK ₀ to RCLK ₁ rising edge skew (77V7101)	1.4V to 1.4V, C _L = 10pF	7.5		8.5	ns
t _{R, RX} ⁽³⁾	RXCG Rise Time	0.8V to 2.0V, C _L = 10pF	0.7	1		ns
t _{F, RX} ⁽³⁾	RXCG Fall Time	0.8V to 2.0V, C _L = 10pF	0.7	1		ns
t _{SU, RX}	RXCG Setup Time to rising RCLK	{0.8,2.0}V to 1.4V, C _L = 10pF	2.5			ns
t _{HO, RX}	RXCG Hold Time from rising RCLK	1.4V to {0.8,2.0}V, C _L = 10pF	1.5			ns
t _{R, TX} ⁽³⁾	TXCG Rise Time	0.8V to 2.0V	0.7			ns
t _{F, TX} ⁽³⁾	TXCG Fall Time	0.8V to 2.0V	0.7			ns
t _{SU, TX}	TXCG Setup Time to rising TCLK	{0.8,2.0}V to 1.4V	2.0			ns
t _{HO, TX}	TXCG Hold Time to rising TCLK	1.4V to {0.8,2.0}V	1.0			ns
t _{LAT, TX} ⁽⁴⁾	Transmit Latency				16	ns
t _{LAT, RX} ⁽⁵⁾	Receiver Latency				34	ns
V _{SD}	Signal Detect Threshold		200	100		mV pk-pk
V _{IHS}	HS Input Differential Voltage		200		2000	mV pk-pk
V _{OHS}	HS Output Differential Voltage		1100		2000	mV pk-pk
V _{OHS, OFF}	HS Output Differential Off Voltage				170	mV pk-pk
t _{R, HS}	HS Output Differential Rise Time		85		327	ps
t _{F, HS}	HS Output Differential Fall Time		85		327	ps
J _{TOTAL} ⁽⁶⁾	Total Transmit Jiffer				192	ps pk-pk

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NOTES:

- Test conditions are Recommended Operating Conditions unless otherwise noted.
- 1250 Mbaud ±100ppm is the rate specified by IEEE 802.3z.
- IEEE does not specify code group maximum rise and fall times, but TXCG and RXCG inputs and outputs must meet the required setup and hold times.
- Transmitter latency is the time from the positive edge of TCLK that clocks in a particular transmit code group to the differential first edge of the first bit of that code group to be transmitted at TXP/N. Reference levels are 1.4V for TCLK, and zero-crossing for AC-coupled TXP-TXN.
- Receiver latency is the time from the differential first edge of the first bit of a particular code group received at RXP/N to the positive edge of the RCLK output (RCLK₀ or RCLK₁) that clocks out that code group. Reference levels are 1.4V for RCLK and zero-crossing for AC-coupled RXP-RXN.
- Total jitter at this component level is specified by IEEE 802.3z at TP1, as they define test points. See subclauses 38.5, 38.6.8-9, and 39.3.3 for system level specifications and measurement methods.

Timing Diagrams

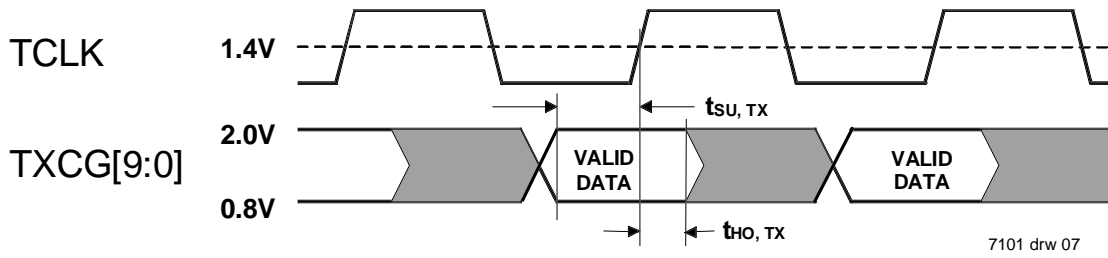


Figure 6. Transmit Parallel Interface Timing Diagram

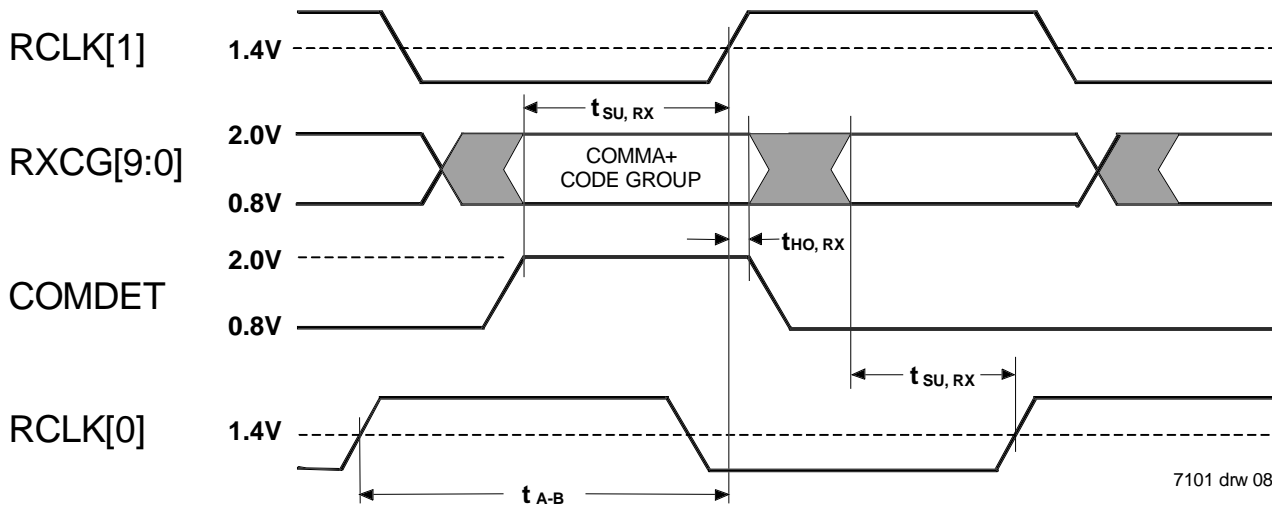


Figure 7. Receive Parallel Interface Timing Diagram (V7101)

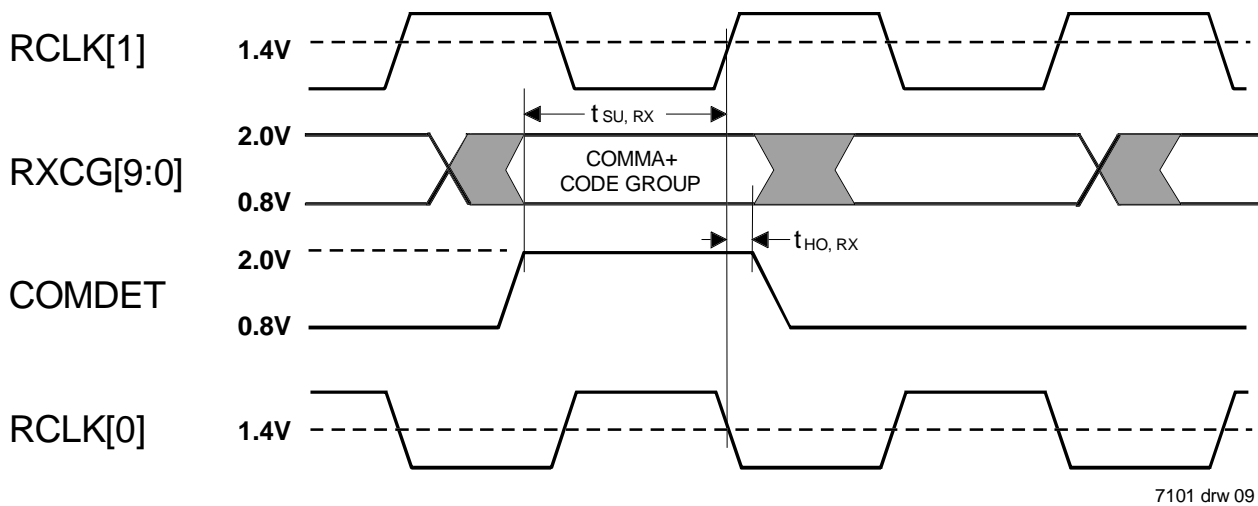
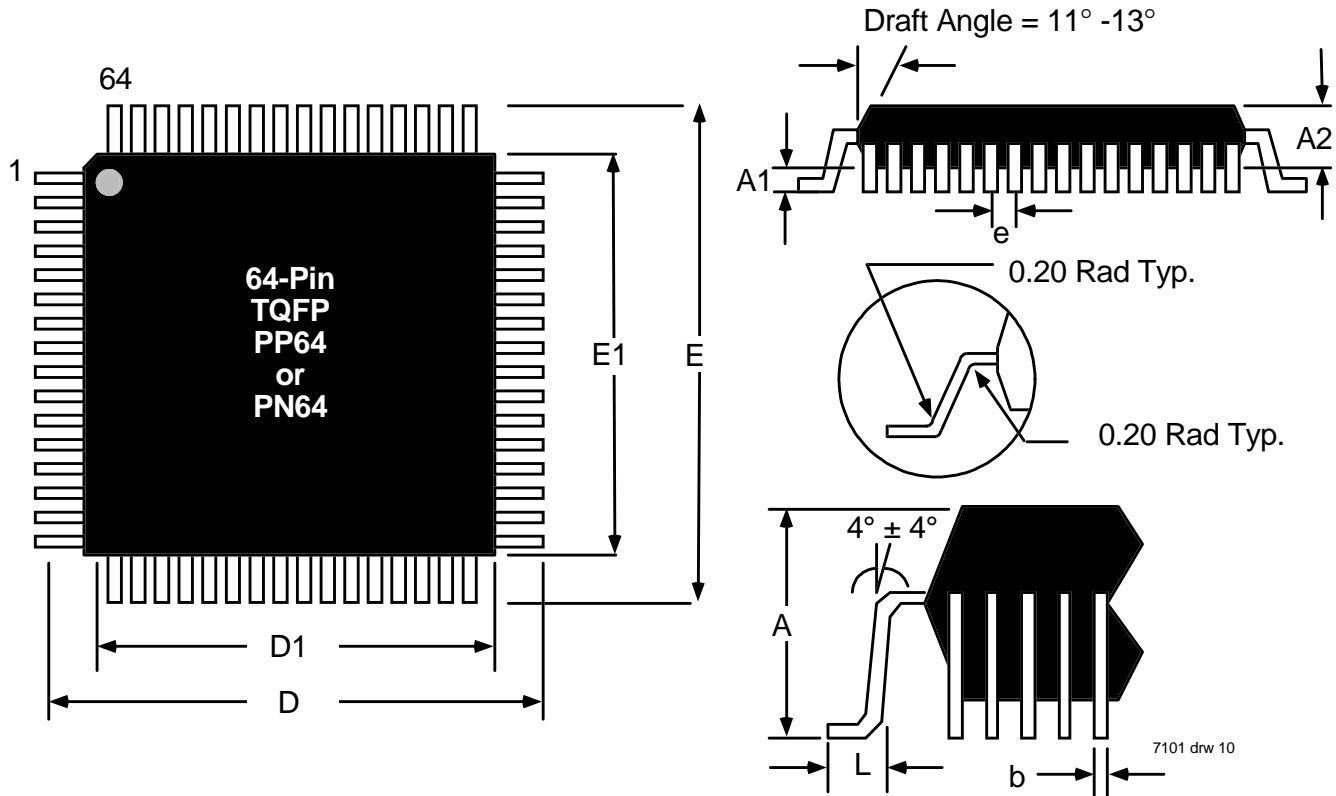


Figure 8. Receive Parallel Interface Timing Diagram (V7111)

Package Dimensions



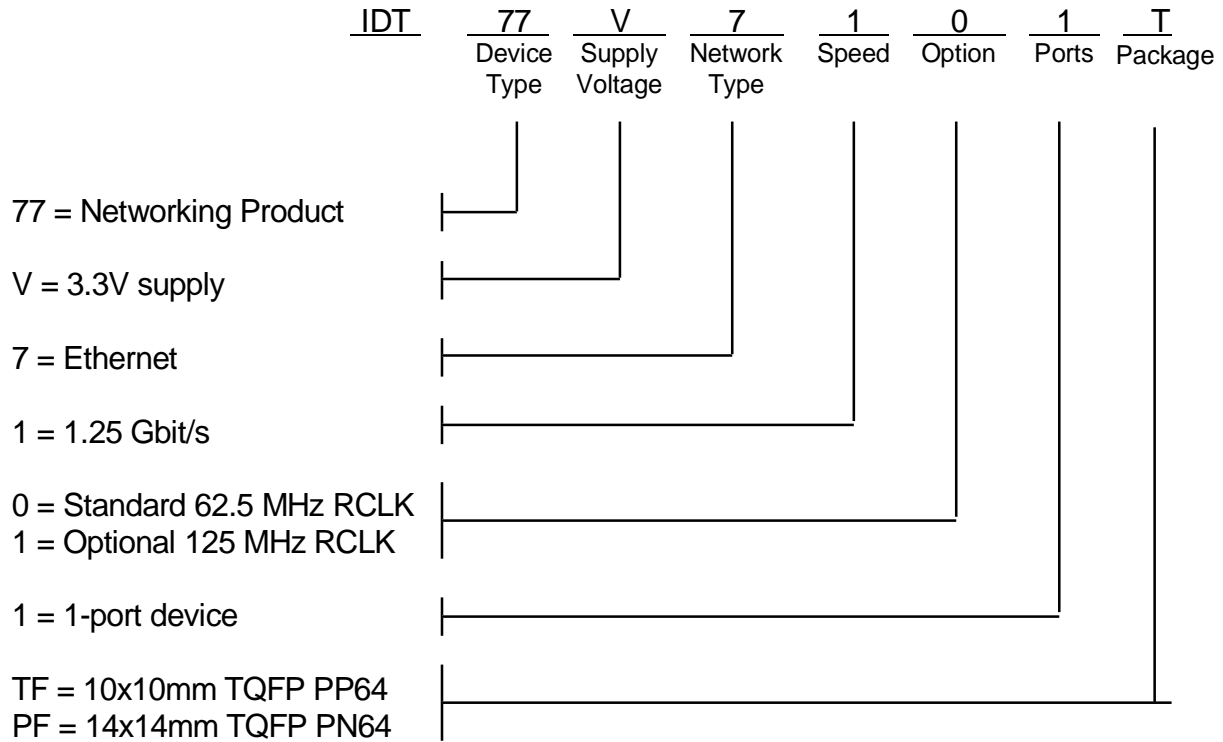
SYMBOL	PP64			PN64		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	1.60
A1	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45
D	—	12.00	—	—	16.00	—
D1	—	10.00	—	—	14.00	—
E	—	12.00	—	—	16.00	—
E1	—	10.00	—	—	14.00	—
L	0.45	—	0.75	0.45	—	0.75
e	—	0.50	—	—	0.80	—
b	0.17	0.22	0.27	0.30	0.37	0.45

Dimensions are in millimeters

7101 tbl 09

A more comprehensive package outline drawing is available from the IDT website.

Ordering Information



Preliminary Datasheet: Definition

"PRELIMINARY" datasheets contain descriptions for products soon to be, or recently released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.



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