GMM2732233DTG

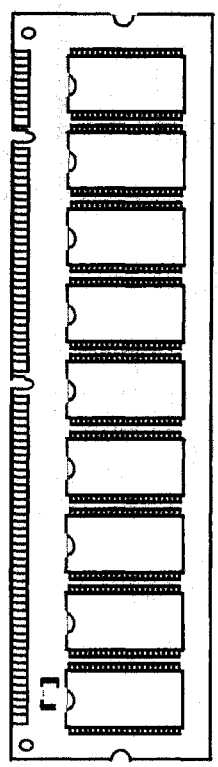
2,097,152 WORDS x72BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2732233DTG is a 2M x 72bits Synchronous Dynamic RAM MODULE which is assembled 9 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2732233DTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2732233DTG provides common data inputs and outputs.

- **GMM2732233DTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

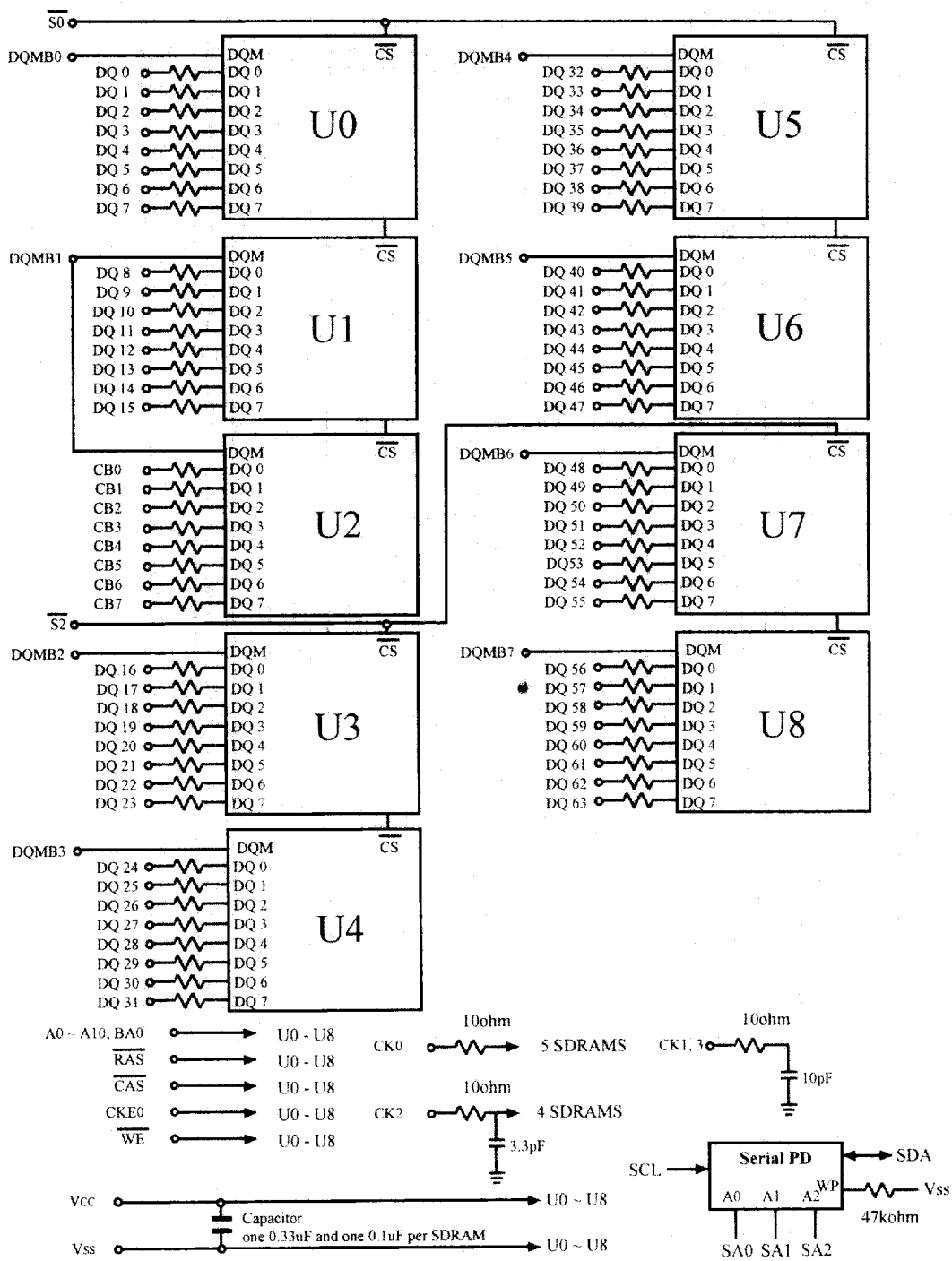
CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0, 2}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=7.5ns	75h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	x8	08h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=10ns	A0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=6.0ns	60h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=14ns	0Eh	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=48ns	30h	
31	Module Bank Density	16MBytes	04h	
32	Command & address signal input setup time	t_{CS} = 2ns	20h	
33	Command & address signal input hold time	t_{CH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
36~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev. 1.2	01h	
63	Checksum for bytes 0 ~ 62		C6h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2732233DTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			32h	2
80			32h	2
81			33h	3
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			44h	D
84			54h	T
85			47h	G
86			2Dh	-
87			37h	7
88			4Ah	J
89			20h	null
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		AFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	Vss, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-75		-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current		I_{CC1}	-	900	-	900	-	765	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	18	-	27	-	27	mA	CKE=V_{IL}, t_{CK}=min	5
		I_{CC2}	-	18	-	18	-	18	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
		(100MHz)	-	360	-	360	-	315	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
		(133MHz)	-	495							
Active standby current (Bank Active)		I_{CC3}	-	63	-	63	-	63	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
		(100MHz)	-	405	-	405	-	360	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
		(133MHz)	-	540							
Burst operating current	(CL=1)	I_{CC4}	-	-	-	585	-	495	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=2)		-	1350	-	900	-	765	mA		
	(CL=3)		-	1710	-	1350	-	1125	mA		
Refresh current		I_{CC5}	-	765	-	765	-	630	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	3.6	-	18	-	18	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V ≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	-10	10	μA	0 ≤ Vin ≤ Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	-10	10	μA	0 ≤ Vout ≤ Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB1)	-	TBD	pF	1, 2
C_{I6}	Input capacitance (DQMB0, 2, 3, 4, 5, 6, 7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-75		-10		-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	-	-	30	-	36	-	ns	1
	(CL=2)	t_{CK}	10	-	15	-	18	-		
	(CL=3)	t_{CK}	7.5	-	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	-	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	6	-	9	-	12		
	(CL=3)	t_{AC}	-	6	-	7.5	-	9		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	-	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	6	-	7	-	9		
Data-in setup time		t_{DS}	2	-	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	3	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	90	-	100	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	60	120000	70	120000	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	-75		-10		-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	20	-	30	-	30	-	ns	1
Precharge to active command period	t_{RP}	20	-	30	-	30	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	10	-	15	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	20	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

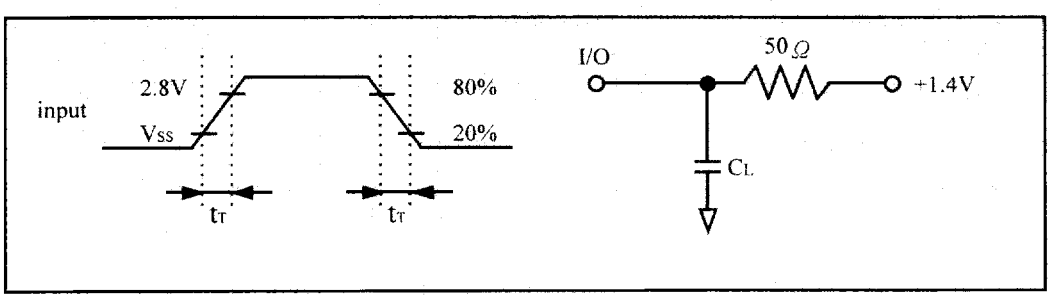
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-75		-10			-12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	10	7	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	5	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	2	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

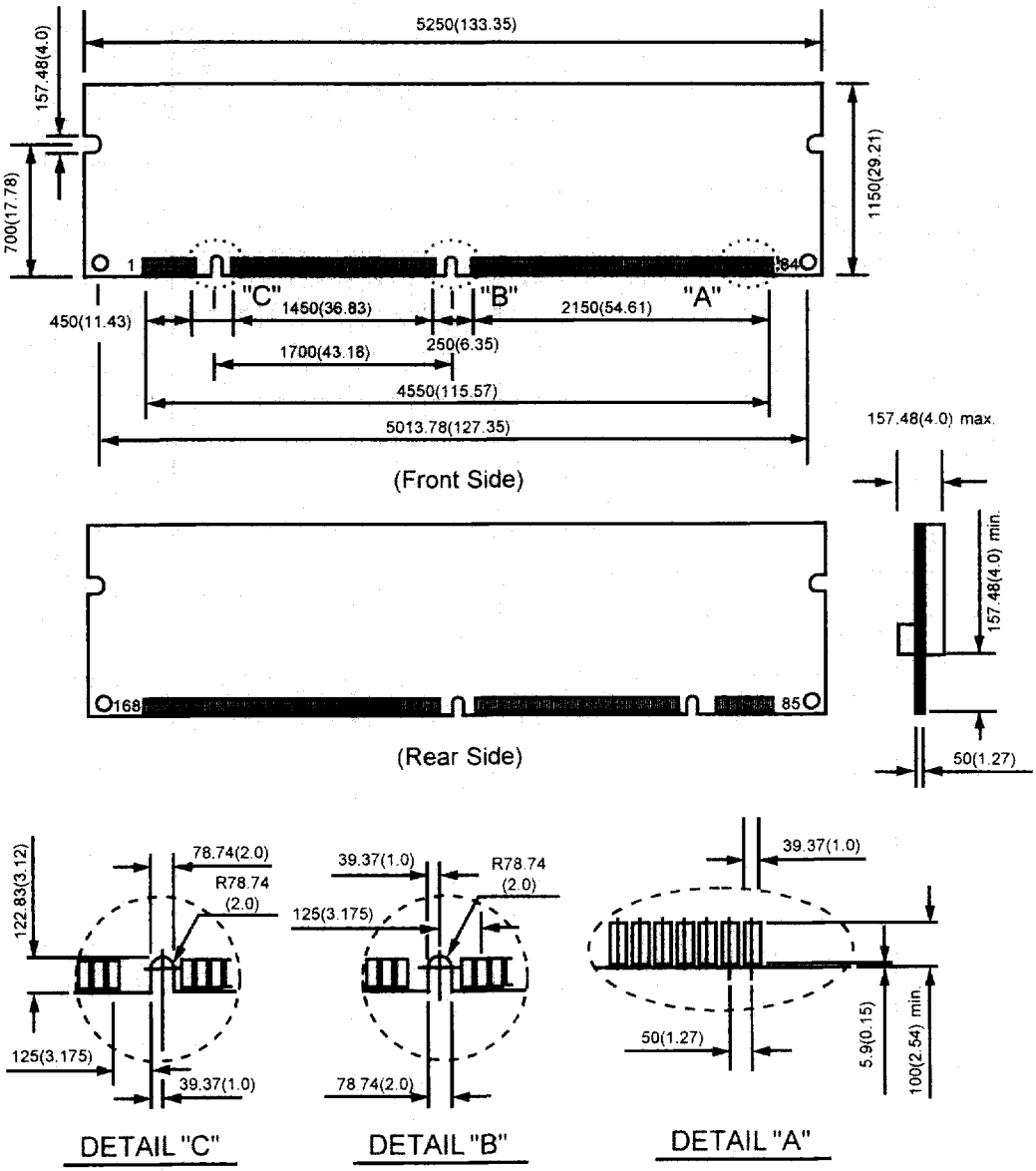
Parameter		Symbol	-75		-10			-12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.

2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ± 5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.