

SONY**CXB1159Q-Y****High-Speed Programmable Delay Line/Duty Cycle Controller** T-47-17**Description**

The CXB1159Q-Y is an ultra high-speed Programmable Delay Line/Duty Cycle Controller IC. Two types of delay length settings are provided, coarse (rough step length) and fine (detailed step length).

The coarse step can be set in approximately 160ps increments up to 128 steps by select input lines C0 to C6. The fine step can be set in approximately 5ps increments up to 64 steps by select input lines F0 to F5.

The duty cycle adjustment can be controlled just as the delay length settings through the step length select inputs.

Features

High-speed bipolar process provides for ultra high-speed operation.

- Rise and fall times: $T_{TLH}=220\text{ps}$ (Typ.)
 $T_{THL}=220\text{ps}$ (Typ.)
- Maximum delay range: 20.6ns (Typ.)
- Resolution: 5ps (Typ.)
- Maximum input frequency: $f_{INMAX}=800\text{MHz}$ (Min.)
- Input/output interface: ECL10KH Compatible
- Power dissipation: $P_d=780\text{mW}$ (Typ.)

Absolute Maximum Ratings

- Supply voltage V_{EE} -7.0 to +0.3 V
- Input voltage V_{IN} V_{EE} to 0.5 V
- Differential input voltage V_{ID} $|\overline{DIN}-DIN|$ 0 to 2.5 V
 $|DINP-\overline{DINP}|$
- Operating case temperature T_c -55 to +125 °C
- Storage temperature T_{stg} -65 to +150 °C

Recommended Operating Conditions

- Supply voltage V_{EE} -5.46 to -4.94 V
- Operating case temperature T_c 0 to 85 °C

32 pin QFP (Metal)

**Application**

Performance of timing and pulse width adjustment, and waveform shaping make this IC very suitable for high-speed digital signal processing applications such as in instruments, high-speed testers, and optical fiber communications.

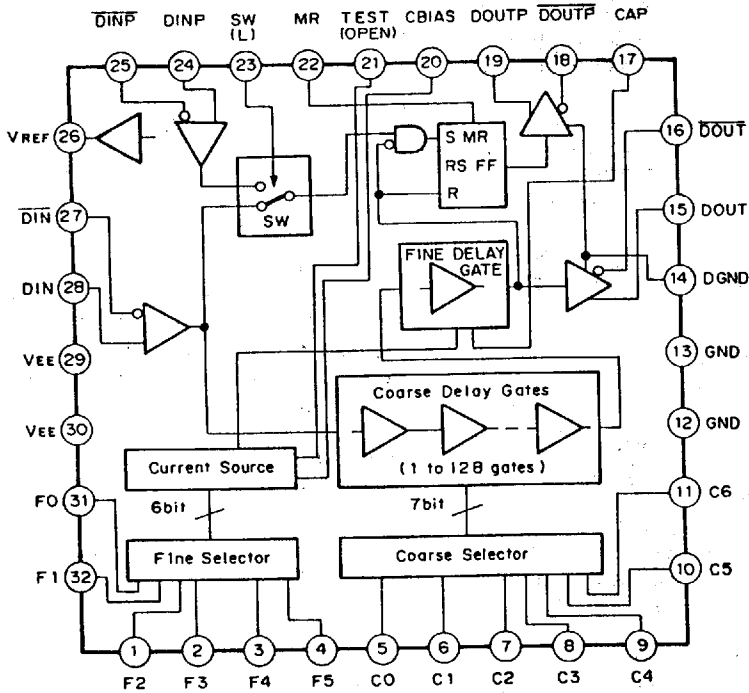
Structure

Bipolar silicon monolithic IC

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Block Diagram and Pin Configuration

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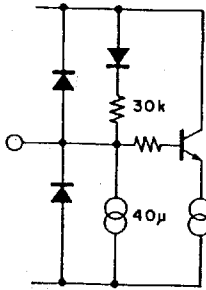
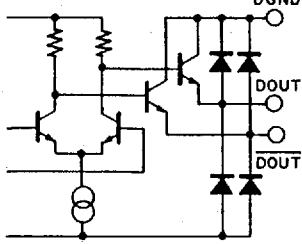
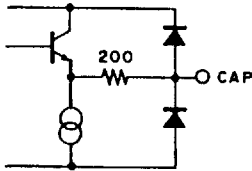


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Pin Description

Pin No.	Symbol	Pin voltage typ. (V)		Resistance (Ω)	Equivalent circuit	Description
		DC	AC			
31	F0		-1.8 to -0.8	30k		<p>Pin for setting fine delay time. "Low" (approx. -2V) when open. Longer delay time is achieved by changing F5 from "Low" to "High" at MSB.</p> <p>Pin for setting coarse delay time. "Low" (approx. -2V) when open. Longer delay time is achieved by changing C6 from "Low" to "High" at MSB.</p>
32	F1					
1	F2					
2	F3					
3	F4					
4	F5					
5	C0					
6	C1					
7	C2					
8	C3					
9	C4					
10	C5					
11	C6					
12	GND	0				GND
13						
14	DGND	0				<p>GND for output transistor. Collectors for DOUTP/DOUTP are also connected.</p> <p>Delay line output.</p>
15	DOUT					
16	DOUT					
17	CAP	-2.4		200		<p>D/A converter output. The ramp waveform of the fine delay circuit is compared with this output.</p>

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Pin No.	Symbol	Pin voltage typ. (V)		Resistance (Ω)	Equivalent circuit	Description
		DC	AC			
18	DOUTP					Duty cycle controller output.
19	DOUTP		-1.80 to -0.86			
20	CBIAS	-0.4	—	10k		Pin for connecting capacitor for oscillation prevention.
21	TEST	-1.4				Test
22	MR					Reset pin for duty cycle controller. "Low" (approx. -2V) when open.
23	SW		-1.8 to -0.8	30k		Input signal select pin for duty cycle controller. "Low" (approx. -2V) when open.
24	DINP					Input for duty cycle controller. Selected when SW is at "High".
25	DINF					"Low" (approx. -2V) when open.
26	VREF	-1.4				Reference voltage output.

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Pin No.	Symbol	Pin voltage typ. (V)		Resistance (Ω)	Equivalent circuit	Description
		DC	AC			
27	$\overline{\text{DIN}}$		-1.8 to -0.8			Delay line input. Also transmits to the duty cycle controller when SW is at "Low". No internal DC bias.
28	DIN					
29	V_{EE}	-5.2				Negative power terminal.
30						

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Electrical Characteristics

DC Characteristics ($V_{EE} = -5.2 \pm 5\%$, $GND = DGND = 0V$, $V_{TT} = -2.0V$, $T_c = 0$ to $85^\circ C$, $R_T = 50\Omega$ to V_{TT})

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		-210	-150	-110	mA
"H" level input voltage	V_{IH}		-1.08			V
"L" level input voltage	V_{IL}				-1.6	
"H" level input current for control pin	I_c	Cn, Fn, MR, SW		45	100	μA
"H" level input current for DINP/DINP	I_{DP}			45	100	
"H" level input current for DIN/DIN	I_D				10	
"H" level output voltage	V_{OH}		-1035	-865	-700	mV
"L" level output voltage	V_{OL}		-1980	-1800	-1610	
Reference voltage	V_{REF}		-1500	-1385	-1270	

AC Characteristics ($V_{EE} = -5.2 \pm 5\%$, $GND = DGND = 0V$, $V_{TT} = -2.0V$, $T_c = 0$ to $85^\circ C$, $R_T = 50\Omega$ to V_{TT})

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{dLH}	Cn=L	0.8	1.4	2.0	ns
	T_{dHL}	Fn=L	0.8	1.4	2.0	
	T_{dLH}	Cn=H	16.0	22.0	28.0	
	T_{dHL}	Fn=H	16.0	22.0	28.0	
	T_{pLH}	SW=L	0.8	1.4	2.0	
	T_{pHL}	Cn=L, Fn=L	1.0	1.7	2.5	
		Cn=H, Fn=H	16.0	22.0	28.0	
	T_{ppLH}	SW=H	0.8	1.4	2.0	
	T_{ppHL}	Cn=L, Fn=L	1.0	1.7	2.5	
		Cn=H, Fn=H	16.0	22.0	28.0	
Min. pulse width	T_{pw}	Cn=L, Fn=L			1.0	
Resolution	T_{res}			5	8	ps
Max. input frequency	f_{inMAX}	DIN/DIN, DINP/DINP	800			MHz
Rise time	T_{TLH}	20 to 80%		220	350	ps
Fall time	T_{THL}			220	350	
Jitter	$T\sigma$	Cn=H, Fn=H		7		

Standard delay time is calculated using the approximated formula below:

$$T_d (\text{ns}) = (1.4 + 0.16M) \{1 + K_c (T_c - 25)\} + 0.004N \{1 + K_f (T_c - 25)\}$$

$$M = 2^6 \cdot C_8 + 2^5 \cdot C_5 + 2^4 \cdot C_4 + 2^3 \cdot C_3 + 2^2 \cdot C_2 + 2^1 \cdot C_1 + 2^0 \cdot C_0$$

$$N = 2^5 \cdot F_5 + 2^4 \cdot F_4 + 2^3 \cdot F_3 + 2^2 \cdot F_2 + 2^1 \cdot F_1 + 2^0 \cdot F_0$$

(Cn and Fn are control signals. When "H", substitute "1". When "L", substitute "0".)

$$K_c = 0.0013$$

$$K_f = 0.0006$$

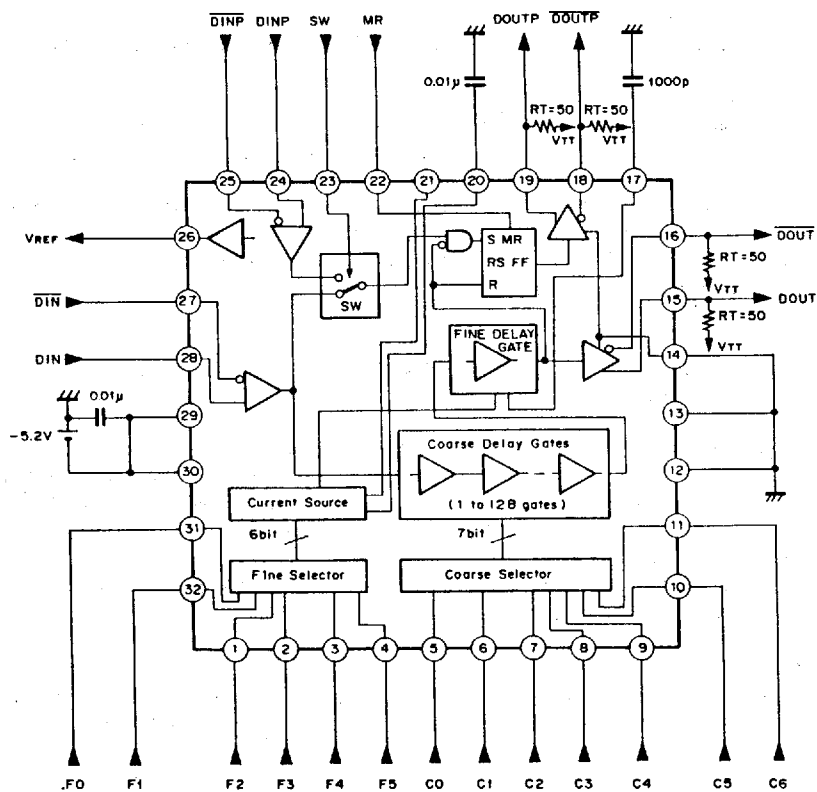
Tc: Case Temperature

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Electrical Characteristics Test Circuit

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Description of Operation

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Coarse Delay Block

This coarse delay block uses gates for a coarse delay control of input signals. The delay time covered by one step is approximately 160ps. With a total of 128 steps, the delay length can be set with the 7-bit digital control signals.

Conventional systems select the bus for gate passage by using a multiplexer. This approach has the following disadvantages:

- (1) To delay high speed signals, the number of multiplexers must equal that of the gates (if the number of gates is assumed to be 2^n , 2^n-1 multiplexers will be needed), and be capable of the same high-speed operation. Thus, resulting in high power consumption.
- (2) A long insertion time is required so that the delayed signals can pass through the multiple multiplexer stages (if the gate number is assumed to be 2^n , the number of multiplexer stages is n).
- (3) Because of the large number of multiplexers in the configuration, from the aspect of the system layout, the delay time has poor linearity characteristics.

As the result of the newly developed circuit system, this product has overcome all of these disadvantages and achieved superior linearity characteristics. The figure below shows the actual output waveform.

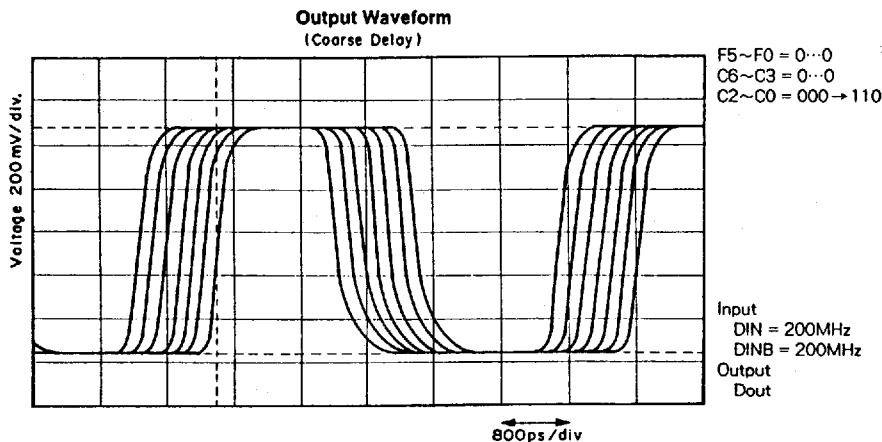
Fine Delay Block

This delay control block provides fine adjustment for the input signal delay control. Each step covers a delay time of approximately 5ps. With the total of 64 steps, the delay length can be set with the 6-bit digital control signals. Fine delay adjustment is possible within a total variation range of approximately 250ps. Since the coarse delay control steps are approximately 160ps, a resolution of approximately 5ps can be achieved, through overlapping in a total range of approximately 20ns.

This block uses circuits delaying the respective positions for the leading and trailing edges of the input signal. As a result, it is possible to delay the input signals by maintaining their pulse width.

Duty Cycle Controller

RS-FF is set at the leading edge of the input signal and the pulse is generated by resetting the leading edge of the output signal obtained by setting the digital control signal. Cascade connection of multiple ICs expands the pulse width even further.



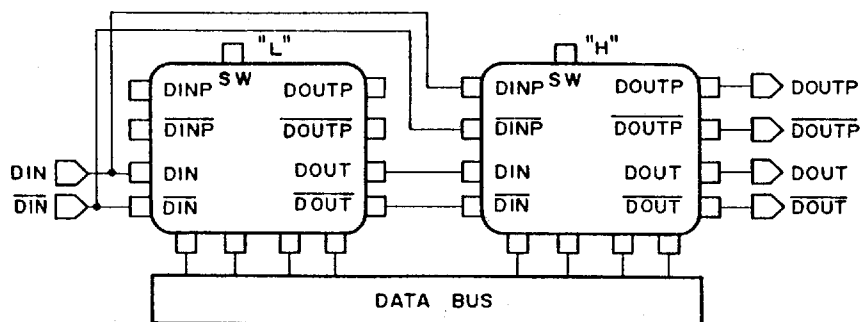
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Notes on Operation

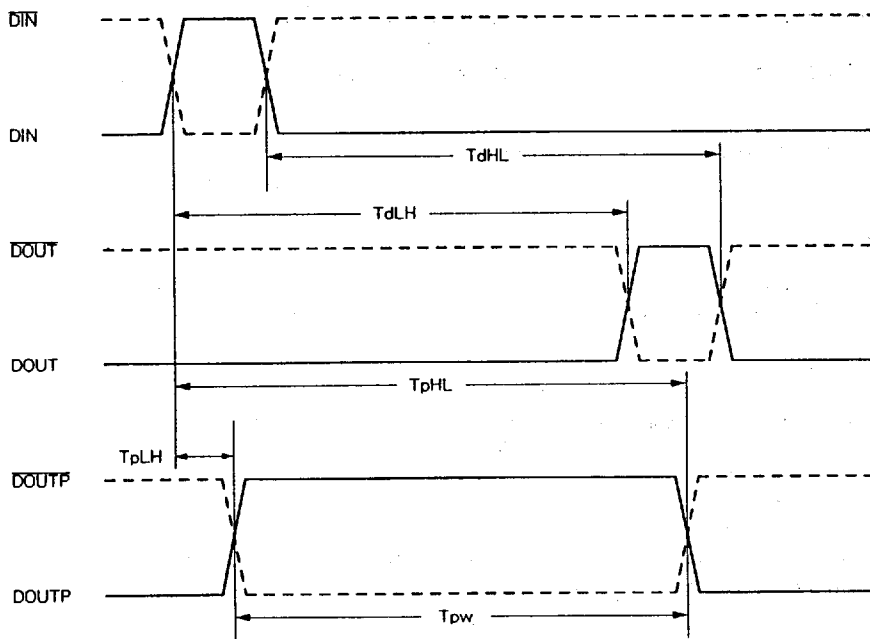
1. The complementary input/output must be used to take advantage of this IC's capabilities.
2. Since Pin 28 (DIN) and Pin 27 ($\overline{\text{DIN}}$) are not DC biased, an external complementary ECL output buffer should be connected.
3. Pins 15, 16, 18 and 19 ($R_T=50\Omega$) are terminated to V_{TT} (-2V).
4. For Pins 24, 25, 27, and 28, signals should be input when the rise and fall times (20%–80%) are 5ns or below.
5. The duty cycle controller pulse width can be widened by employing a multiple IC configuration. Pin 23 (SW) should be set accordingly to accommodate this configuration. Refer to the Application Circuit.
6. Pin 21 (TEST) should normally be left open.
7. A decoupling capacitor should be connected to Pins 17 (CAP) and 20 (CBIAS) with values respective to GND as follows:
Pin 17 1000pF
Pin 20 $\geq 0.01\mu\text{F}$
8. Ensuring that the Supply/GND lines of the IC are adequately sunk is desirable. Please provide decoupling capacitors near the pins of the IC as much as possible.

Application Circuit – Cascade connection

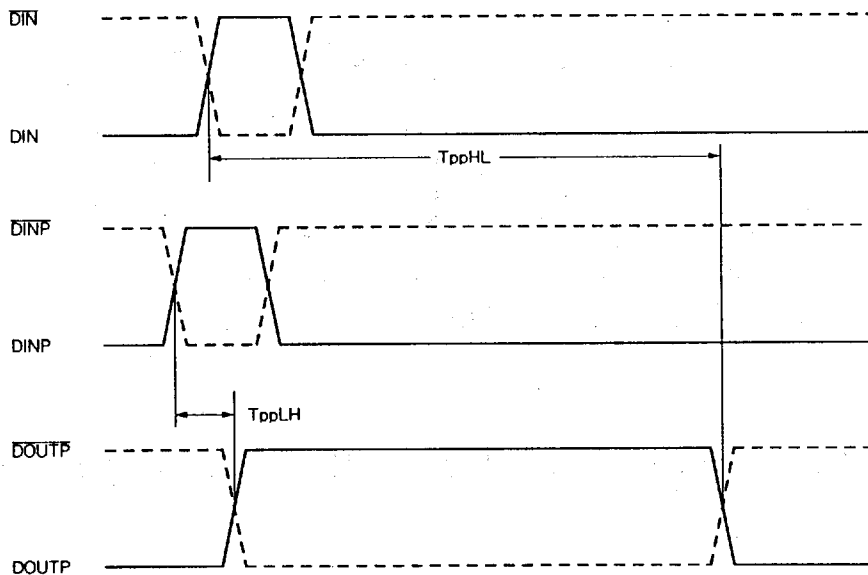
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

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Output Timing (SW="L")



Output Timing (SW="H")

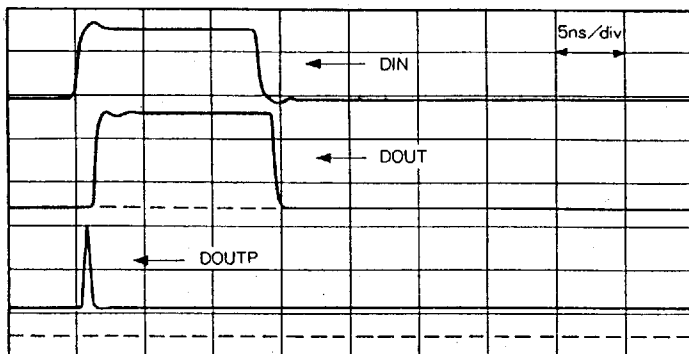


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Example of Representative Characteristics

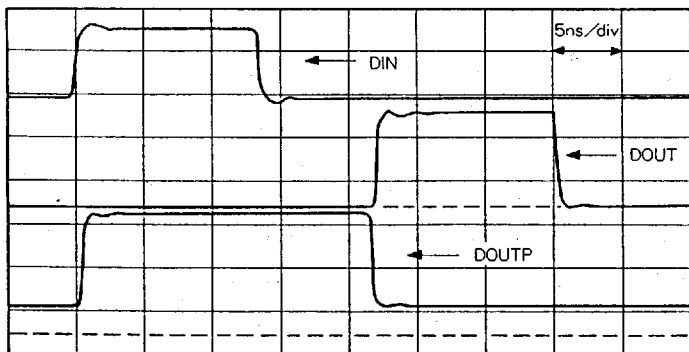
Output Waveform

Operating Waveforms of Delay Line and Duty Cycle Controller



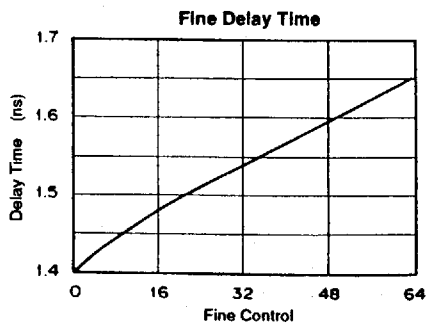
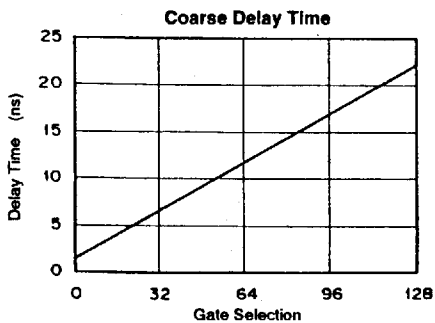
CONDITION (A)

C6 = ... = C0 = F5 = ... = F0 = "L"

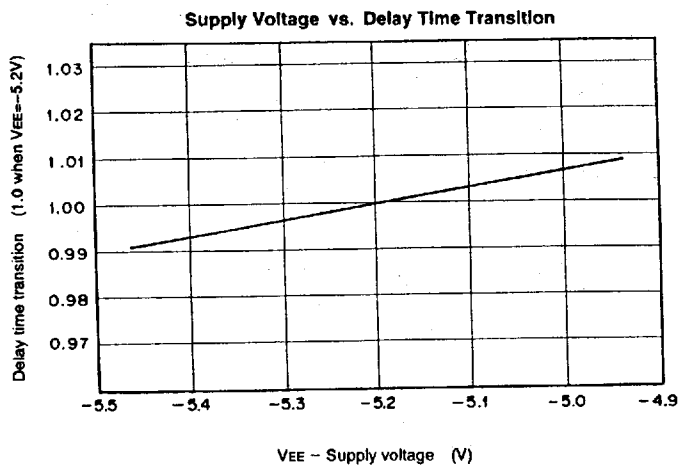
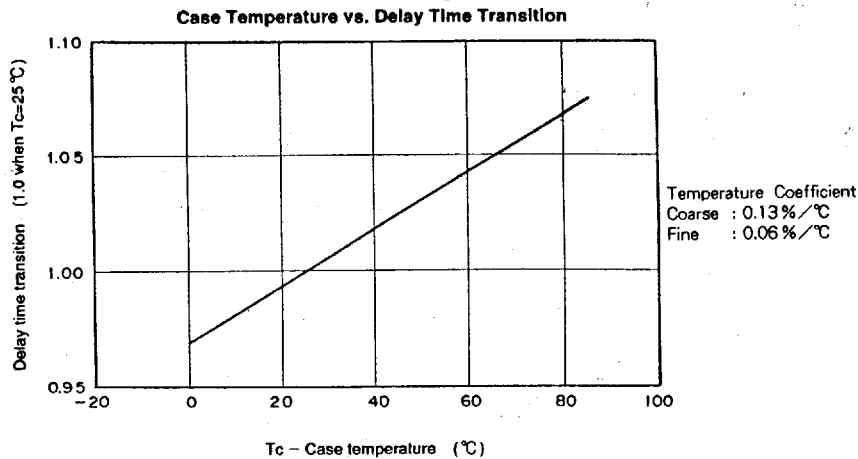


CONDITION (B)

C6 = ... = C0 = F5 = ... = F0 = "H"



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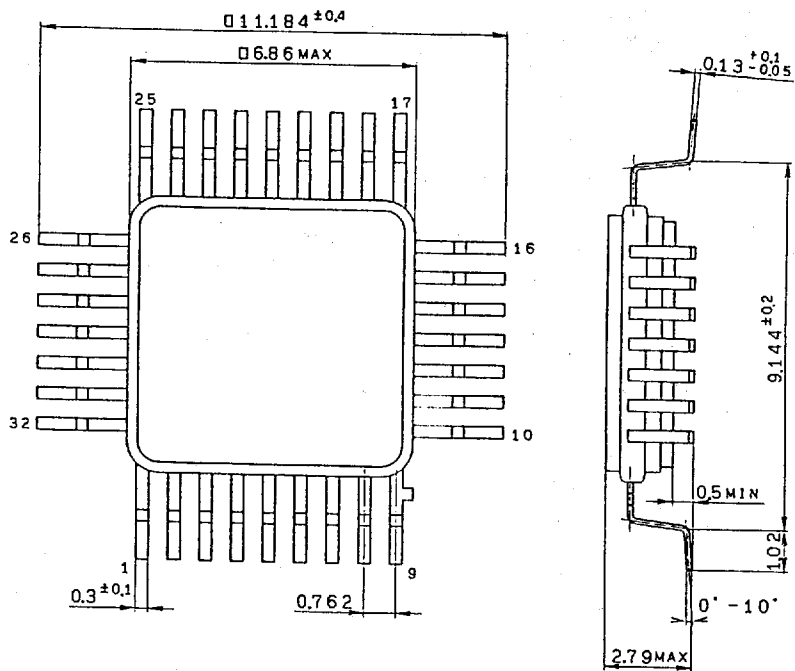
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Package Outline Unit: mm

32pin GFP (Metal)



SONY NAME	GFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	

Package Data

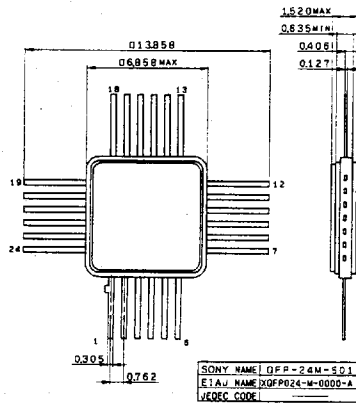
T-90-20

Package Outline

Unit: mm

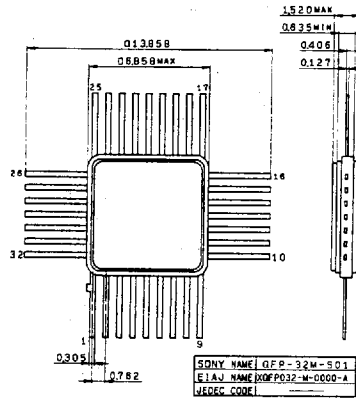
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



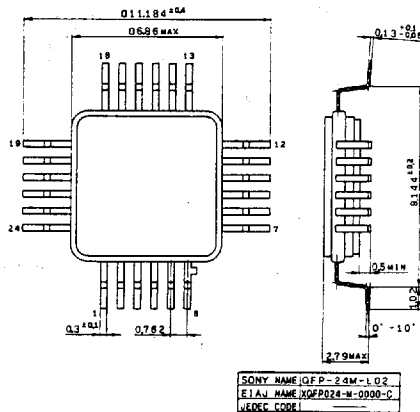
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



24pin QFP (QFP-24M-L02)

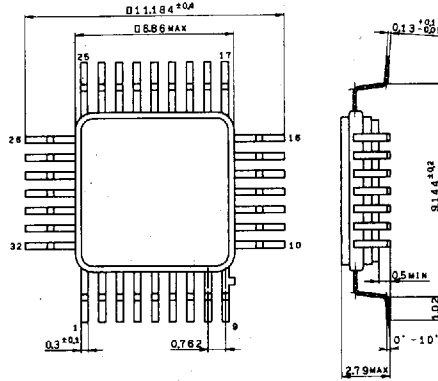
24pin QFP (Metal) 0.3g



T-90-20

32pin QFP (QFP-32M-L02)

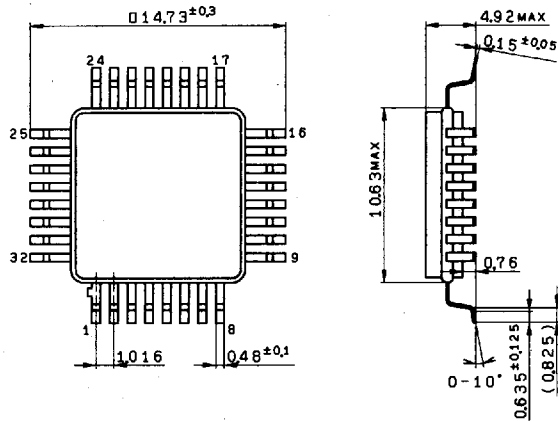
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	

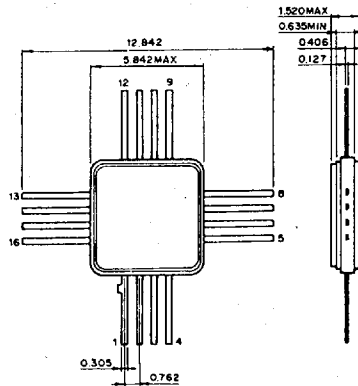
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	

16pin QFP



Package Data

Package Data	Page
1. 16 pin QFP	6-3
2. 24 pin QFP	6-3
3. 32 pin QFP	6-3
4. 24 pin QFP with formed lead	6-4
5. 32 pin QFP with formed lead	6-4

Package Data

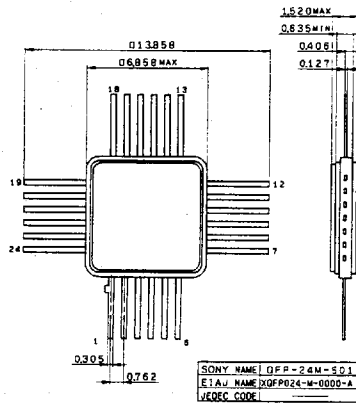
T-90-20

Package Outline

Unit: mm

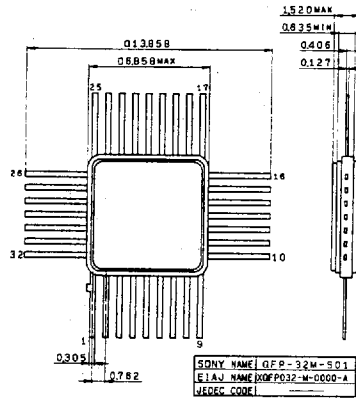
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



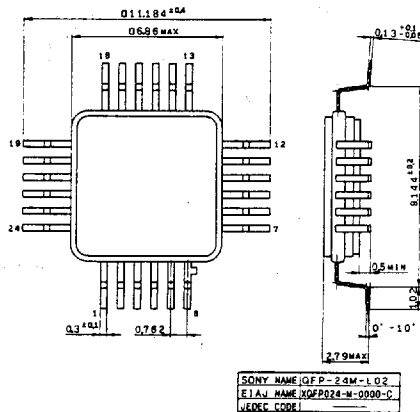
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



24pin QFP (QFP-24M-L02)

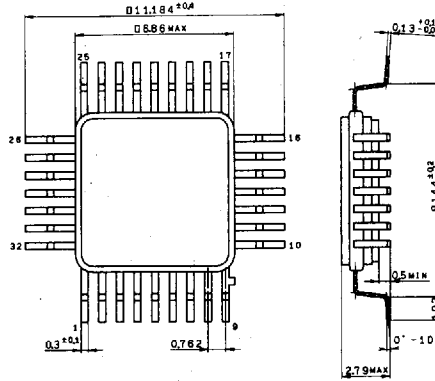
24pin QFP (Metal) 0.3g



T-90-20

32pin QFP (QFP-32M-L02)

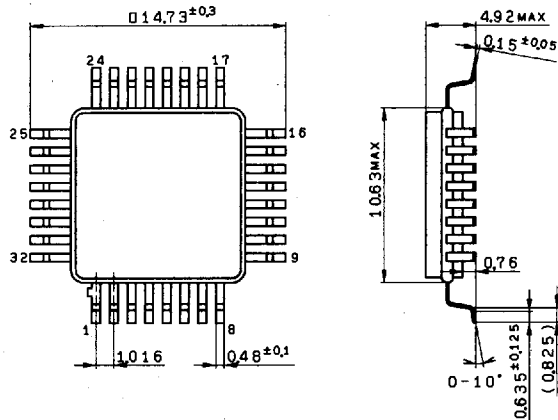
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	

16pin QFP

