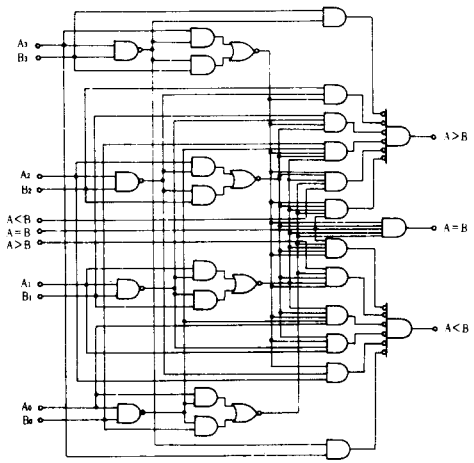
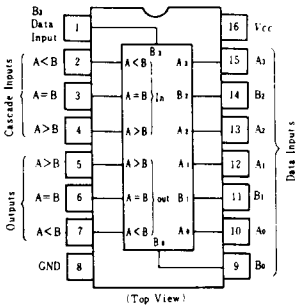
HD74LS85 ●4-bit Magnitude Comparators

This four bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. This device is fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A>B, A<B, and A=B outputs of a stage handling less-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the AßB input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■FUNCTION TABLE

Inputs				Cascading inputs			Outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	A<B	A<B	A=B	A>B	A<B	A=B
$A_3 > B_3$	×	×	×	×	×	×	H	L	L
$A_3 < B_3$	×	×	×	×	×	×	L	H	L
$A_3 = B_3$	$A_2 > B_2$	×	×	×	×	×	H	L	L
$A_3 = B_3$	$A_2 < B_2$	×	×	×	×	×	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	×	×	×	×	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	×	×	×	×	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	×	×	×	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	×	×	×	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	×	×	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H; high level, L; low level, X; irrelevant

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=4mA$	–	–	0.4	V
			$V_{IL}=0.8V$	$I_{OL}=8mA$	–	–	0.5	
Input current	A<B, A>B Inputs	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	Other inputs				–	–	60	
	A<B, A>B Inputs	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	Other inputs				–	–	−1.2	
	A<B, A>B Inputs	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	Other inputs				–	–	0.3	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current **		I_{CC}	$V_{CC}=5.25V$		–	10.4	20	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

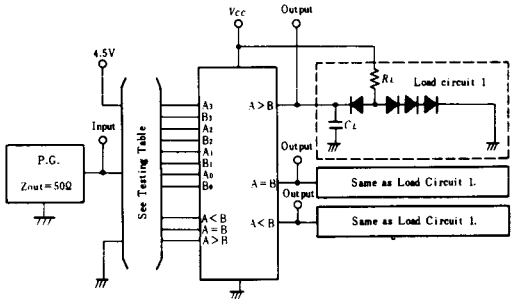
** I_{CC} is measured with outputs open, A=B grounded, and all other inputs at 4.5V.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Number of gate levels	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	Any A or B data Input	A<B, A>B	1	$C_L=15pF$, $R_L=2k\Omega$	–	14	–	ns
				2		–	19	–	
				3		–	24	36	
			A=B	4		–	27	45	
	t_{PHL}	Any A or B data Input	A<B, A>B	1		–	11	–	ns
				2		–	15	–	
				3		–	20	30	
			A=B	4		–	23	45	
	t_{PLH}	A<B or A=B	A>B	1		–	14	22	ns
	t_{PHL}	A<B or A=B	A>B	1		–	11	17	ns
	t_{PLH}	A=B	A=B	2		–	13	20	ns
	t_{PHL}	A=B	A=B	2		–	13	26	ns
	t_{PLH}	A>B or A=B	A<B	1		–	14	22	ns
	t_{PHL}	A>B or A=B	A<B	1		–	11	17	ns

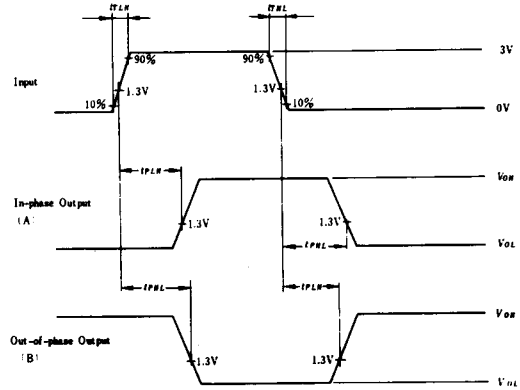
■TESTING METHOD

1) Test Circuit



Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle=50%
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

Waveform



2) Testing Table

Item	Inputs											Output Waveforms		
	A_3	B_3	A_2	B_2	A_1	B_1	A_0	B_0	A>B	A=B	A<B	A>B	A=B	A<B
	IN	4.5V	4.5V	GND	GND	GND	GND	GND	GND	GND	GND	A	–	B
	4.5V	IN	GND	4.5V	GND	GND	GND	GND	GND	GND	GND	B	–	A
	GND	GND	IN	4.5V	4.5V	GND	GND	GND	GND	GND	GND	A	–	B
	GND	GND	4.5V	IN	GND	4.5V	GND	GND	GND	GND	GND	B	–	A
	GND	GND	GND	GND	IN	4.5V	4.5V	GND	GND	GND	GND	A	–	B
	GND	GND	GND	GND	4.5V	IN	GND	4.5V	GND	GND	GND	B	–	A
t_{PLH}	GND	GND	GND	GND	GND	GND	IN	4.5V	4.5V	GND	GND	A	–	B
t_{PHL}	GND	GND	GND	GND	GND	GND	4.5V	IN	GND	GND	4.5V	B	–	A
	GND	GND	GND	GND	GND	GND	IN	4.5V	GND	4.5V	GND	–	A	B
	GND	GND	GND	GND	GND	GND	4.5V	IN	GND	4.5V	GND	B	A	–
	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	GND	–	–	B
	GND	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	B	A	B
	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	IN	B	–	–

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

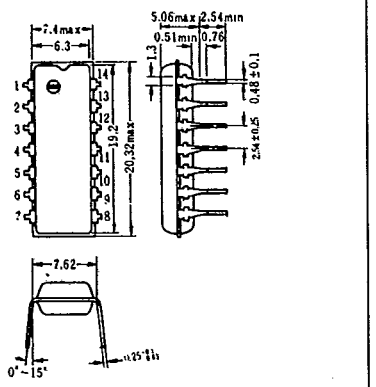
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

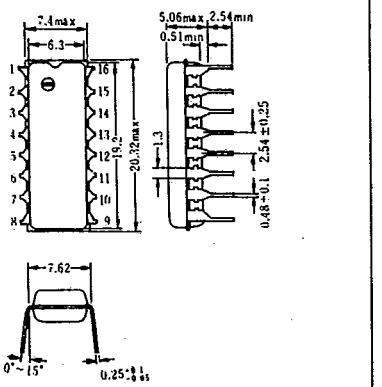
●14 Pin

DP-14



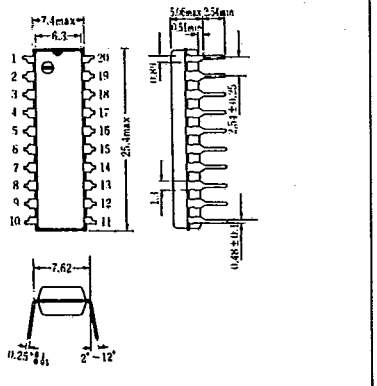
●16 Pin

DP-16



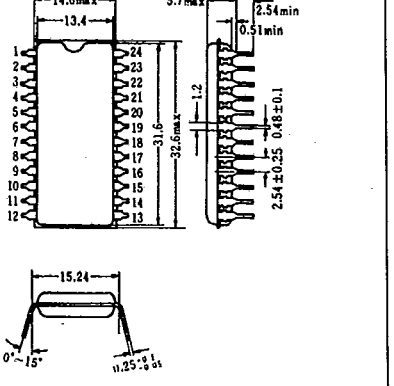
●20 Pin

DP-20



●24 Pin

DP-24

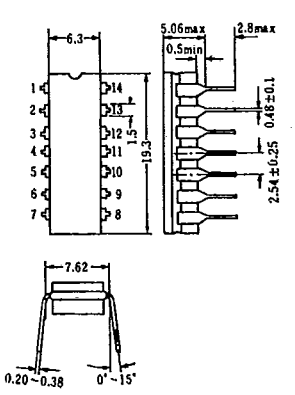


PACKAGING INFORMATIONS

■Cerdip

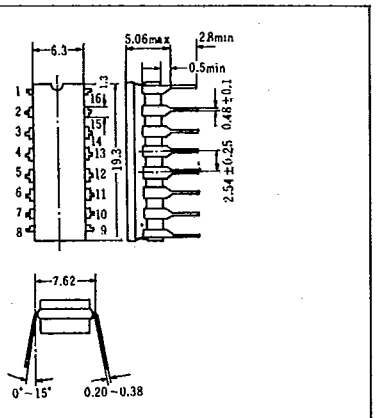
●14 Pin

DG-14



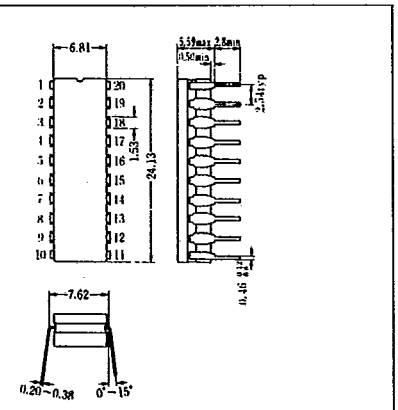
●16 Pin

DG-16



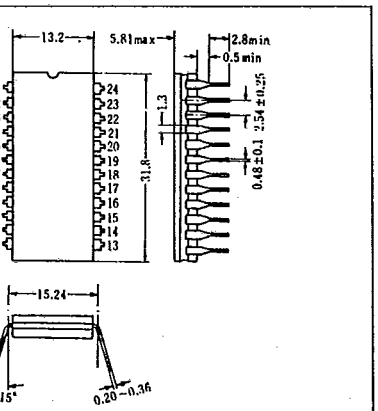
●20 Pin

DG-20



●24 Pin

DG-24



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