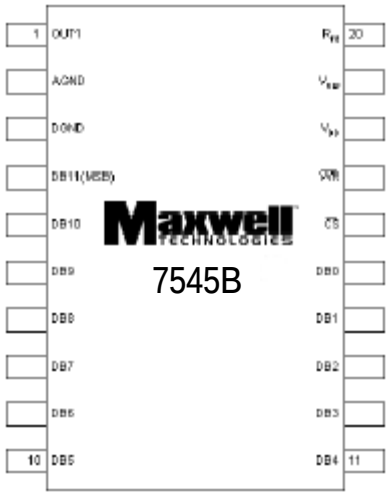
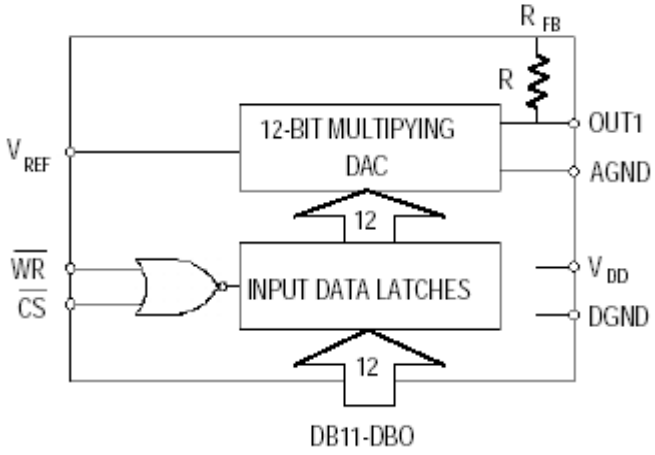
7545B
12-Bit Buffered Multiplying Digital to Analog Converter





BLOCK DIAGRAM

FEATURES:

- RAD-PAK® patented shielding against natural space radiation
- Total dose hardness:
  - > 50 krad (Si), depending upon space mission
- Excellent single event effects
  - SEL_{TH}: > 120 MeV/mg/cm^2
  - SEU_{TH}: > 120 MeV/mg/cm^2
- Package:
  - 20 pin RAD-PAK® Flat Pack
  - 20 pin RAD-PAK® DIP
- Low gain temperature coefficient:
  - 5 ppm/°C typ.
- Fast interface timing
- Single +5 V to +15 V supply

DESCRIPTION:

Maxwell Technologies' 7545B is a 12-bit CMOS-buffered multiplying DAC with internal data latches, which features a greater than 50 krad (Si) total dose tolerance, depending upon space mission. The 7545B features a $\overline{WR}$ pulse width of 100 ns which allows interfacing to a much wider range of fast 8-bit and 16-bit microprocessors. It is loaded by a single 12-bit wide word under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing unbuffered operation of the DAC. The 7545B is particularly suitable for single supply operations and applications with wide temperature variations.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 50 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

TABLE 1. 7545B PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	OUT 1	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB 11	Data Bit 11 (MSB)
5	DB 10	Data Bit 10
6	DB 9	Data Bit 9
7	DB 8	Data Bit 8
8	DB 7	Data Bit 7
9	DB 6	Data Bit 6
10	DB 5	Data Bit 5
11	DB 4	Data Bit 4
12	DB 3	Data Bit 3
13	DB 2	Data Bit 2
14	DB 1	Data Bit 1
15	DB 0	Data Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	WR	Write (Active Low)
18	V_{DD}	Digital Supply Voltage
19	V_{REF}	Reference Input
20	RFB	Feedback Resistance

TABLE 2. 7545B ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
V_{DD} to DGND	--	-0.3	17	V
Digital Input Voltage to DGND	--	-0.3	V_{DD} + 0.3	V
V_{RFB}, V_{REF} to DGND	--	--	25	V
V_{PIN1} to DGND	--	-0.3	V_{DD} + 0.3	V
AGND to DGND	--	-0.3	V_{DD} + 0.3	V
Power Dissipation to 75 ˚C	P_D	--	450	mW
Weight	Mass		2.75	grams
Thermal Impedance — Flat Package	Θ_{JC}	--	6.08	°C/W
Thermal Impedance — DIP Package	Θ_{JC}	--	6.04	°C/W
Operating Temperature	--	-55	125	˚C
Storage Temperature Range	T_S	-65	150	˚C

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{DD}	±10%

TABLE 4. 7545B SPECIFICATIONS

(V_{DD} = +5 V ±10%, T_A = -55 TO 125 ˚C UNLESS OTHERWISE NOTED)

TEST	SYMBOL	TEST CONDITION	SUBGROUPS	MIN	MAX	UNIT
Resolution	RES		1, 2, 3	12	--	Bits
Relative Accuracy	RA	V_{DD} = 5V	1, 2, 3	-1/2	1/2	LSB
Differential Nonlinearity	DNL	12-Bit Monotonic T_{MIN} to T_{MAX} V_{DD} = 5V	1, 2, 3	-1	1	LSB
Gain Error[1]	A_E	DAC Register Loaded with 1111 1111 1111; V_{DD} = 5V	1, 2, 3	-4	4	LSB
Gain Temperature Coefficient[2]	TC_{AE}		1, 2, 3	-5	5	ppm/˚C
Power Supply Rejection	PSRR	V_{DD} = +/-5%	1, 2, 3	-0.004	0.004	%/%
Output Current Settling Time[2]	t_{SL}	To 1/2LSB; OUT1 Load = 100Ω, DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS}$ = 0V	1, 2, 3	--	2	µs
Feed through Error	FT		1, 2, 3	5 (typical)		mV p-p
Reference Input Resistance (Pin 19 to Ground)	R_{IN}		1, 2, 3	10	25	KΩ
Digital Input High Voltage[4]	V_{IH}		1, 2, 3	2.4	--	V
Digital Input Low Voltage[4]	V_{IL}		1, 2, 3	--	0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{DD}	1, 2, 3	-10	10	µA
Digital Input Capacitance[2]	C_{IN}	DB0 - DB11; $\overline{WR}$, $\overline{CS}$	1, 2, 3	--	20	pF
Output Capacitance[2]	C_{OUT1}	DB0 - DB11 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0V	1, 2, 3	--	70	pF
		DB0 - DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V	1, 2, 3	--	200	
Chip Select to Write Setup Time[3]	t_{CS}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	9, 10, 11	380	--	nS
Chip Select to Write Hold Time[3]	t_{CH}		9, 10, 11	0	--	
Write Pulse Width[3]	t_{WR}		9, 10, 11	400	--	
Data Setup Time[3]	t_{DS}		9, 10, 11	210	--	
Data Hold Time[3]	t_{DH}		9, 10, 11	10	--	
Supply Current from V_{DD}	I_{DD}	All Digital Inputs V_{IL} or V_{IH}	1, 2, 3	--	2	mA
		All Digital Inputs 0 or V_{DD}	1, 2, 3	--	100	µA

1)Measured using feedback resistor
2) Guaranteed by design
3) Not Tested
4)Tested by application of signal

TABLE 5. 7545B SPECIFICATIONS

(V_{DD} = +15 V ±10%, T_A = -55 TO 125 °C UNLESS OTHERWISE NOTED)

TEST	SYMBOL	TEST CONDITION	Subgroups	MIN	MAX	UNIT
Relative Accuracy	RA	V_{DD} = 15V	1, 2, 3	-1/2	1/2	LSB
Differential Nonlinearity	DNL	12-Bit Monotonic T_{MIN} to T_{MAX} V_{DD} = 15V	1, 2, 3	-1	1	LSB
Gain Error[1]	A_E	DAC Register Loaded with 1111 1111 1111 V_{DD} = 15V	1, 2, 3	-4	4	LSB
Gain Temperature Coefficient[2]	TC_{AE}		1, 2, 3	-5	5	ppm/°C
Power Supply Rejection	PSRR	V_{DD} = 5%	1, 2, 3	-0.004	0.004	%/%
Output Current Settling Time[2]	t_{SL}	To 1/2LSB; OUT1 Load = 100Ω, DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS}$ = 0V	1, 2, 3	--	2	µs
Feed through Error	FT		1, 2, 3	5 (typical)		mV p-p
Reference Input Resistance (Pin 19 to Ground)	R_{IN}		1, 2, 3	10	25	KΩ
Digital Input High Voltage[4]	V_{IH}		1, 2, 3	13.5	--	V
Digital Input Low Voltage[4]	V_{IL}		1, 2, 3	--	1.5	V
Digital Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{DD}	1, 2, 3	-10	10	µA
Digital Input Capacitance[2]	C_{IN}	DB0 - DB11; $\overline{WR}$, $\overline{CS}$	1, 2, 3	--	15	pF
Output Capacitance[2]	C_{OUT1}	DB0 - DB11 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0V	1, 2, 3	--	70	pF
		DB0 - DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V	1, 2, 3	--	150	
Chip Select to Write Setup Time[3]	t_{CS}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	9, 10, 11	95	--	nS
Chip Select to Write Hold Time[3]	t_{CH}		9, 10, 11	0	--	
Write Pulse Width[3]	t_{WR}		9, 10, 11	95	--	
Data Setup Time[3]	t_{DS}		9, 10, 11	80	--	
Data Hold Time[3]	t_{DH}		9, 10, 11	5	--	
Supply Current from V_{DD}	I_{DD}	All Digital Inputs V_{IL} or V_{IH}	1, 2, 3	--	2	mA
		All Digital Inputs 0 or V_{DD}	1, 2, 3	--	100	µA

1) Measured using feedback resistor
2) Guaranteed by design
3) Not tested
4)Tested by application of signal

FIGURE 1. WRITE CYCLE TIMING DIAGRAM

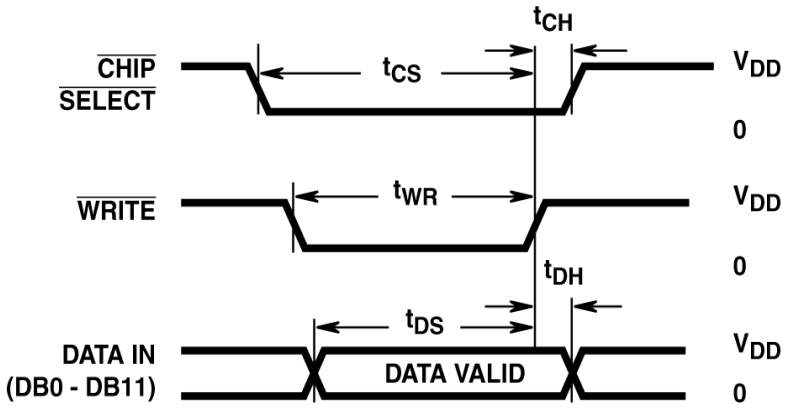
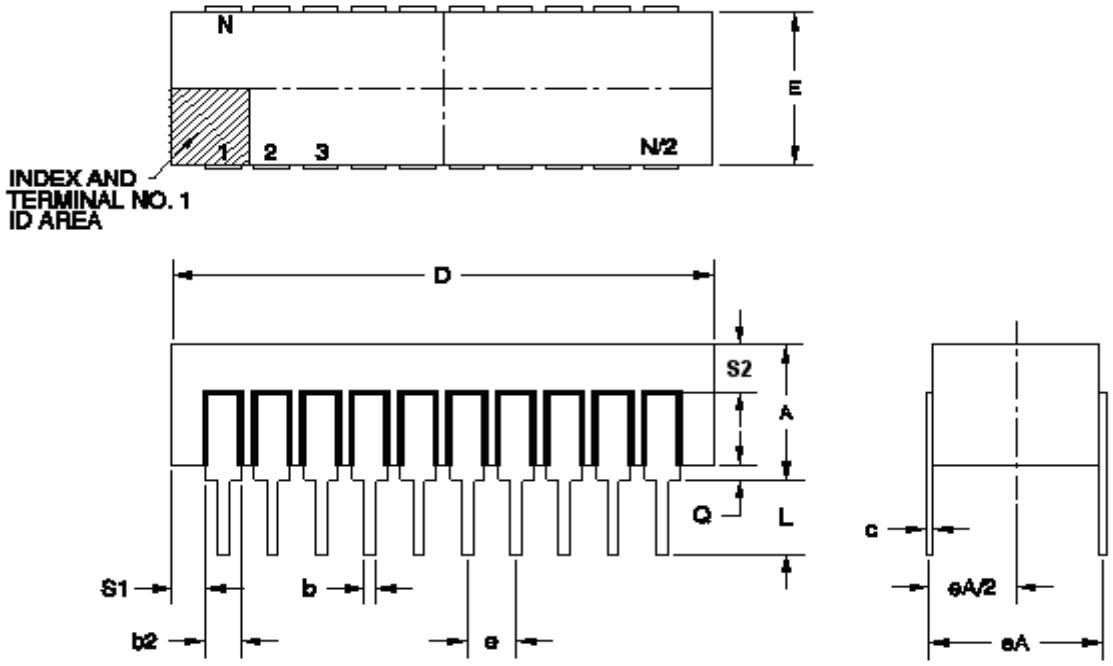


FIGURE 2. MODE SELECTION TABLE

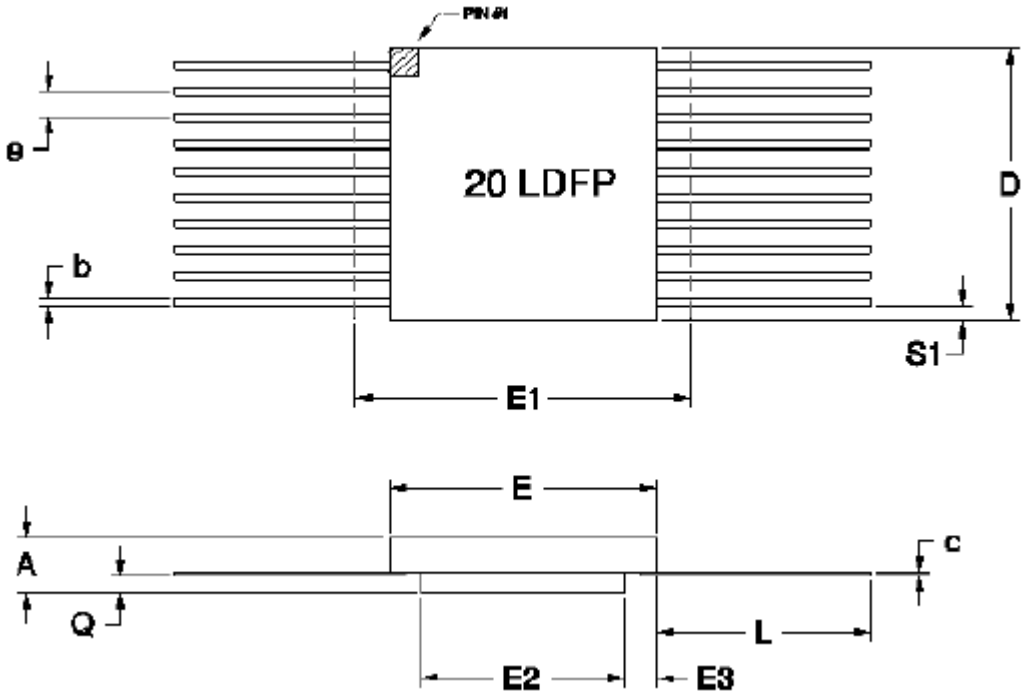
MODE SELECTION	
WRITE MODE: $\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0 - DB11) inputs	HOLD MODE: Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0 - DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.



20 PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.202	0.230
b	0.014	0.018	0.026
b2	0.045	0.050	0.065
c	0.008	0.010	0.018
D	--	1.000	1.060
E	0.220	0.290	0.310
eA	0.300 BSC		
eA/2	0.150 BSC		
e	0.100 BSC		
L	0.125	0.145	0.155
Q	0.015	0.045	0.070
S1	0.005	0.025	--
S2	0.005	--	--
N	20		

Note: All dimensions in inches



20 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.128	0.141	0.154
b	0.015	0.017	0.022
c	0.003	0.005	0.009
D	0.472	0.480	0.488
E	0.287	0.295	0.303
E1	--	--	0.333
E2	0.155	0.160	--
E3	0.030	0.068	--
e		0.050 BSC	
L	0.370	0.380	0.390
Q	0.026	0.034	0.045
S1	0.005	0.007	--
N		20	

Note: All dimensions in inches

Important Notice:

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