HN62434 Series

262,144-word × 16-bit / 524,288-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Rev. 2.0
September 12, 1995

The HN62434 is a 4-Mbit CMOS Programmable Mask ROM organized either as 262,144 words by 16 bits or as 524,288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

Features

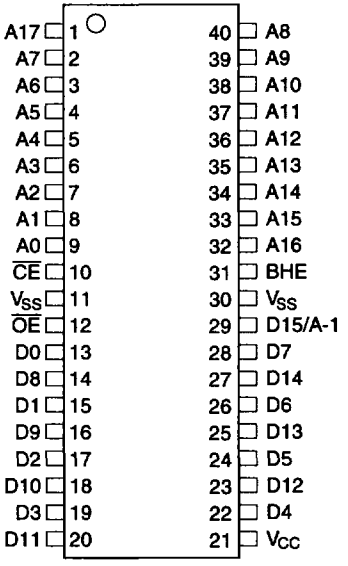
- Single +5 V power supply
- Access time: 120/150 ns (max)
- Low power consumption: 100 mW (typ) active
  5 µW (typ) standby
- Byte-wide or word-wide data organization with BHE
- Wired OR is permitted for the output in three status
- TTL compatible

Ordering Information

Type No.	Access time	Package
HN62434P-12 HN62434P-15	120 ns 150 ns	600 mil 40-pin plastic DIP (DP-40)
HN62434F-12 HN62434F-15	120 ns 150 ns	48-pin plastic SOP (FP-48DA)
HN62434FA-12 HN62434FA-15	120 ns 150 ns	40-pin plastic SOP (FP-40D)
HN62434TT-12 HN62434TT-15	120 ns 150 ns	44-pin plastic TSOP II (TTP-44D)

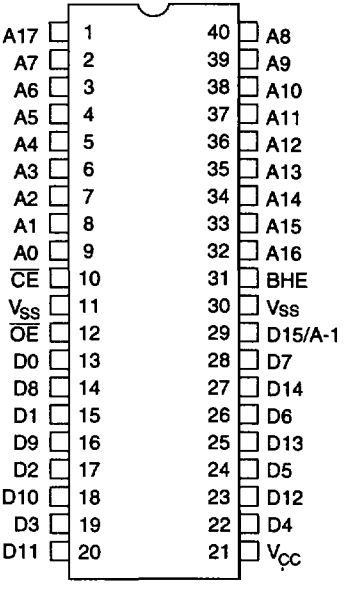
Pin Arrangement

HN62434P Series



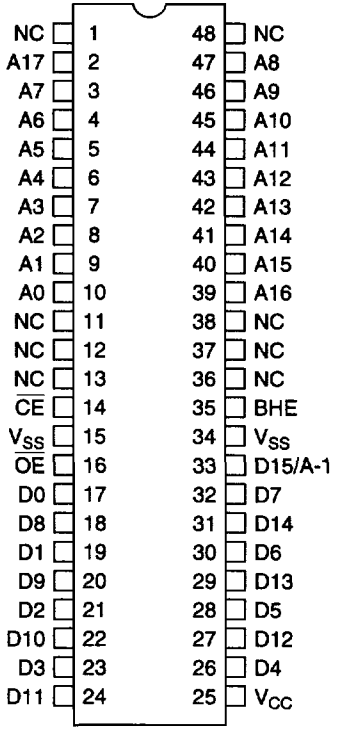
(Top View)

HN62434FA Series



(Top View)

HN62434F Series

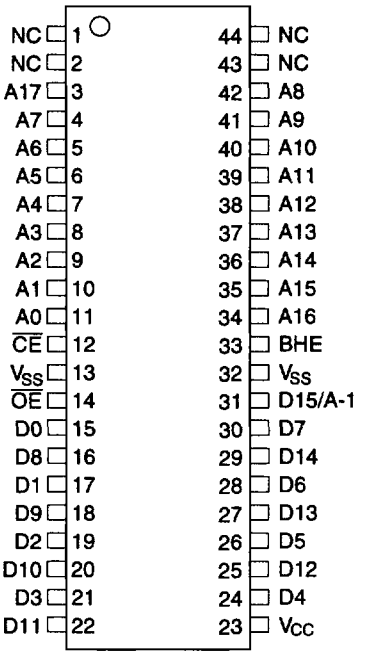


(Top View)

11-12-13 pin and 36-37-38 pin are connected to inner lead frame.

Pin Arrangement (cont.)

HN62434TT Series

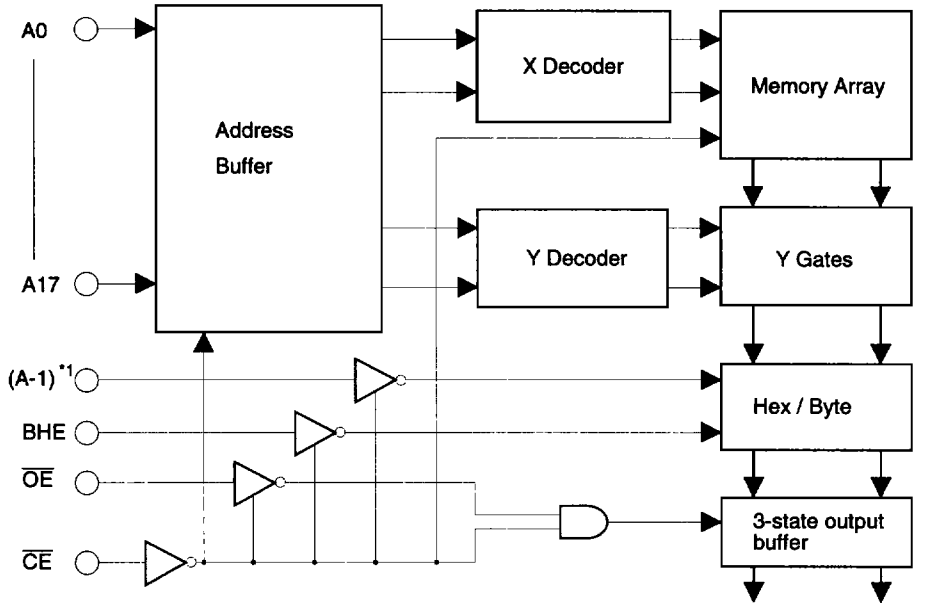


(Top View)

Pin Description

Pin name	Function
A0 to A17	Address input
D0 to D14	Data out
D15/A-1	Data out/address input
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word select
NC	No connection
V_{CC}	Power (+5 V)
V_{SS}	Ground

Block Diagram



BHE = V_{IH}: 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	−0.3 to +7.0	V	1
All input and output voltage	Vin, Vout	−0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	−55 to +125	°C	
Temperature under bias	Tbias	−20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
		I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{LI}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = −205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = +25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70 °C)

Test Condition

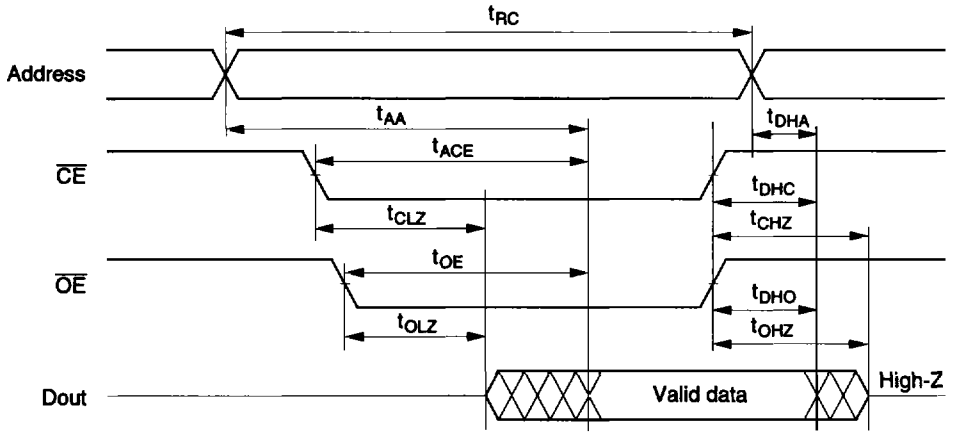
- Output load: 1 TTL gate + C_L = 100 pF (including jig)
- Input pulse level: 0.8 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns

		HN62434-12		HN62434-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns	
BHE access time	t_{BHE}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high Z	t_{CHZ}	—	60	—	70	ns	1
$\overline{OE}$ to output in high Z	t_{OHZ}	—	60	—	70	ns	1
BHE to output in high Z	t_{BHZ}	—	60	—	70	ns	1
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	10	—	ns	
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	10	—	ns	
BHE to output in low Z	t_{BLZ}	5	—	10	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

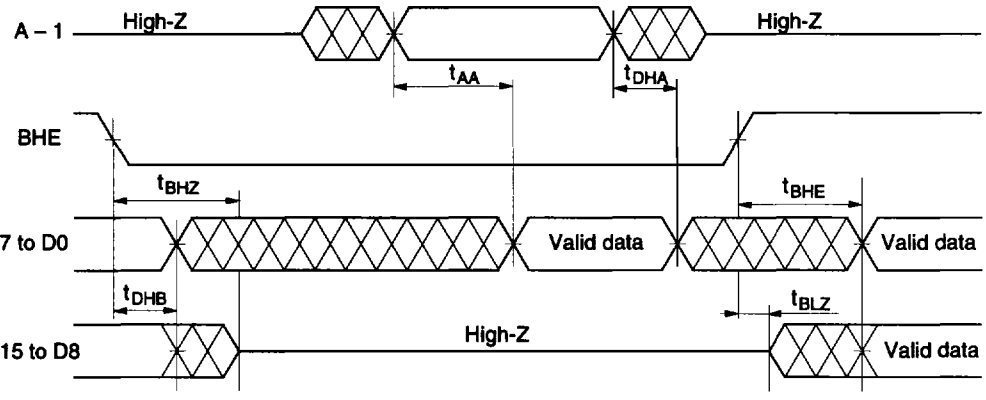
Timing Waveform

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Note: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

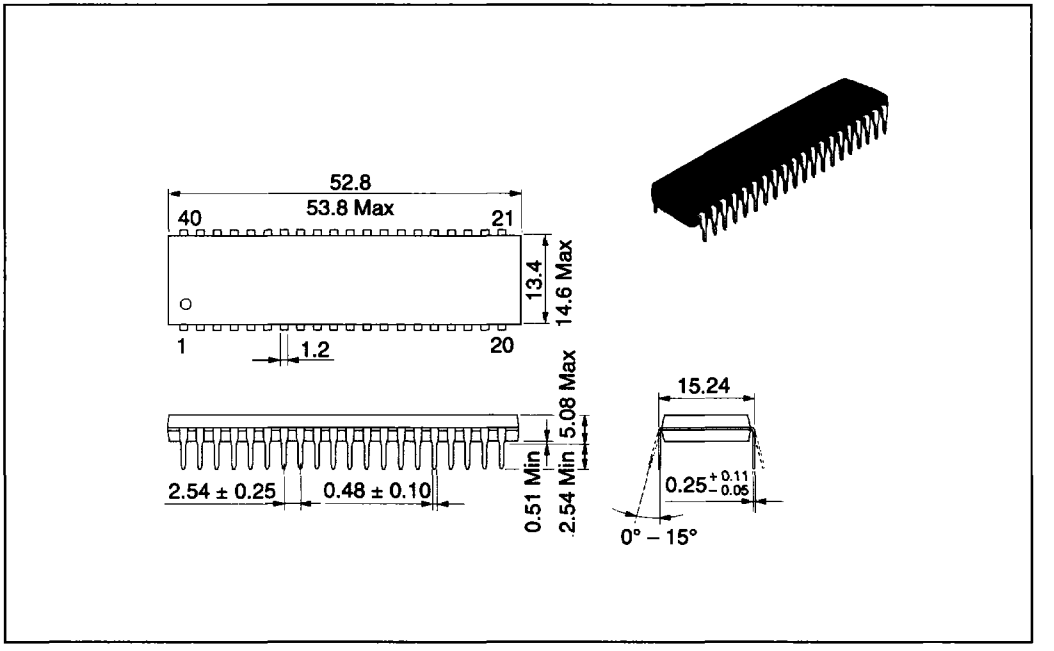
Word Mode, Byte Mode Switch



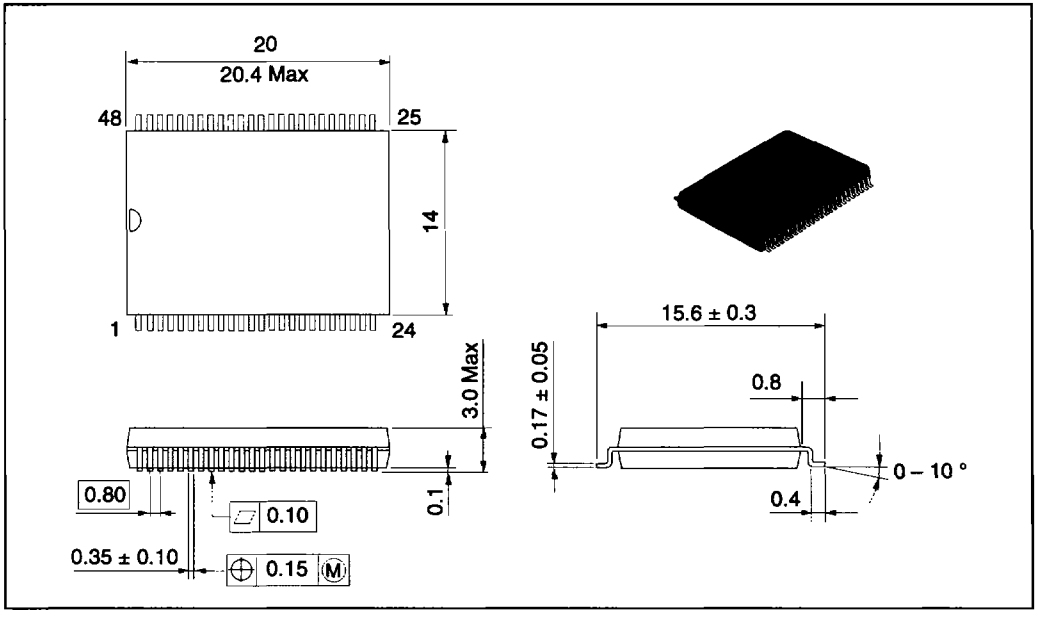
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A17 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Package Dimensions

HN62434P Series (DP-40) **Unit: mm**

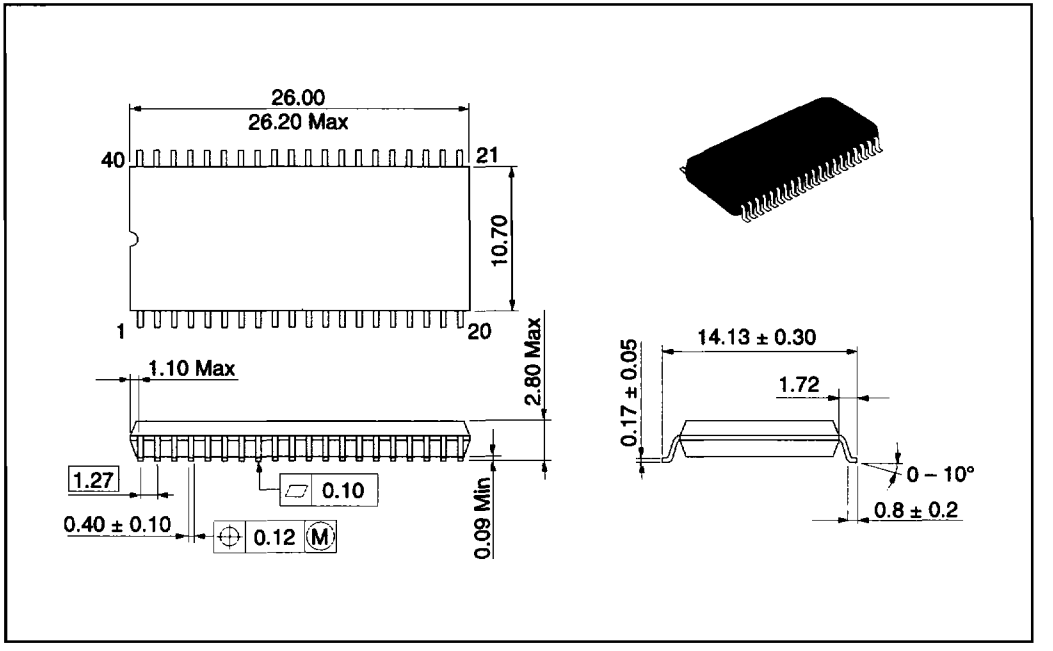


HN62434F Series (FP-48DA) **Unit: mm**



Package Dimensions (cont.)

HN62434FA Series (FP-40D) **Unit: mm**



HN62434TT Series (TTP-44D) **Unit: mm**