4M x 4-Bit Dynamic RAM
2k & 4k Refresh
(Hyper Page Mode - EDO)

HYB 5116405BJ/BT -50/-60/-70
HYB 5117405BJ/BT -50/-60/-70

Preliminary Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{\text{RAS}}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  89 ns (-50 version)
  104 ns (-60 version)
  124 ns (-70 version)
  CAS access time:
  12 ns (-50 version)
  15 ns (-60 version)
  20 ns (-70 version)
- Hyper page mode (EDO) cycle time
  20 ns (-50 version)
  25 ns (-60 version)
  30 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 550 mW active
  (HYB 5116405BJ/BT-50)
  max. 660 mW active
  (HYB 5117405BJ/BT-50)
  max. 605 mW active
  (HYB 5117405BJ/BT-60)
  max. 550 mW active
  (HYB 5117405BJ/BT-70)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, Self Refresh and test mode
- Hyper page mode (EDO) capability
- All inputs, outputs and clocks fully TTL-compatible
- 4096 refresh cycles / 64 ms for HYB5116405BJ/BT (4k-Refresh)
- 2048 refresh cycles / 32 ms for HYB5117405BJ/BT (2k-Refresh)
- Plastic Package: P-SOJ-26/24 300 mil
  P TSOPII-26/24 300 mil

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5116405BJ-50	Q67100-Q1098	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 5116405BJ-60	Q67100-Q1099	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 5116405BJ-70	Q67100-Q1100	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 5116405BT-50	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 50 ns)
HYB 5116405BT-60	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 60 ns)
HYB 5116405BT-70	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 70 ns)
HYB 5117405BJ-50	Q67100-Q1101	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 5117405BJ-60	Q67100-Q1102	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 5117405BJ-70	Q67100-Q1103	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 5117405BT-50	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 50 ns)
HYB 5117405BT-60	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 60 ns)
HYB 5117405BT-70	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 70 ns)

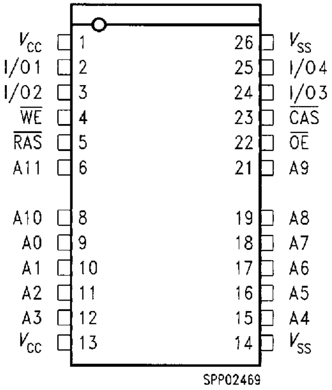
The HYB 5116(7)405BJ/BT is the new generation dynamic RAM organized as 4194304 words by 4-bits. The HYB 5116(7)405BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5116(7)405BJ/BT to be packaged in a standard SOJ 26/24 or TSOPII-26/24 plastic package, both with 300 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Pin Definitions and Functions

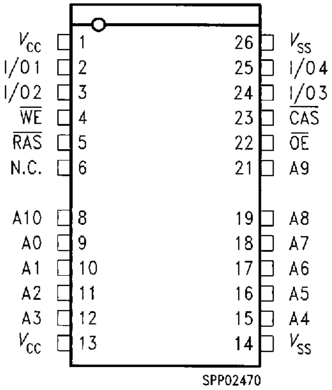
Pin No.	Function
A0-A11	Row Address Inputs for HYB5116405
A0-A9	Column Address Inputs for HYB5116405
A0-A10	Row and Column Address Inputs for HYB5117405
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{OE}}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

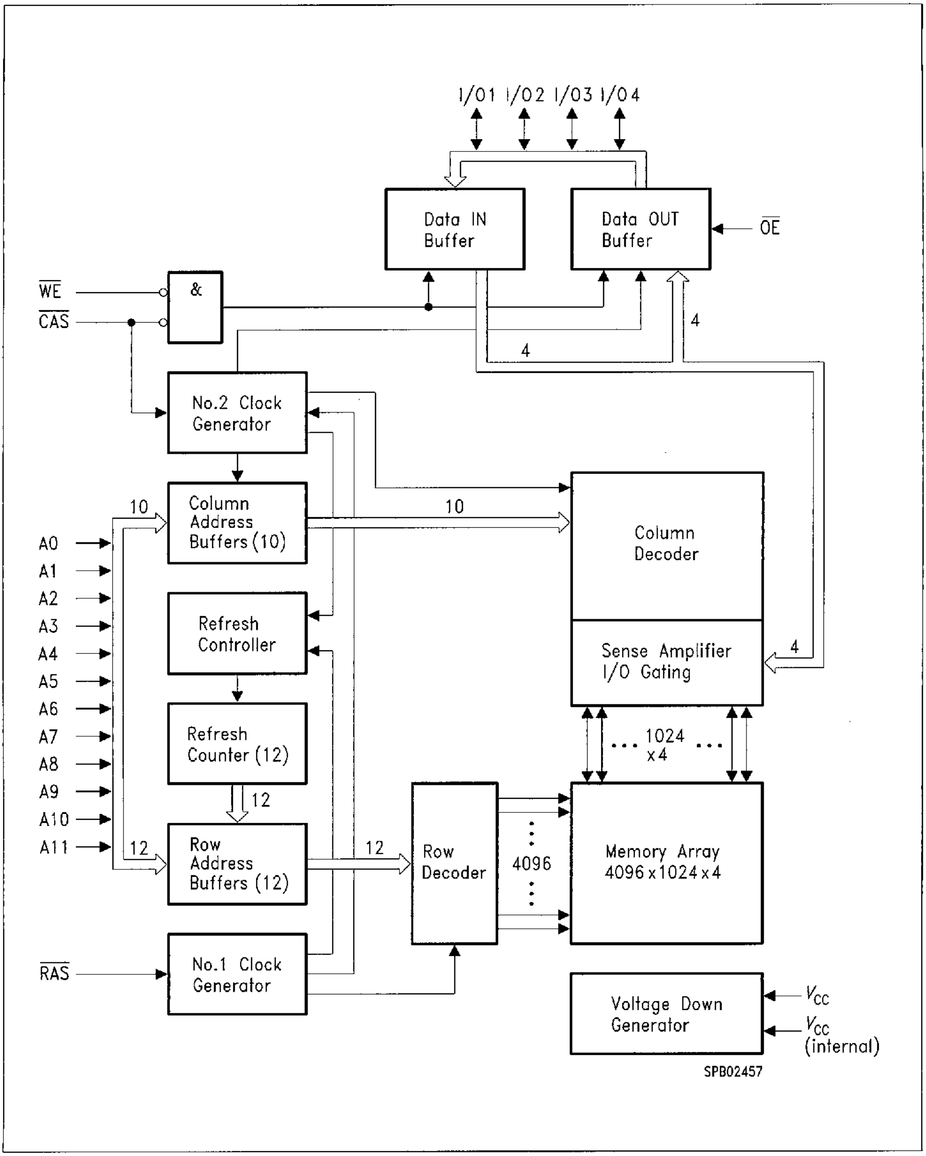
P-SOJ-26/24 300 mil
P-TSOPII-26/24 300 mil



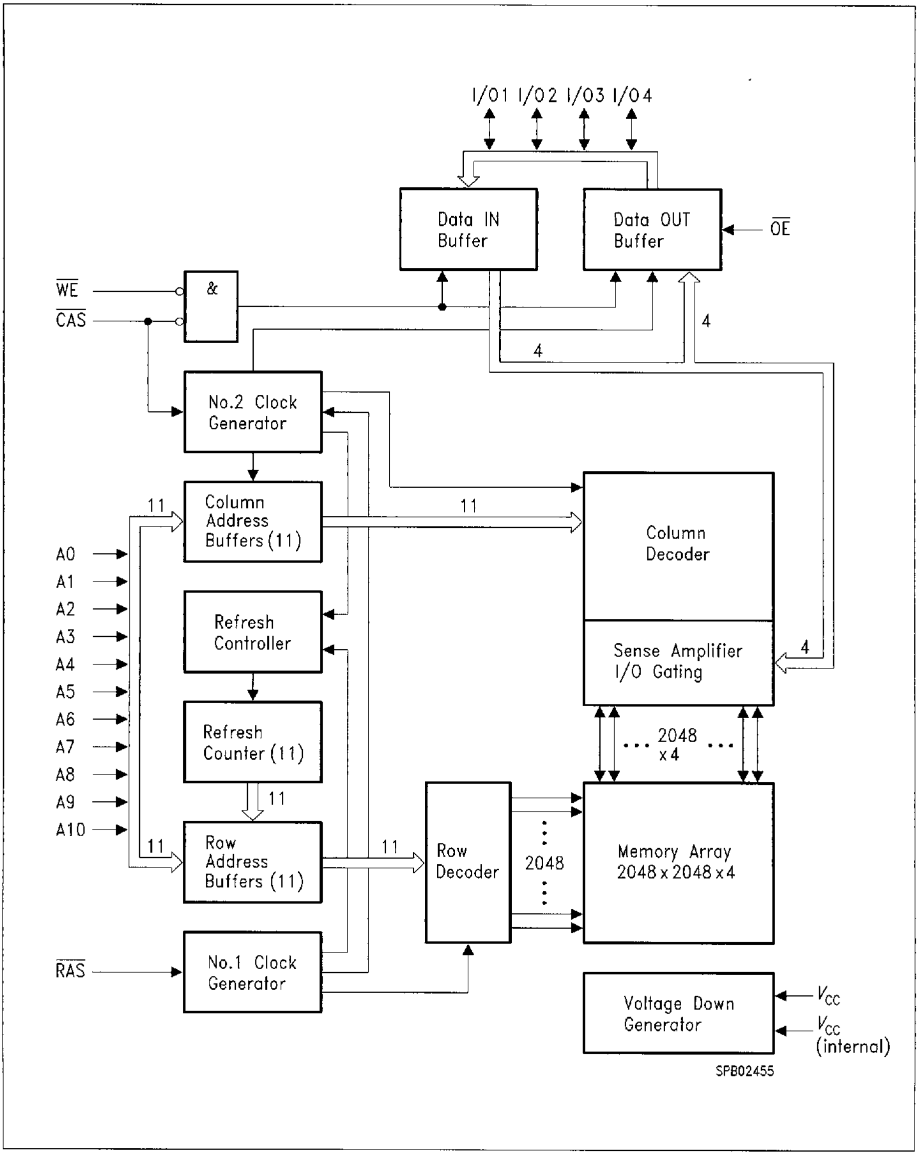
HYB 5116405 BJ/BT



HYB 5117405 BJ/BT



Block Diagram for HYB 5116405



Block Diagram for HYB 5117405 BJ/BT

Absolute Maximum Ratings

Operating temperature range .... 0 to 70 °C
Storage temperature range .... – 55 to 150 °C
Soldering temperature .... 260 °C
Soldering time .... 10 s
Input/output voltage .... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage .... – 1.0 V to 7.0 V
Power dissipation .... 1.0 W
Data out current (short circuit) .... 50 mA

Note:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (note : values in brackets for HYB 5117405 BJ/BT)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	100(120)	mA	2) 3) 4)
-60 ns version		–	90 (110)	mA	2) 3) 4)
-70 ns version		–	80 (100)	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	100(120)	mA	2) 4)
-60 ns version		–	90 (110)	mA	2) 4)
-70 ns version		–	80 (100)	mA	2) 4)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (note : values in brackets for HYB 5117405 BJ/BT) (cont'd)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during hyper page mode:	I_{CC4}				
-50 ns version		–	85 (90)	mA	2) 3) 4)
-60 ns version		–	75 (80)	mA	2) 3) 4)
-70 ns version		–	65 (70)	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode:	I_{CC6}				
-50 ns version		–	100(120)	mA	2) 4)
-60 ns version		–	90 (110)	mA	2) 4)
-70 ns version		–	80 (100)	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)					
Average Self Refresh Current (CBR cycle with t_{RAS}>t_{RASS}min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} - 0.2 V or 0.2V)	I_{CC7}	–	1	mA	

AC Characteristics 5)7)

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/ BT-50		HYB 5116(7)405BJ/ BT-60		HYB 5116(7)405BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	89	–	104	–	124	–	ns
Read-write cycle time	t_{RWC}	117	–	138	–	162	–	ns
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	57	–	68	–	77	–	ns
Access time from $\overline{\text{RAS}}$ 7) 12)	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{\text{CAS}}$ 7) 12)	t_{CAC}	–	12	–	15	–	17	ns
Access time from column address 7) 13)	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{\text{CAS}}$ precharge 7)	t_{CPA}	–	27	–	32	–	37	ns
$\overline{\text{CAS}}$ to output in low-Z 7)	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay 8) 18)	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) 6)	t_T	1	50	1	50	1	50	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{\text{RAS}}$ pulse width (Hyper page mode- EDO)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{\text{CAS}}$ pulse width	t_{CAS}	7	10k	10	10k	12	10k	ns
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay (Hyper Page Mode)	t_{RHCP}	27	–	32	–	37	–	ns
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ (HPM RMW)	t_{CPWD}	41	–	49	–	56	–	ns
$\overline{\text{RAS}}$ hold time	t_{RSH}	12		15	–	17	–	ns
$\overline{\text{CAS}}$ hold time	t_{CSH}	50		60	–	70	–	ns

AC Characteristics (cont'd) [5][7]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/ BT-50		HYB 5116(7)405BJ/ BT-60		HYB 5116(7)405BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time [12]	t_{RCD}	12	38	14	45	14	53	
$\overline{\text{RAS}}$ to column address delay time [13]	t_{RAD}	10	25	12	30	12	35	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{\text{CAS}}$ precharge time	t_{CP}	9	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	5	–	7	–	10	–	ns
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{\text{RAS}}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	5	–	7	–	10	–	ns
Write command pulse width	t_{WP}	5	–	7	–	10	–	ns
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	12	–	15	–	17	–	ns
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	12	–	15	–	17	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	5	–	7	–	10	–	ns
Refresh period for HYB5116405	t_{REF}	–	64	–	64	–	64	ms
Refresh period for HYB5117405	t_{REF}	–	32	–	32	–	32	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5][7]
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/ BT-50		HYB 5116(7)405BJ/ BT-60		HYB 5116(7)405BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time [11]	t_{CWD}	26	–	32	–	36	–	ns
$\overline{\text{RAS}}$ to WE delay time [11]	t_{RWD}	64	–	77	–	89	–	ns
Column address to $\overline{\text{WE}}$ delay time [11]	t_{AWD}	39	–	47	–	54	–	ns
$\overline{\text{CAS}}$ setup time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{\text{CAS}}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{\text{CAS}}$ precharge time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
Output data hold time	t_{COH}	5	–	5	–	5	–	ns
$\overline{\text{OE}}$ command hold time	t_{OEH}	12	–	15	–	17	–	ns
$\overline{\text{OE}}$ access time	t_{OEA}	–	12	–	15	–	17	ns
Output buffer turn-off delay from $\overline{\text{OE}}$	t_{OEZ}	0	12	0	15	0	17	ns
Data to $\overline{\text{CAS}}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{\text{OE}}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5)7)]
T_A = 0 to 70 ˚C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/ BT-50		HYB 5116(7)405BJ/ BT-60		HYB 5116(7)405BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{\text{CAS}}$ high to data delay [16)]	t_{CDD}	12	–	15	–	17	–	ns
$\overline{\text{OE}}$ high to data delay [16)]	t_{ODD}	12	–	15	–	17	–	ns
$\overline{\text{RAS}}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns
$\overline{\text{RAS}}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{\text{CAS}}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance
T_A = 0 to 70 ˚C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10,A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O4)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$. In the case of I_{CC4} it can be changed once or less during a hyper page mode cycle (t_{HPC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL gates and 50 pF ($V_{ol} = 0.8$ V and $V_{oh} = 2.0$ V).

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10)These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{\text{WE}}$ leading edge in read-write cycles.

11)t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12)Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13)Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14)AC measurements assume $t_T = 2$ ns.

15)Either t_{DZC} or t_{DZO} must be satisfied.

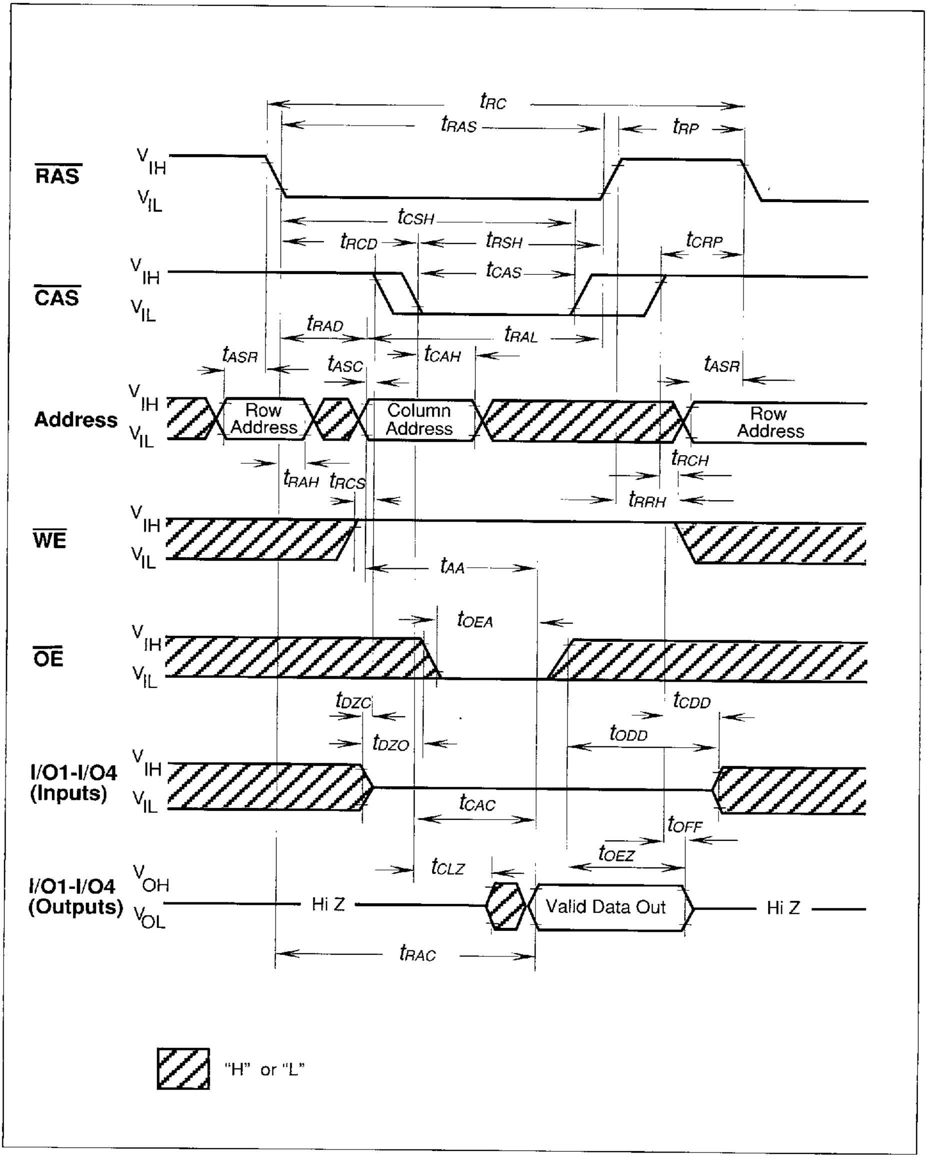
16)Either t_{CDD} or t_{ODD} must be satisfied.

17)When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

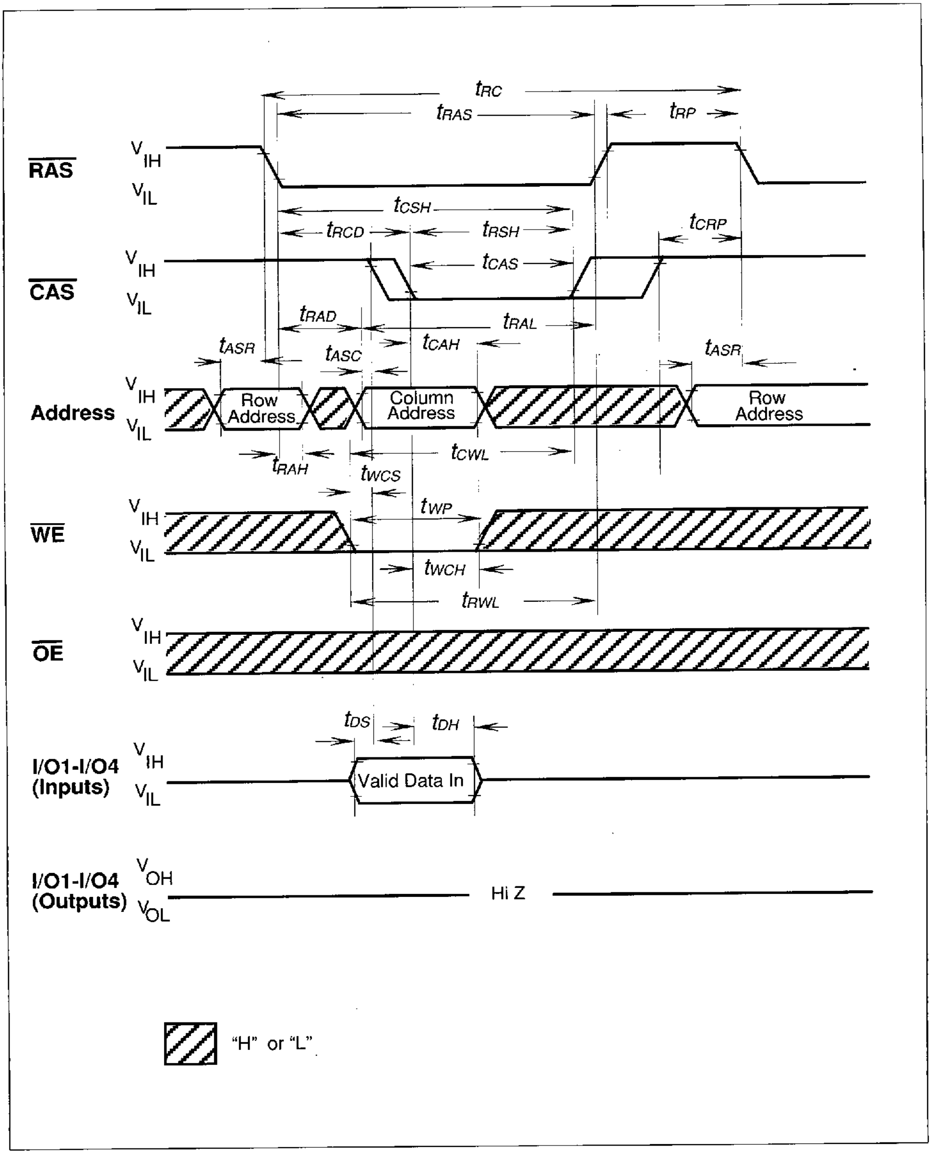
If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

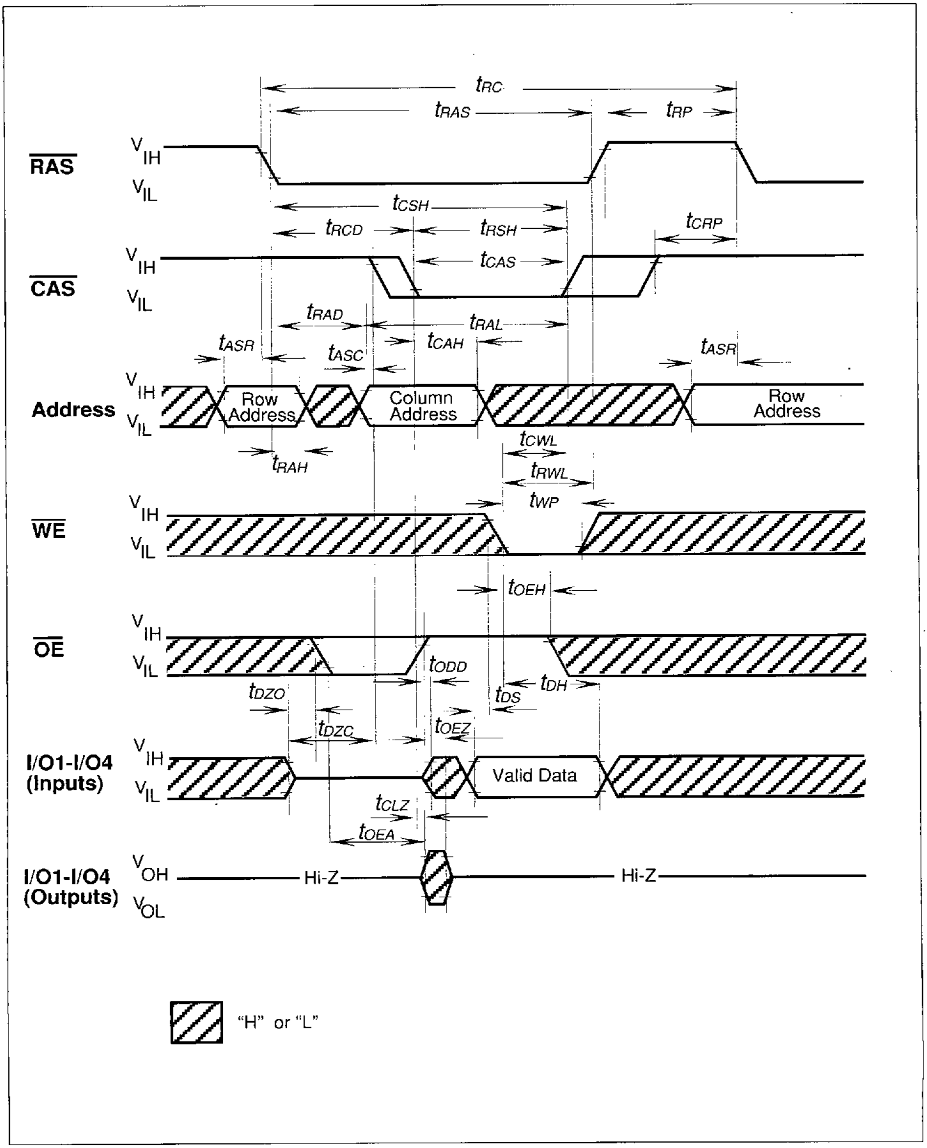
18)t_{off} is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
CAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O4 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O4 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

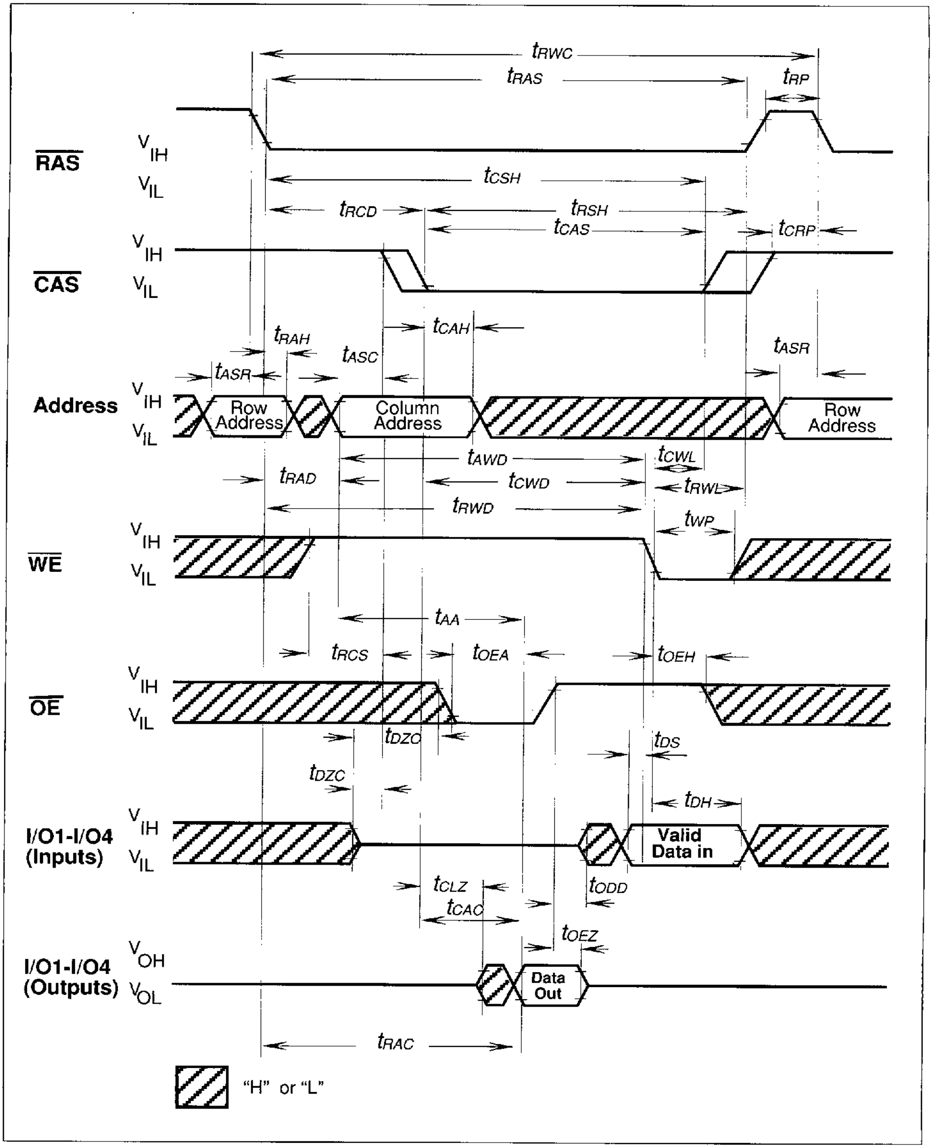
Read Cycle



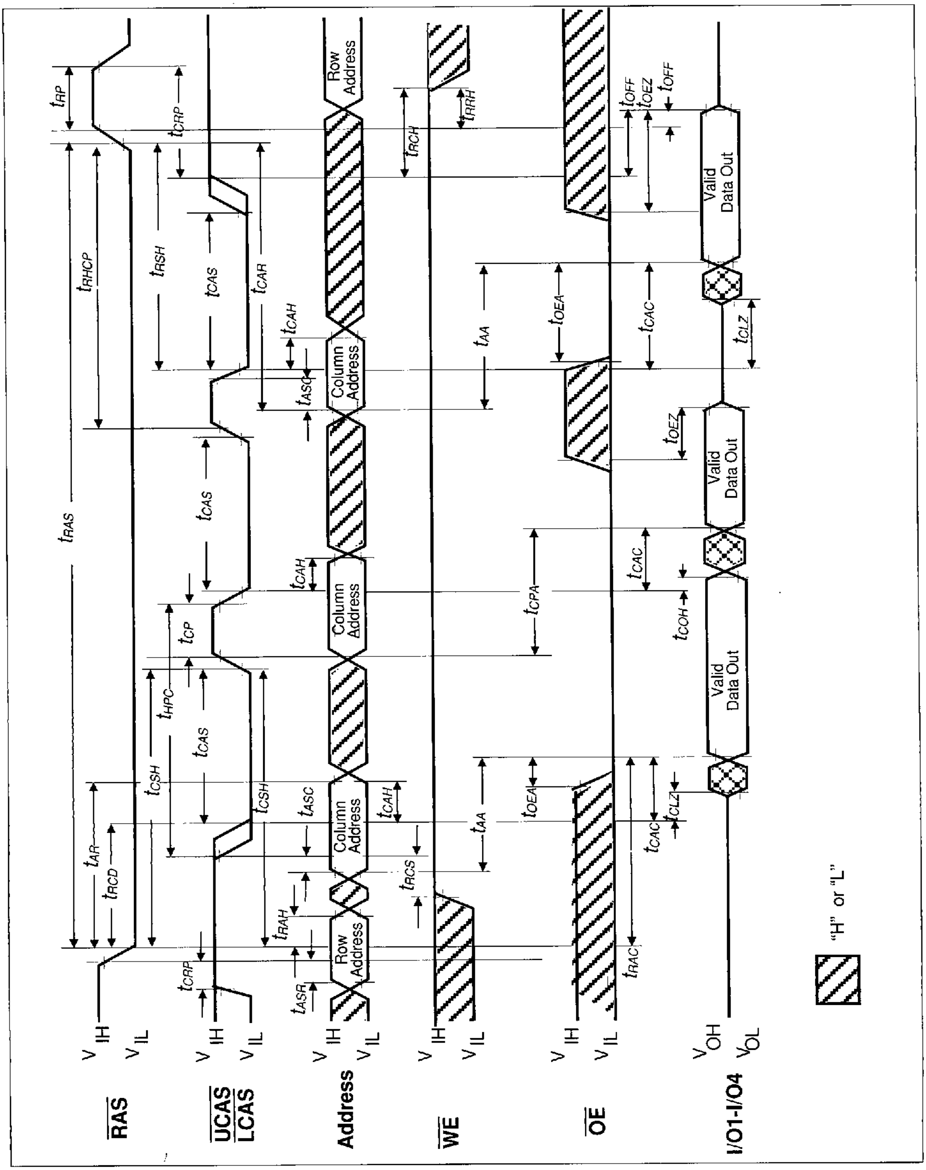
Write Cycle (Early Write)



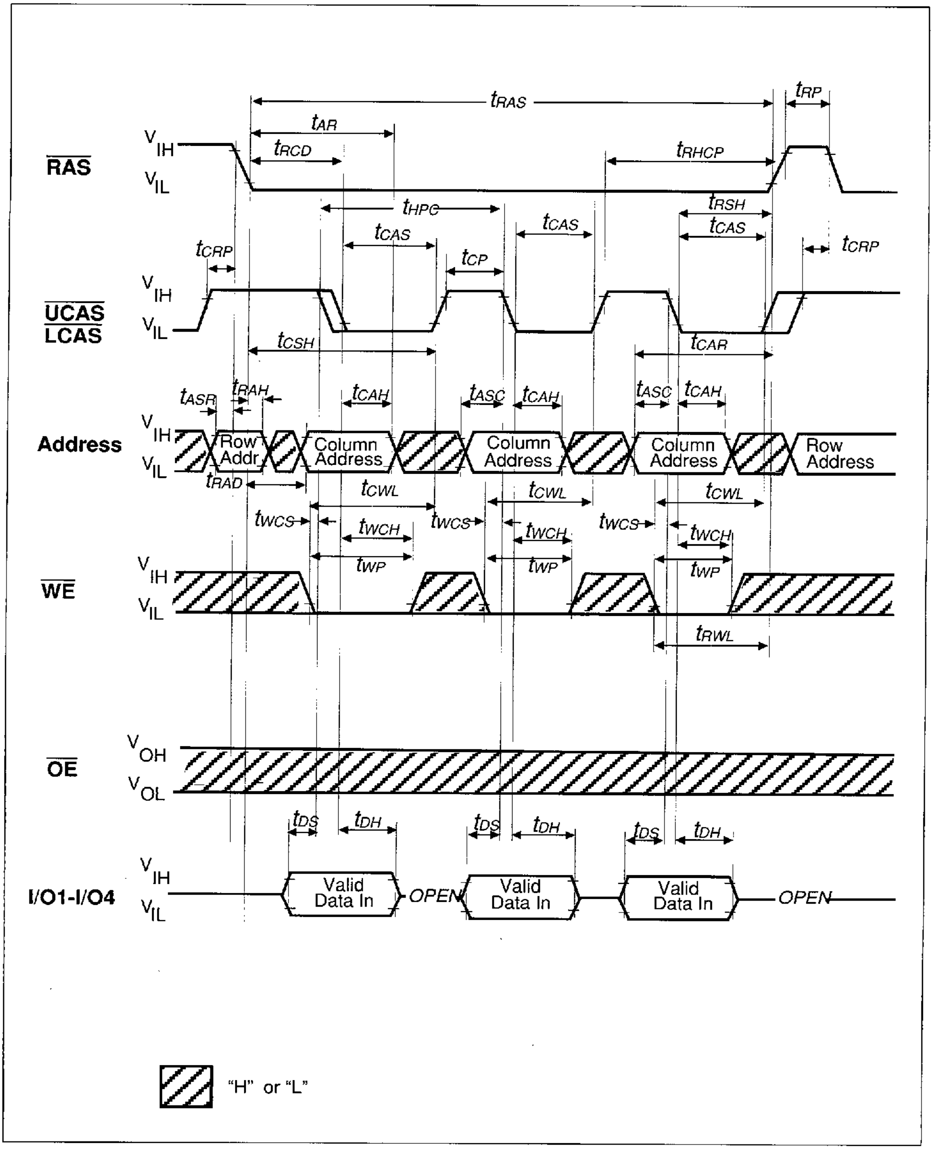
Write Cycle ($\overline{\text{OE}}$ Controlled Write)



Read-Write (Read-Modify-Write) Cycle

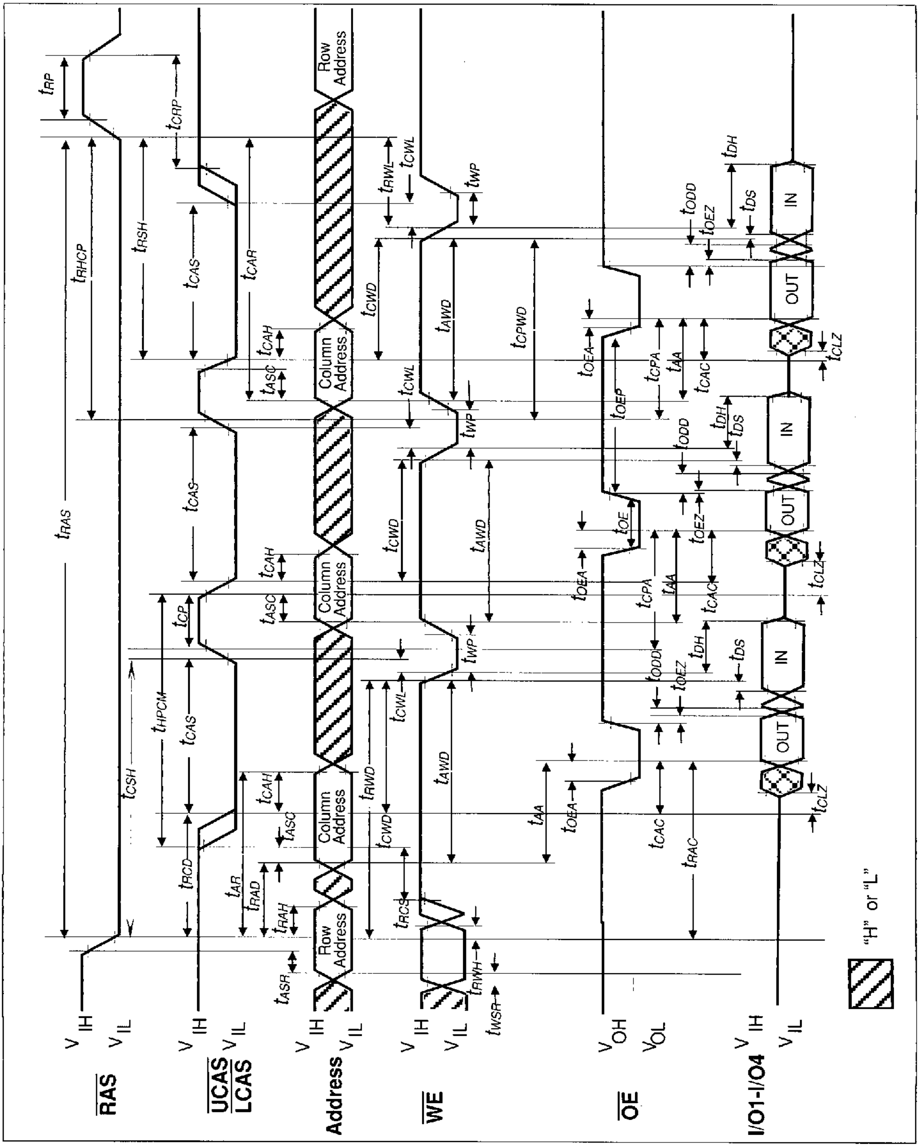


Hyper Page Mode (EDO) Read Cycle

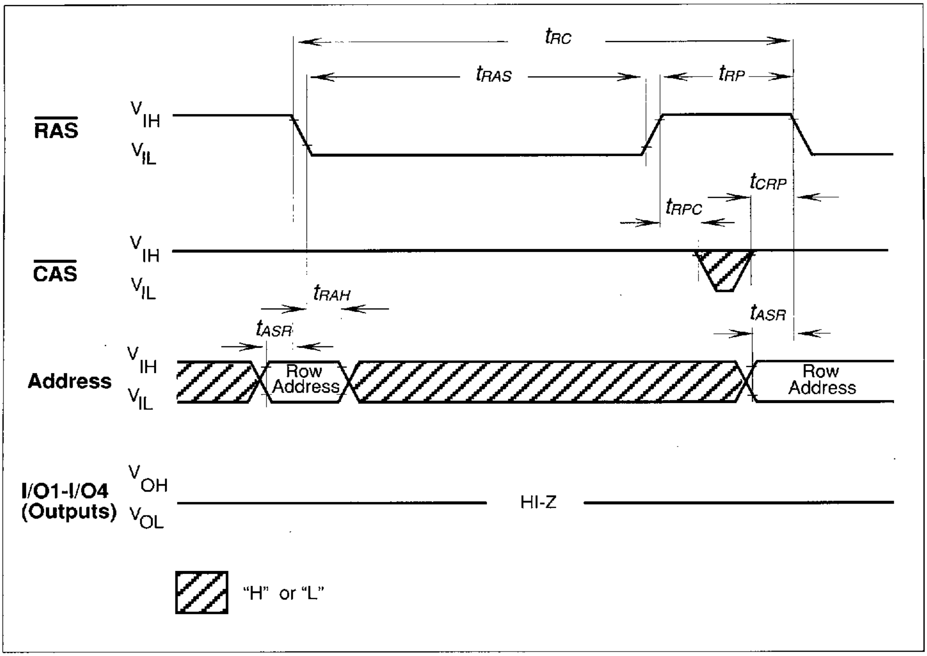


▨ "H" or "L"

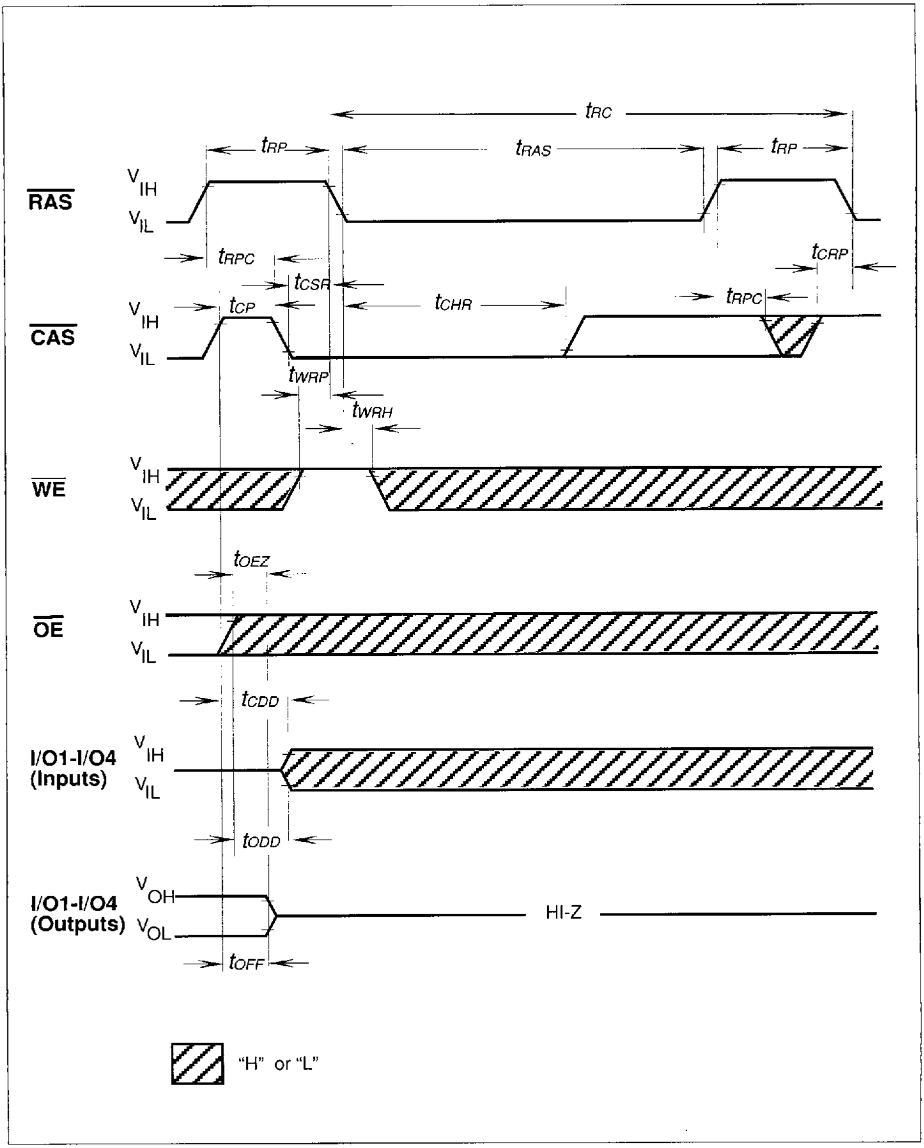
Hyper Page Mode (EDO) Write Cycle



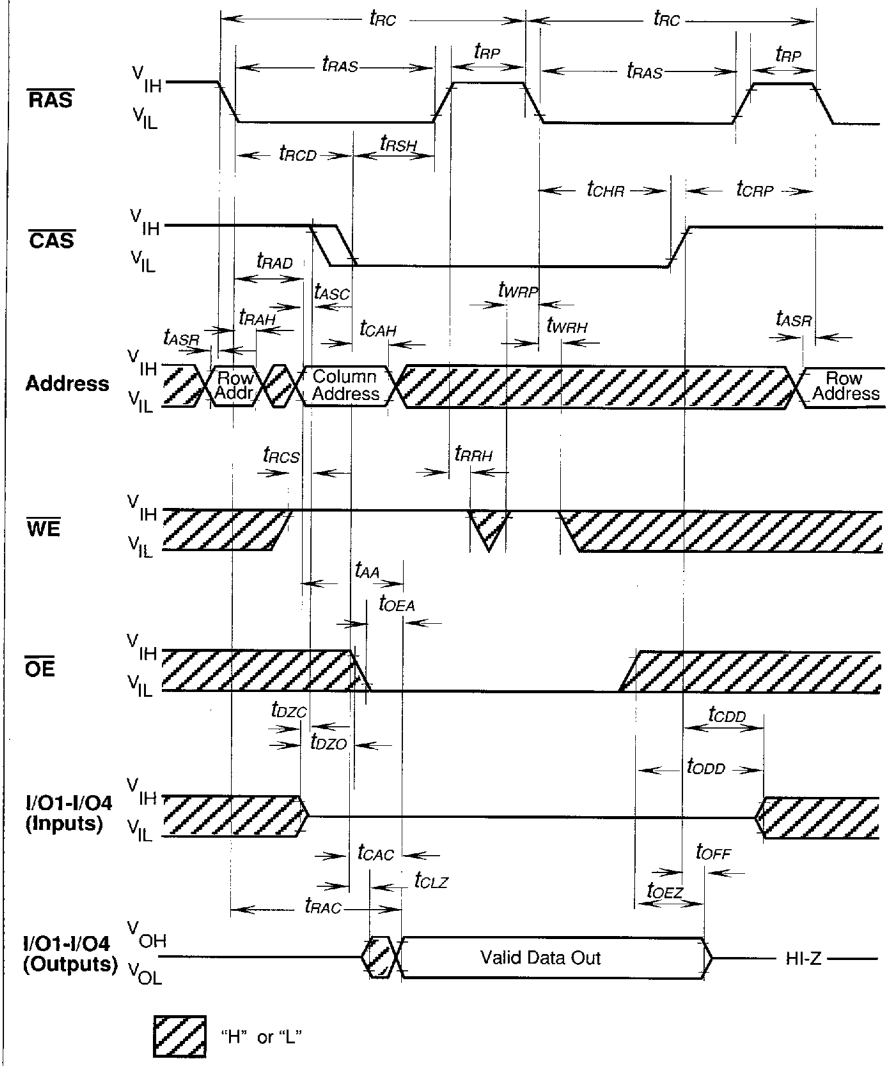
Hyper Page Mode (EDO) Late Write and Read-Modify Write Cycle



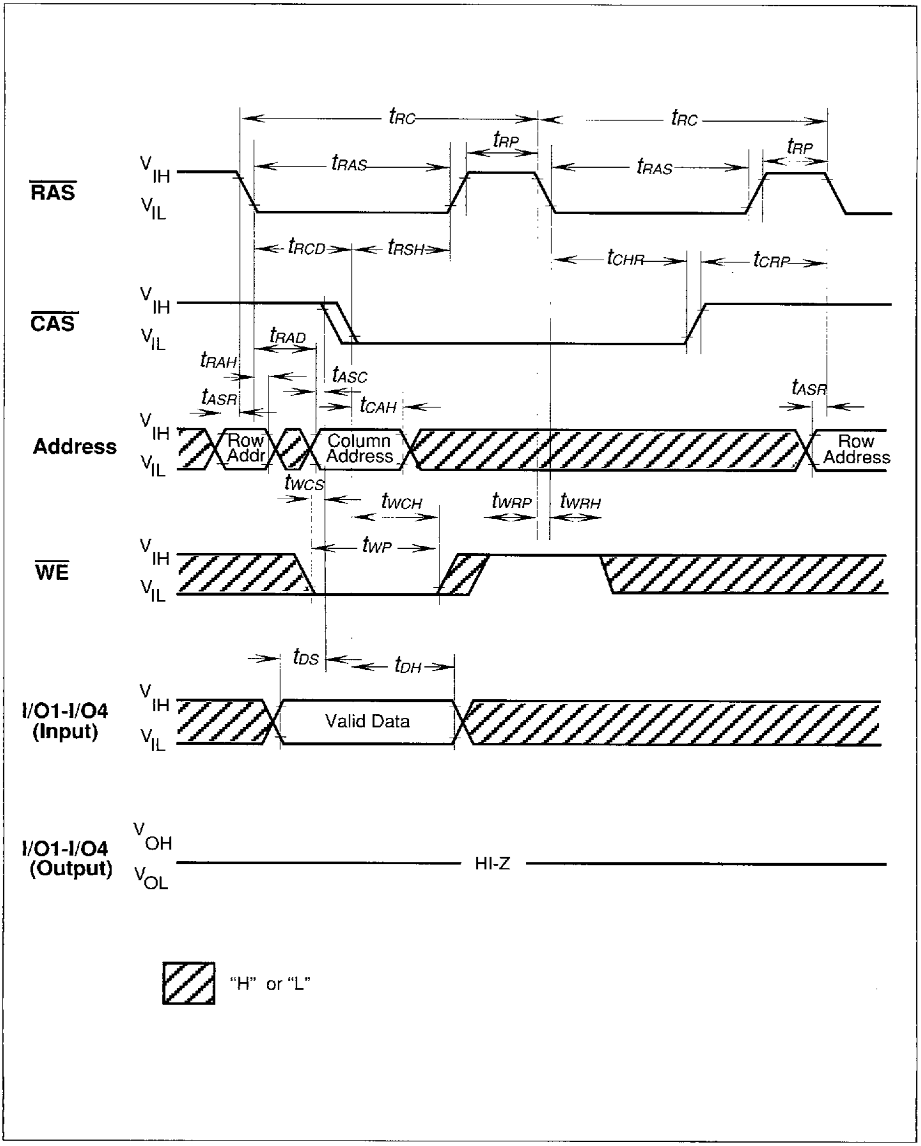
$\overline{RAS}$-Only Refresh Cycle



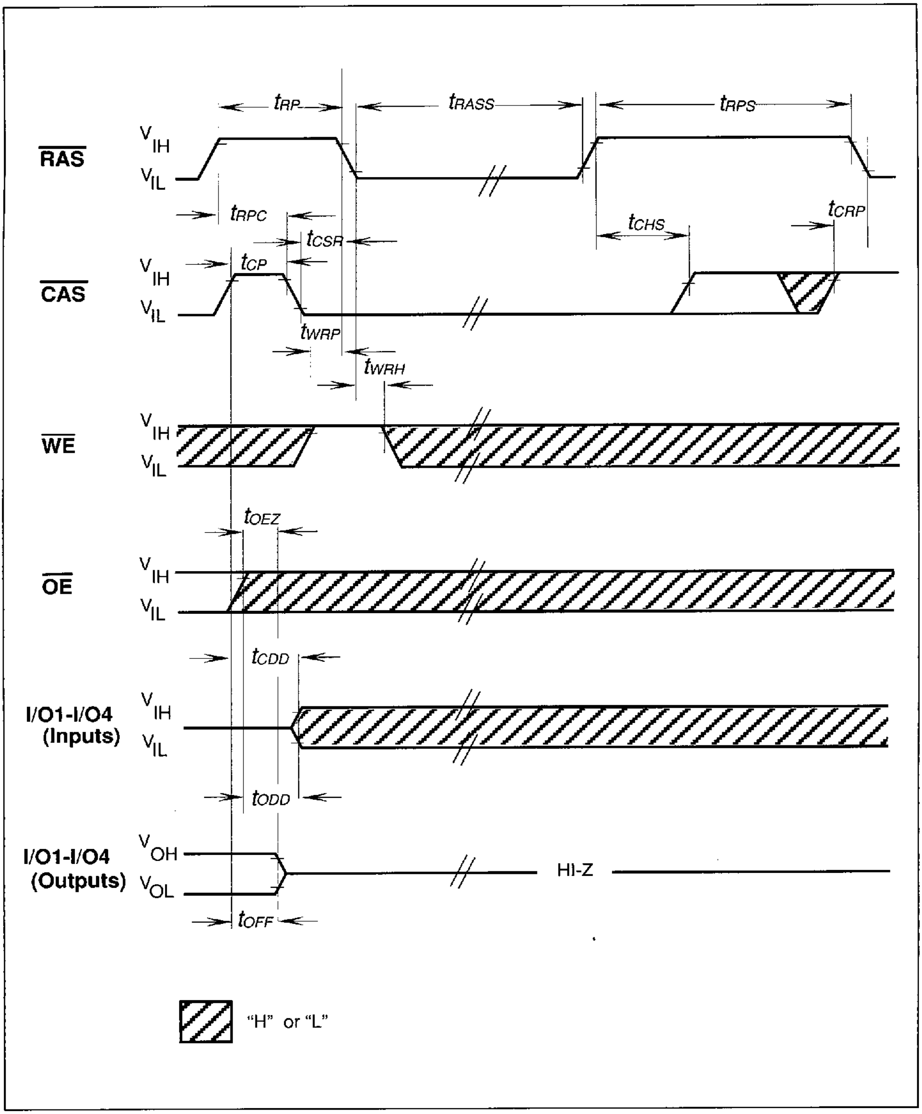
CAS-Before-RAS Refresh Cycle



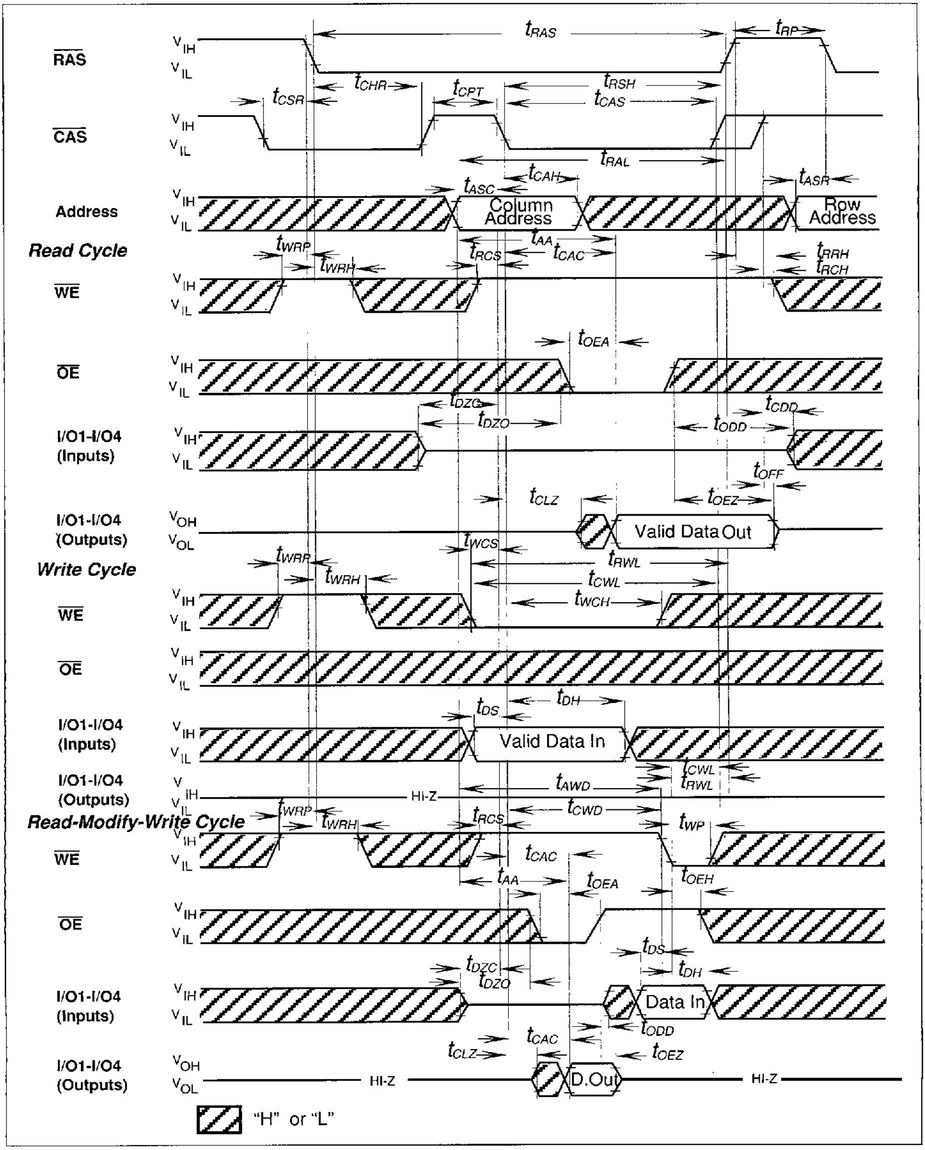
Hidden Refresh Cycle (Read)



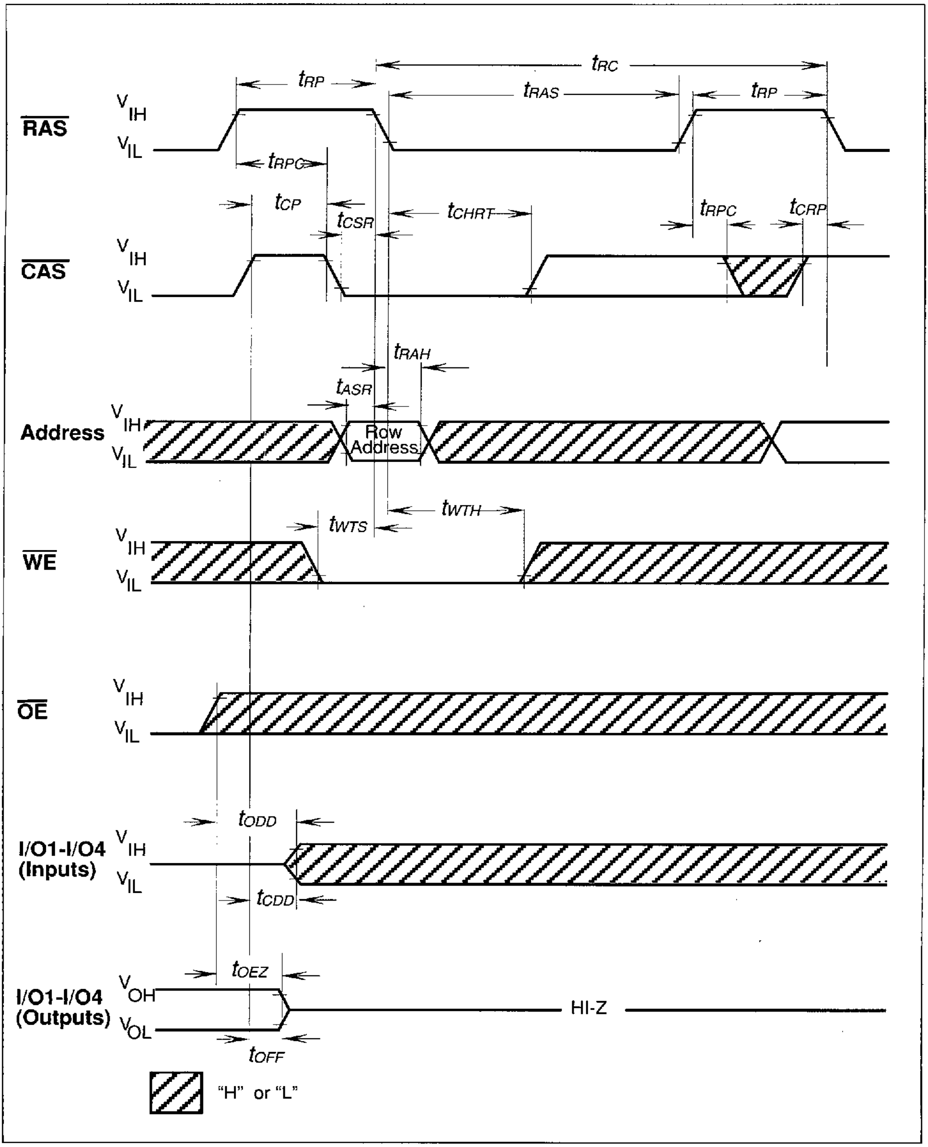
Hidden Refresh Cycle (Early Write)



CAS-before-RAS Self Refresh



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle



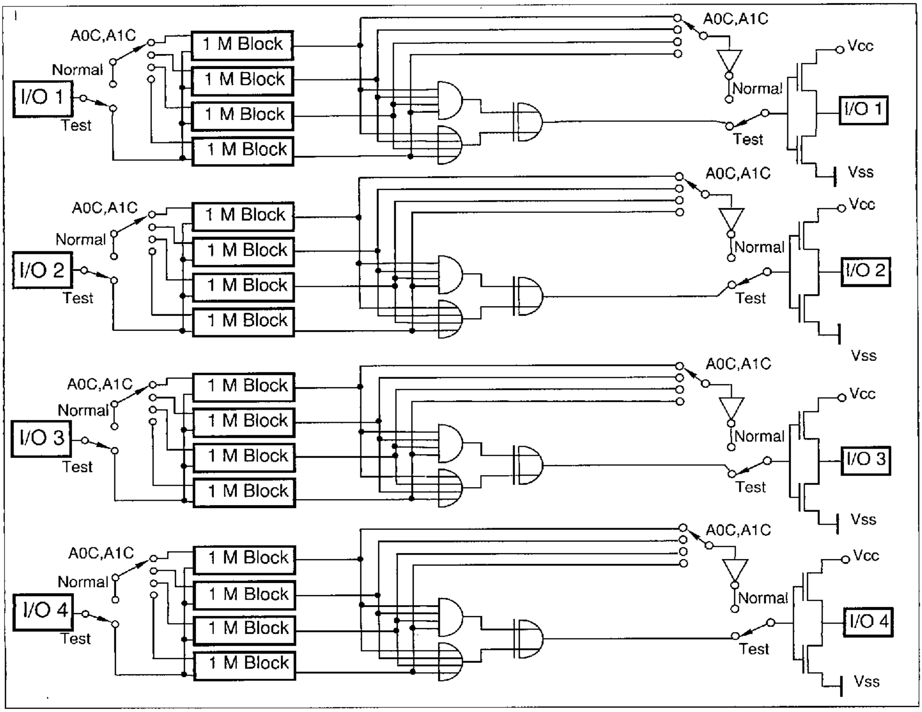
Test Mode Entry

Test Mode

As the HYB 5116(7)405BJ/BT is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used.Refresh during test mode operation can be performed by normal read cylces or by WCBR refresh cycles.

Row addresses A0 through A9 have to kept high to perform a testmode entry cylce. All other addresses are don't care.



Block Diagram in Test Mode