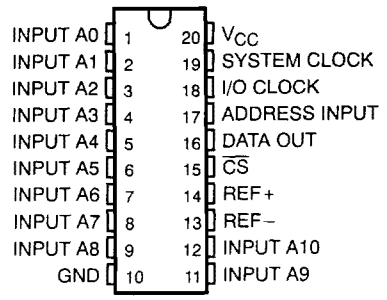
TLC1540C, TLC1540I, TLC1540M, TLC1541C, TLC1541I, TLC1541M
LinCMOS™ 10-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

D2859, DECEMBER 1985–REVISED AUGUST 1991

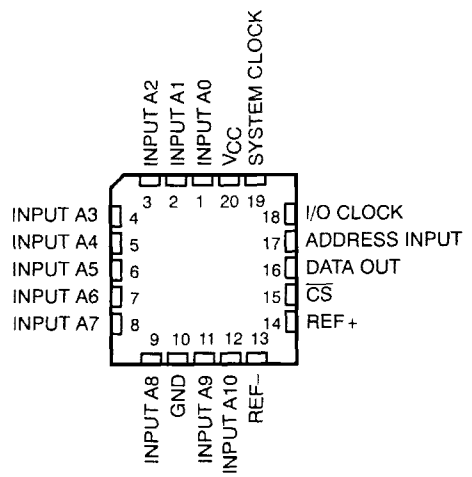
- LinCMOS™ Technology
- 10-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error
  - TLC1540: ±0.5 LSB Max
  - TLC1541: ±1 LSB Max
- Pinout and Control Signals Compatible With TLC540 and TLC549 Families of 8-Bit A/D Converters

TYPICAL PERFORMANCE	
Channel Acquisition Sample Time	5.5 µs
Conversion Time	21 µs
Samples Per Second	32 × 10^3
Power Dissipation	6 mW

DW, J, OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



description

The TLC1540 and TLC1541 are LinCMOS™ A/D peripherals built around a 10-bit, switched-capacitor, successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs [including independent system clock, I/O clock, chip select ($\overline{CS}$), and address input]. A 2.1-MHz system clock for the TLC1540 and TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates of up to 32,258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip, 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage and a sample and hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC1540 and TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error conversion (±0.5 LSB for the TLC1540, ±1 LSB for the TLC1541) in 21 µs over the full operating temperature range.

The TLC1540 and the TLC1541 are available in DW, FK, FN, J, and N packages. The C-suffix versions are characterized for operation from 0°C to 70°C. The I-suffix versions are characterized for operation from −40°C to 85°C. The M-suffix versions are characterized for operation from −55°C to 125°C.

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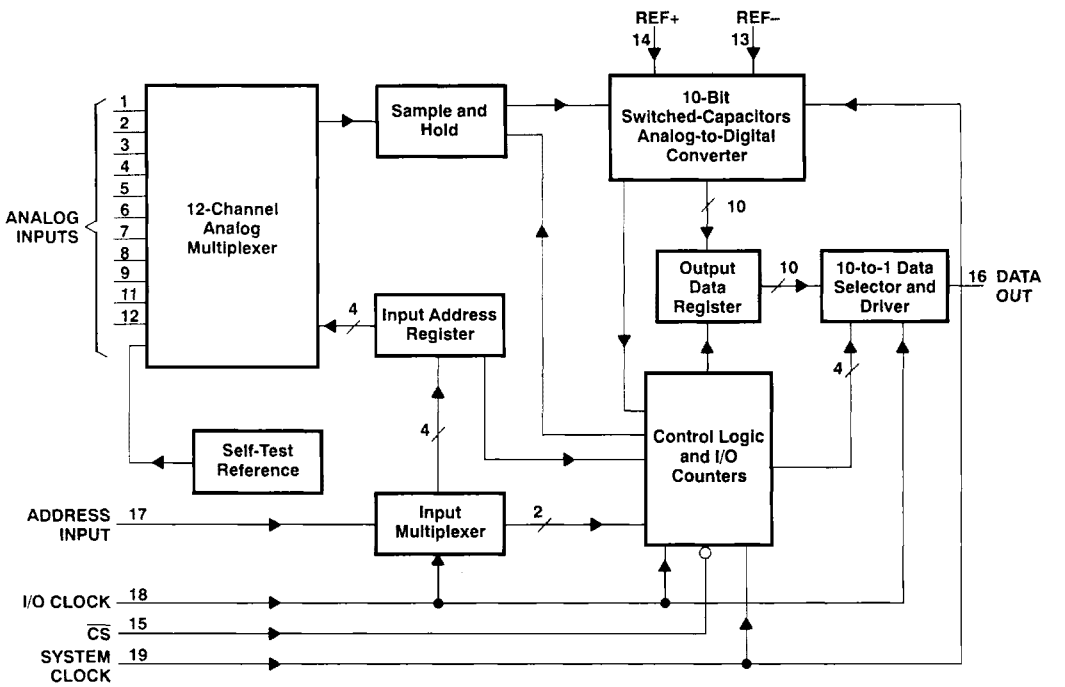
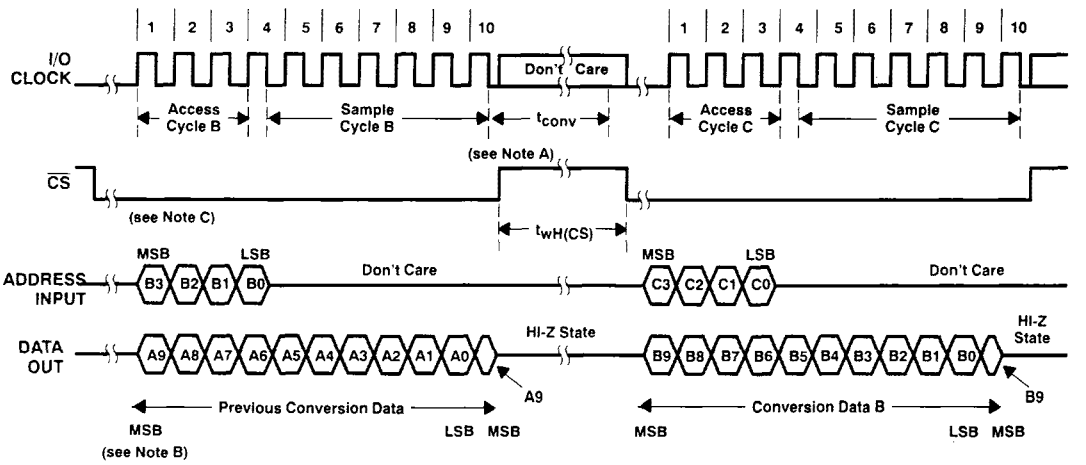
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 44 system clock periods, is initiated on the 10th falling edge of the I/O clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O clock must remain low for at least 44 system clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8–A0) will be clocked out on the first nine I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	−0.3 V to V_{CC} + 0.3 V
Output voltage range	−0.3 V to V_{CC} + 0.3 V
Peak input current (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range: TLC1540C, TLC1541C	0°C to 70°C
TLC1540I, TLC1541I	−40°C to 85°C
TLC1540M, TLC1541M	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}			2			V
Low-level control input voltage, V_{IL}					0.8	V
Input/Output clock frequency, $f_{CLK(I/O)}$			0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		2.1	MHz
Setup time, address bits before I/O CLK↑, $t_{su(A)}$			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			44			System clock cycles
System clock high, $t_{wH(SYS)}$			210			ns
System clock low, $t_{wL(SYS)}$			190			ns
Input/Output clock high, $t_{wH(I/O)}$			404			ns
Input/Output clock low, $t_{wL(I/O)}$			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A		TLC1540C, TLC1541C	0		70	°C
		TLC1540I, TLC1541I	−40		85	
		TLC1540M, TLC1541M	−55		125	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (1111111111), while input voltages less than that applied to REF− convert as all "0"s (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V,	I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

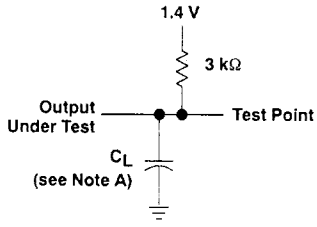
operating characteristics over recommended operating temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 1.1$ MHz, $f_{CLK(SYS)} = 2.1$ MHz

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
	Linearity error	TLC1540	See Note 5		±0.5	LSB
		TLC1541			±1	
	Zero error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Full-scale error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Total unadjusted error	TLC1540	See Note 7		±0.5	LSB
		TLC1541			±1	
	Self-test output code		Input A11 address = 1011 (See Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time		See Operating Sequence		21	µs
	Total access and conversion time		See Operating Sequence		31	µs
t_{acq}	Channel acquisition time (sample cycle)		See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓			10		ns
t_d	Delay time, I/O clock↓ to data output valid		See Parameter Measurement Information		400	ns
t_{en}	Output enable time				150	ns
t_{dis}	Output disable time				150	ns
$t_{r(bus)}$	Data bus rise time				300	ns
$t_{f(bus)}$	Data bus fall time				300	ns

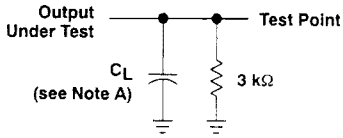
NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (1111111111), while input voltages less than that applied to REF− convert as all "0"s (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
7. Total unadjusted error comprises linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

PARAMETER MEASUREMENT INFORMATION

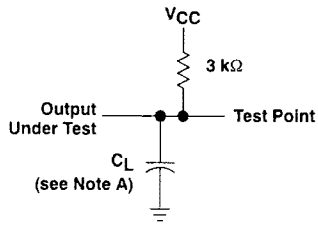


LOAD CIRCUIT FOR t_d, t_r, AND t_f



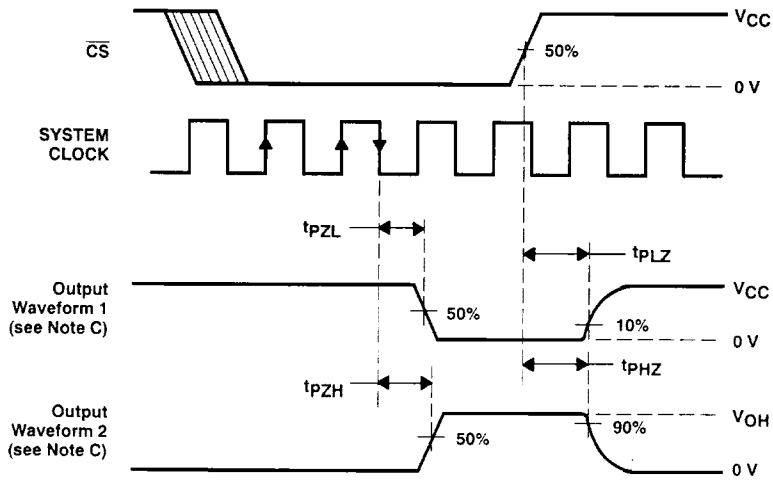
(see Note B)

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

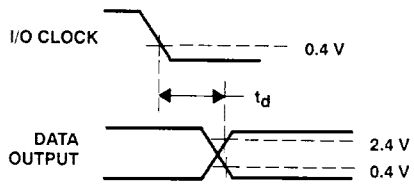


(see Note B)

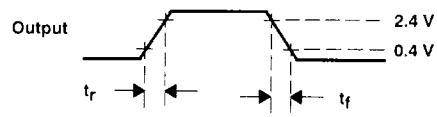
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF

B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC1540 and TLC1541 are complete data acquisition systems on single chips. Each includes such functions as sample and hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs: chip select ($\overline{CS}$), address input, I/O clock, and system clock. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1540 and TLC1541 can complete conversions in a maximum of 21 μs, while complete input-conversion-output cycles can be repeated at a maximum of 31 μs.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the system clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The system clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the DATA OUT pin is in a 3-state condition and the address input and I/O clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with its counterpart pins on additional A/D devices when additional TLC1540/1541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the system clock after a low $\overline{CS}$ transition before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the data out pin (or "on DATA OUT").
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O clock. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O pin, and the sixth, seventh, eighth, ninth, and tenth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final tenth clock cycle is applied to the I/O clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 44 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O clock line. If glitches occur on the I/O clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the system and I/O clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and the system clock pin subsequently receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must go high after the eighth I/O clock that has been recognized by the device so that a $\overline{CS}$ low level will be recognized on the falling edge of the tenth I/O clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O clock pulses and will shift in an erroneous address.

For certain applications, such as strobing, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample and hold begins sampling upon the falling edge of the fourth I/O clock cycle, the hold function is not initiated until the fallling edge of the tenth I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the tenth I/O clock cycle until the moment at which the analog signal must be converted. The TLC1540/TLC1541 will continue sampling the analog input until the tenth falling edge of the I/O clock. The control circuitry or software will then immediately lower the I/O clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.