

# M X T 3 0 2 0

## Circuit Coprocessor for ATM

### Typical Applications

#### WAN access "common card" services

- AAL1-SDT, AAL1-UDT, AAL2, AAL5
- Inverse Multiplexing for ATM (IMA)
- Cell Relay (T1/E1 UNI)
- Frame Relay with external hardware
- Circuit Emulation
- Any service on any link concurrently

#### Integrated Services applications

- AAL1/AAL5 backplane fabrics
- Voice/packet over ATM

#### PBX and mobile trunking

### Distinctive Characteristics

#### High port density

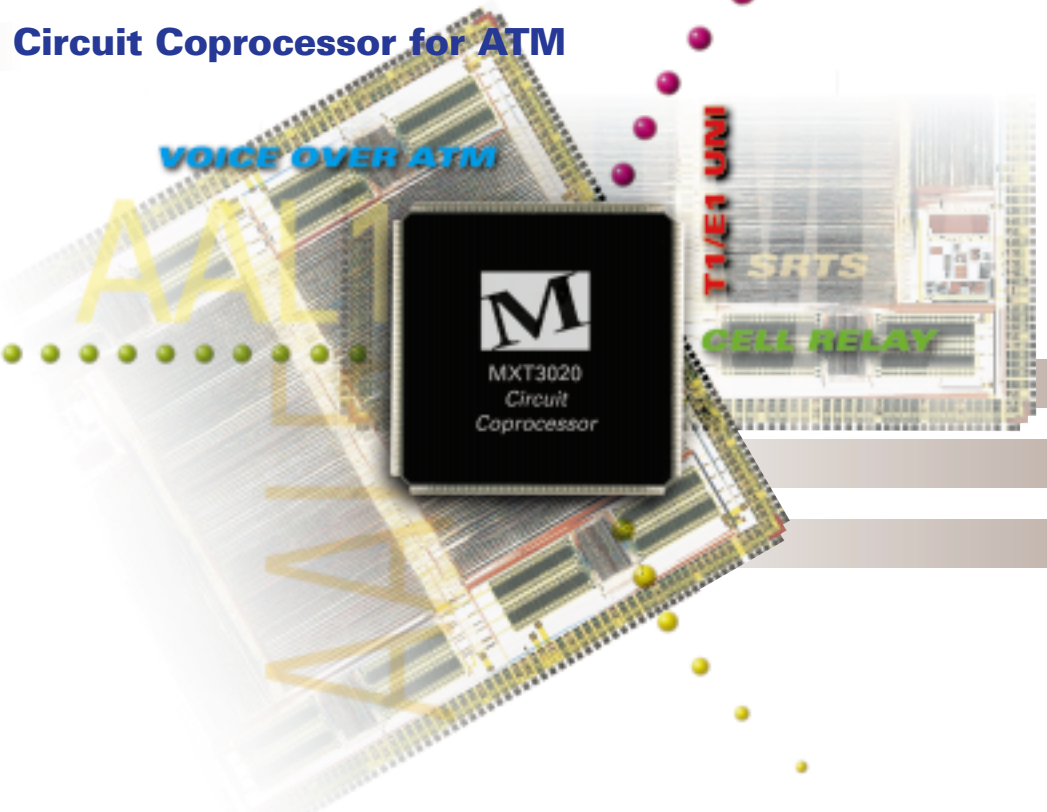
- Up to four MXT3020s per MXT3010
- 8 T1/E1/J2 links per MXT3020 through standard framers or
- 16 bi-directional computer telephony bus wires (MVIP/SCSA) per MXT3020

#### Unparalleled performance

- Multiple services concurrently
- Each MXT3020 can support 2048 DSOs with up to 1024 virtual connections

#### Programmability

- Adapts to new or changing standards
- Supports custom features
- Operates as an MXT3010 coprocessor
- Requires only new MXT3010 firmware for field upgrades



The MXT3020 is a circuit coprocessor for building systems that integrate ATM, packet-based technologies and TDM circuits – including voice-over-ATM products. Together with the MXT3010, the MXT3020 delivers the performance and features to support multiple services concurrently, such as structured and unstructured AAL1 circuit emulation, T1/E1 UNI, Inverse Multiplexing for ATM (IMA), AAL2, and TM 4.0 compliant AAL5. With up to four MXT3020s connected to a single MXT3010, systems can be developed with any combination of up to 32 T1, E1 or J2 links or up to 64 bi-directional computer telephony bus wires (up to 8 Mbps each) with support for SCSA and MVIP.

Developers can license prepackaged software that runs on the MXT3010 and MXT3020 or may write their own custom software. Maker's software product for the MXT3020 is:

**CircuitMaker™:** firmware for ATM/TDM/packet interworking using the MXT3010 Cell Processor and MXT3020 Circuit Coprocessor. CircuitMaker supports both WAN access "common card" services and integrated services applications. Built upon a modular software framework, CircuitMaker is customizable and expandable.



# Applications

## Multi-Service WAN Access

### Unique Integration

An MXT3010/MXT3020-based design delivers unparalleled flexibility and integration to multi-service WAN edge and access applications. It has the performance to support a channelized DS3 or E3 by connecting up to four MXT3020s to a single MXT3010, and has the flexibility to integrate voice, Nx64kbps TDM, IMA, Cell Relay over T1/E1 UNIs, and Frame Relay over ATM. This solution delivers *Any Service, Any Link* capabilities.

### Performance and Programmability

The MXT3010, the same cell processor used in Maker Communications's 622 Mbps SAR application, is the anchor of this system. For interworking ATM to packet interfaces such as Frame Relay, the MXT3010 supports integrated TM 4.0 compliant AAL5 functionality. It also provides the performance and programmability to support multiple services simultaneously. Features that deliver this unparalleled performance include:

- A unique, programmable RISC core (the SWAN™ processor) optimized for cell processing tasks. This processor has single-cycle performance running at twice the system clock, a highly efficient instruction set accomplishing complex functions with fewer instructions, and zero-time context switching for 100% deterministic behavior.
- Multiple independent on-chip execution units, including three DMA controllers, cell buffer RAM, and dedicated cell scheduling hardware.

### On-Chip Clock Recovery for AAL1-UDT

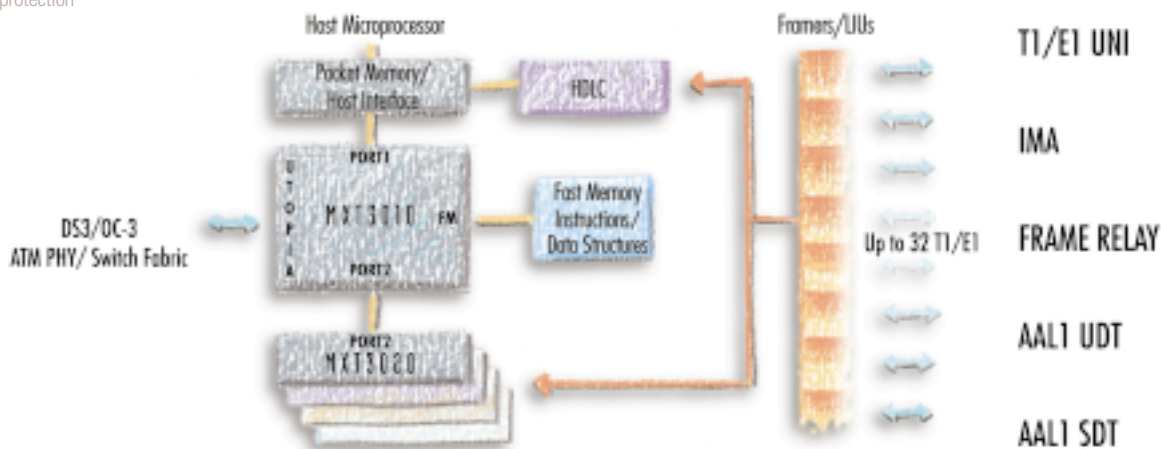
The MXT3020 includes integrated SRTS and Adaptive clock recovery support, requiring no off-chip hardware. Each link includes an independent digital PLL for clock generation and its own SRTS value generation hardware. Powerful and flexible algorithms can be implemented with MXT3010 firmware to deliver superior and targeted jitter/wander characteristics.

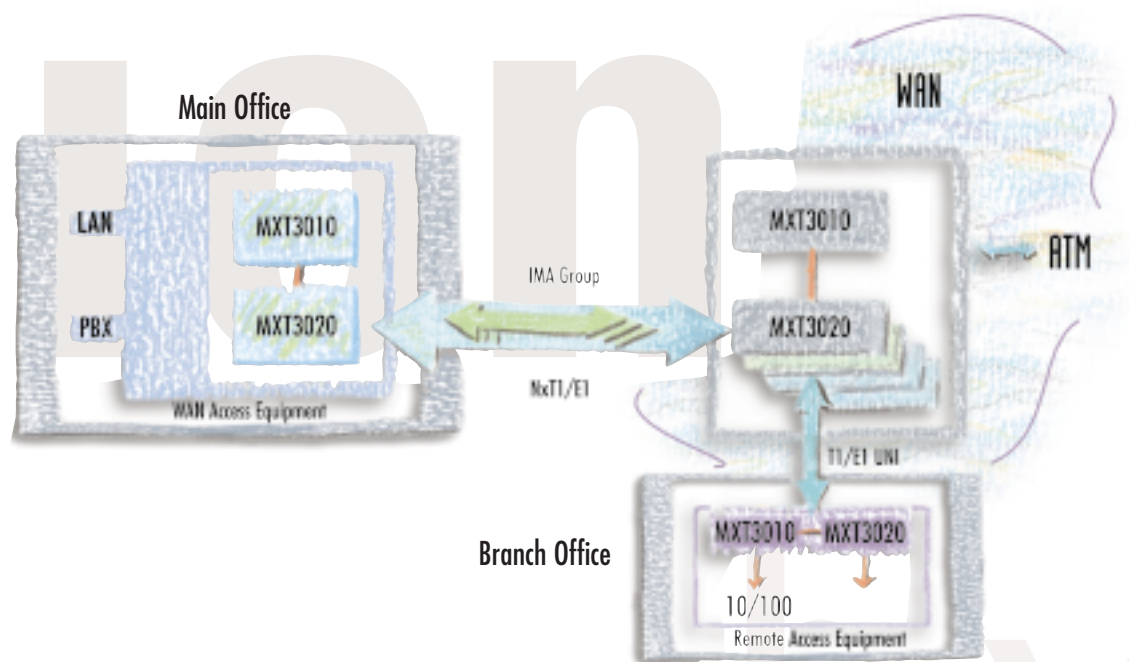
### Multi-Service WAN Access Equipment

- Any Service, Any Link down to a DS0
- 32 T1/E1 links
- Programmable architecture delivers unique investment protection

### Hardware Assist

The MXT3020's data moving engines provide hardware assist for circuit related services, such as AAL1, Cell Relay and IMA. The MXT3020 maps TDM data between ATM cell payloads and serial circuits in order to perform both structured (SDT) and unstructured data transfer (UDT) AAL1. In order to support T1/E1 UNIs for Cell Relay, the MXT3020 includes cell delineation, HEC generation/checking, CRC-10 and cell payload scrambling.





## ATM over T1/E1

The MXT3010/MXT3020 chipset supports both Cell Relay and IMA for transmitting ATM cells over T1/E1 links. It also supports AAL5 and Circuit Emulation Services over AAL1 and/or AAL2 to support integrated voice and data over ATM. The MXT3020 is an ideal solution for this application given its high level of integration and programmability.

### Cell Relay

The MXT3010 cell processor supports comprehensive Cell Relay functionality, including cell flow switching with VPI/VCI translation, per-VC statistics and sophisticated flow control including partial- and early packet discard mechanisms. Developers can tailor applications to meet unique system requirements using the MXT3010's programmable architecture.

The MXT3020 connects directly to T1/E1 framers and includes the following hardware mechanisms for T1/E1 UNI support: cell delineation, HEC generation/checking, CRC-10 and cell scrambling. The MXT3020's integrated frame storage and circuit interface logic ensure that cell processing tasks can proceed while TDM data is captured in the background.

### IMA

The MXT3010 cell processor possesses the power and flexibility to support an IMA firmware application. For applications requiring a dedicated IMA function, an MXT3010 delivers a low-cost solution. The addition of an MXT3020(s) to the solution provides further benefits:

- The flexibility to support additional services in the future
- The density of a hardware platform capable of supporting 32 T1s
- The possibility of leveraging a common host interface across other MXT3020-based designs

## Connections to AAL1/AAL5 ATM Backplanes

The MXT3010/MXT3020 chipset supports the services required to integrate packets and Nx64kbps TDM connections over an ATM backplane. It supports AAL5 for sending and receiving packets. It can also implement AAL1 circuit emulation services, including both Structured Data Transfer (SDT) and Unstructured Data Transfer (UDT) types, for switching circuits at both the DS0 and T1/E1/J2 levels through a cell-based fabric.

### Customization

The MXT3010/MXT3020 chipset has the flexibility required to function in a wide range of system designs. Cell-based backplane designs are system-specific and often impose unique implementation requirements. One example is proprietary routing tags. It can support 52 or 56 byte ATM cells with optional HEC insertion/checking, including proprietary interpretations of the header/routing tag fields. The MXT3010 is unique in its ability to deliver the performance of hardwired approaches using a programmable architecture. MXT3010/MXT3020-based systems can be customized to fit specific applications and can evolve to meet new requirements through simple firmware upgrades.

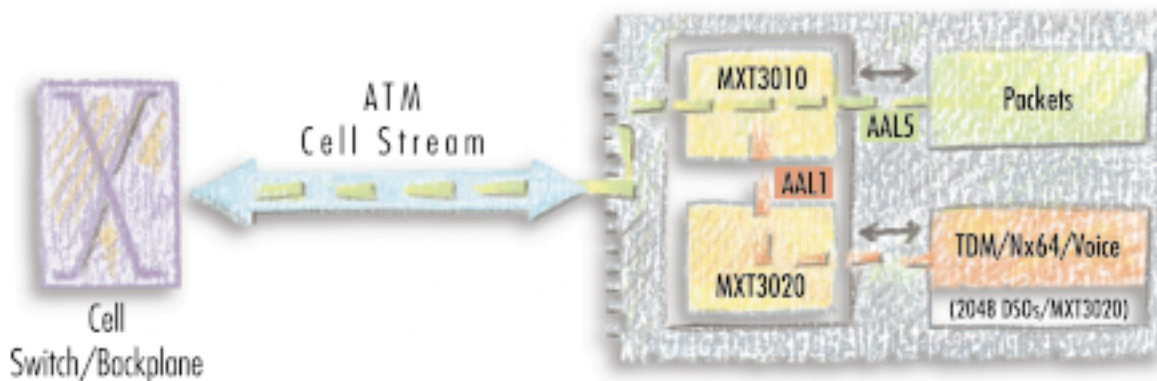
### Truly Integrated Services

The chipset provides per-VC traffic shaping/scheduling for both AAL1 and AAL5 connections. No external cell multiplexing is required and all services can be integrated through a single architecture.

For packet-only cards, the MXT3010 can be used alone - eliminating circuit hardware that is not required. More importantly, development time can be reduced because the host application interface can be the same as for cards that support TDM circuits. In contrast, if different SAR solutions are used for circuit and packet data, two separate interfaces must be supported.

### Integrated AAL1/AAL5 Support

The MXT3010/MXT3020 chipset provides a unified mechanism for integrating packet-based technologies and TDM data over a cell switch or backplane. The programmable architecture ensures flexibility in meeting custom requirements.



# Theory of

The MXT3020, as a coprocessor for the MXT3010, provides two main functions: flexible data moving engines and standard circuit interfaces. Its data moving engines are optimized for TDM to cell interworking functions, while its circuit interfaces support T1/E1/J2 framers and/or TDM highways such as SCSA and MVIP computer telephony buses.

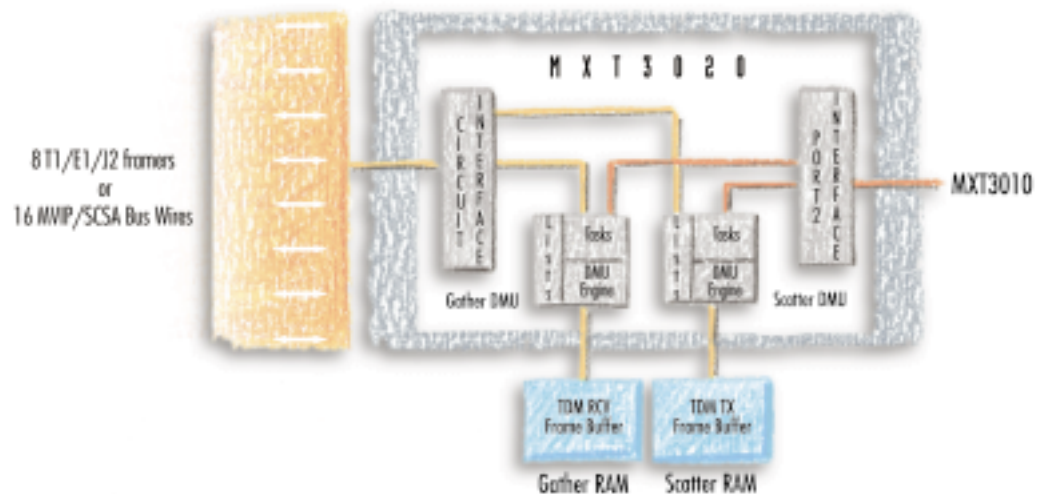
Through its Port2 interface, the MXT3010 cell processor programs and controls the MXT3020 with memory-mapped accesses of MXT3020 registers and memories. Using DMA operations, the MXT3010 configures MXT3020 registers, builds data mover instructions, and constructs cells and transfers them to/from the MXT3020.

Internal to the MXT3020 are Data Mover Units which support the structured and unstructured data modes of AAL1, AAL2, T1/E1 UNI connections for Cell Relay and IMA. The programming model for the Data Mover Units is based on two concepts: lists and tasks. A list is the code that describes the ordering and movement of data between cells (or SAR SDUs) and TDM frames in frame buffer memory. A task is a set of control words that configures and initiates Data Mover operations.

## Circuit Interface

The circuit interface is the logic that receives and transmits TDM serial data. It supports eight serial link pairs. Each link pair:

- Supports the following rates: 1.544, 2.048, 4.096, 6.144 or 8.192 MHz.
- Supports structured or unstructured (SDT and UDT) AAL1 circuit emulation.
- Includes independent clocking and frame synchronization (for T1/E1/J2 mode).
- Can be configured independently in unidirectional (one 2-wire port for connection to standard framers) or bi-directional (two single-wire bi-directional ports capable of supporting SCSA and MVIP telephony buses) mode.
- Can be tri-stated on a DS0-by-DS0 basis.
- Includes per-link SRTS and Adaptive clock recovery capabilities.



## Frame Buffer Memory Interface

The MXT3020 connects to two frame buffer memories: one each for scatter (ATM to TDM) and gather (TDM to ATM). Scatter/gather memories are for both frame buffer storage and control memory. Each memory interface is 16-bits wide and can handle up to 512 Kbytes of pipelined synchronous SRAM, which provides up to 32 msec of cell delay variation tolerance (CDVT).

## Port2 Interface

The Port2 Interface connects the MXT3020 to the MXT3010's Port2 DMA interface and provides a path for programming the MXT3020. Both cells and payload (SAR SDU) data destined for TDM circuits are transferred through this interface. Up to four MXT3020s can be connected to an MXT3010 with minimal external logic.

**Ordering Information**

MXT3020-C60: 60 MHz MXT3020  
 MXT3020-C: 50 MHz MXT3020  
 MXT3020-C40: 40 MHz MXT3020  
 MXT3020-C33: 33 MHz MXT3020

**Summary Characteristics**

**Power Supply:** 3.3V  
**I/O Voltage Levels:** 3.3V- and 5V-compatible  
**Supply Current:** 379mA max @ 50 MHz and 3.3V  
**Maximum Power Dissipation:** 0.825W @ 33 MHz, 1W @ 40MHz, 1.25W @ 50 MHz  
**Typical Power Dissipation @ 50 MHz:** 0.75W  
**Maximum Operating Junction Temperature:** 125 °C  
**Operating Free Air Temperature Range:** 0-70 °C



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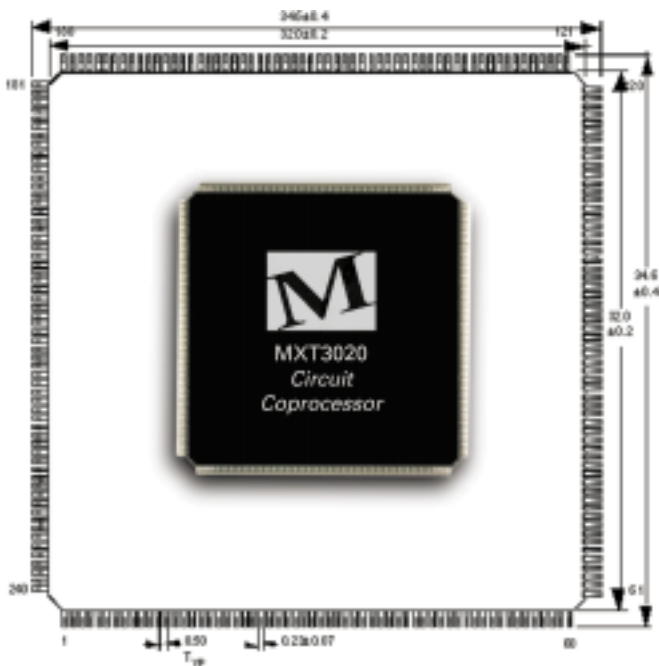
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Product Information:

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Physical Package		
Package Type	Body Size (mm)	Lead Pitch (mm)
PQFP 240	32.0 x 32.0 x 3.6	0.5

$\theta_{jc}$ (°C/W)	$\theta_{ja}$ (°C/W)	
	*Still Air	*Air Flow (1m/sec)
6.5	30	20

\* These numbers will vary depending on board stack-up and orientation.