

# Advanced Data Link Controller

## S6854/S68A54/S68B54

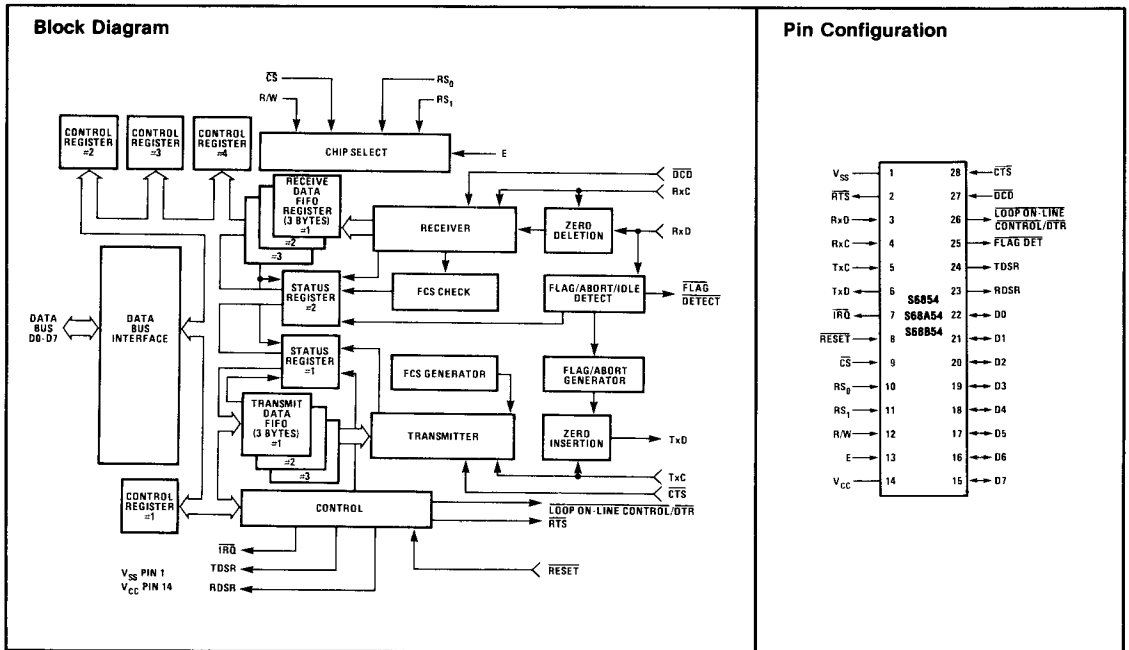
### Features

- S6800 Compatible
- Protocol Features
  - Automatic Flag Detection and Synchronization
  - Zero Insertion and Deletion
  - Extendable Address, Control and Logical Control Fields (Optional)
  - Variable Word Length Info Field — 5, 6, 7, or 8-bits
  - Automatic Frame Check Sequence Generation and Check
  - Abort Detection and Transmission
  - Idle Detection and Transmission
- Loop Mode Operation
- Loop Back Self-Test Mode
- NRZ/NRZI Modes

- Quad Data Buffers for Each Rx and Tx
- Prioritized Status Register (Optional)
- MODEM/DMA/Loop Interface

### General Description

The S6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP), High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.



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### Absolute Maximum Ratings\*

Supply Voltage	- 0.3 to + 7.0V
Input Voltage	- 0.3 to + 7.0V
Operating Temperature Range	0° to + 70°C
Storage Temperature Range	- 55° to + 150°C
Thermal Resistance	70° C/W

\* This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

### Electrical Characteristics: ( $V_{CC} = 5.0V \pm 5\%$ , $V_{SS} = 0$ , $T_A = 0^\circ C$ to $+ 70^\circ C$ unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$V_{IH}$	Input High Voltage	$V_{SS} + 2.0$		Vdc		
$V_{IL}$	Input Low Voltage			$V_{SS} + 0.8$	Vdc	
$I_{IN}$	Input Leakage Current	All Inputs Except $D_0$ - $D_7$	1.0	2.5	$\mu$ Adc	$V_{IN} = 0$ to 5.25 Vdc
$I_{TSI}$	Three-State (Off State) Input Current	$D_0$ - $D_7$	2.0	10	$\mu$ Adc	$V_{IN} = 0.4$ to 2.4 Vdc $V_{CC} = 5.25$ Vdc
$V_{OH}$	Output High Voltage	$D_0$ - $D_7$ All Others	$V_{SS} + 2.4$ $V_{SS} + 2.4$		Vdc Vdc	$I_{LOAD} = -205\mu$ Adc $I_{LOAD} = -100\mu$ Adc
$V_{OL}$	Output Low Voltage			$V_{SS} + 0.4$	Vdc	$I_{LOAD} = 1.6$ mAdc
$I_{LOH}$	Output Leakage Current (Off State)	$\overline{IRQ}$	1.0	10	$\mu$ Adc	$V_{OH} = 2.4$ Vdc
$P_B$	Power Dissipation			850	mW	
$C_{IN}$	Capacitance	$D_0$ - $D_7$ All Other Inputs		12.5 7.5	pF pF	$V_{IN} = 0$ , $T_A = 25^\circ C$ , $f = 1.0$ MHz
$C_{OUT}$		$\overline{IRQ}$ All Others		5.0 10	pF pF	

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$PW_{CL}$	Minimum Clock Pulse Width, Low	700		450		280		ns
$PW_{CH}$	Minimum Clock Pulse Width, High	700		450		280		ns
$f_C$	Clock Frequency		0.66		1.0		1.5	MHz
$t_{RDSU}$	Receive Data Setup Time	250		200		120		ns
$t_{RDH}$	Receive Data Hold Time	120		100		60		ns
$t_{RTS}$	Request-to-Send Delay Time		680		460		340	ns
$t_{TDD}$	Clock-to-Data Delay for Transmitter		460		320		250	ns
$t_{FD}$	Flag Detect Delay Time		680		460		340	ns
$t_{DTR}$	DTR Delay Time		680		460		340	ns
$t_{LOC}$	Loop On-Line Control Delay Time		680		460		340	ns
$t_{RDSR}$	RDSR Delay Time		540		400		340	ns
$t_{TDSR}$	TDSR Delay Time		540		400		340	ns
$t_{IR}$	Interrupt Request Release Time		1.2		0.9		0.7	$\mu$ s
$t_{RES}$	Reset Minimum Pulse Width	1.0		0.65		0.40		$\mu$ s
$t_r, t_f$	Input Rise and Fall Times (except Enable) (0.8V to 2.0V)		1.0*		1.0*		1.0*	$\mu$ s

\* 1.0 $\mu$ s or 10% of the pulse width, whichever is smaller.

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**Bus Timing Characteristics** ( $V_{CC} = +5.0V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$  unless otherwise noted.)

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read</b>								
$t_{CYC}$	Enable Cycle Time	1.0		0.666		0.50		$\mu s$
$PW_{EH}$	Enable Pulse Width, High	0.45		0.28		0.22	25	$\mu s$
$PW_{EL}$	Enable Pulse Width, Low	0.43		0.28		0.21		$\mu s$
$t_{AS}$	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
$t_{DDR}$	Data Delay Time		320		220		180	ns
$t_H$	Data Hold Time	10		10		10		ns
$t_{AH}$	Address Hold Time	10		10		10		ns
$t_{EF}$ , $t_{EF}$	Rise and Fall Time for Enable Input		25		25		25	ns
<b>Write</b>								
$t_{CYCE}$	Enable Cycle Time	1.0		0.666		0.50		$\mu s$
$PW_{EH}$	Enable Pulse Width, High	0.45		0.28		0.22		$\mu s$
$PW_{EL}$	Enable Pulse Width, Low	0.43		0.28		0.21		$\mu s$
$t_{AS}$	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
$t_{DSW}$	Setup Time	195		80		60		ns
$t_H$	Data Hold Time	10		10		10		ns
$t_{AH}$	Address Hold Time	10		10		10		ns
$t_{EF}$ , $t_{EF}$	Rise and Fall Time for Enable Input		25		25		25	ns