Freescale Semiconductor
Technical Data

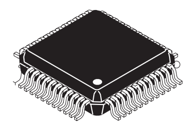
MPC92474
Rev 0, 3/2005

LVPECL Clock Synthesizer w/Spread Spectrum

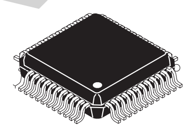
The MPC92474 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 35 MHz to 700 MHz and the support of differential LVPECL output signals the device meets the needs of the most demanding clock applications.

MPC92474

LOW VOLTAGE CLOCK SYNTHESIZER w/SPREAD SPECTRUM



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932-03



AC SUFFIX
48-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 932-03

Features

- 35 MHz to 700 MHz synthesized clock output signal
- Two differential LVPECL outputs
- LVCMOS compatible control inputs
- Two on-chip crystal oscillators for reference frequency generation
- Spread Spectrum output for EMI reduction
- Low Phase Noise
- Serial programming interface
- Parallel programming interface for power-up
- 48-lead LQFP packaging
- 48-lead Pb-free package available
- SiGe Technology
- Ambient temperature range 0°C to +70°C

Functional Description

The MPC92474 is a PLL based clock synthesizer with dual LVPECL outputs. The device uses a reference input that is selectable from 1 of 4 input sources. These sources are either of two crystal oscillator inputs, a differential input or a single-ended input clock. Each of the two internal crystal oscillators uses an external quartz crystal as the basis of its frequency reference. The differential input will accept many differential input levels including industry standard LVPECL levels.

The selected input reference frequency is divided by a configurable P divider of either ÷1, ÷4 or ÷8 and then multiplied by the internal PLL to the VCO frequency. The VCO within the PLL operates over a range of 560 to 700 MHz. Its output is then scaled by two independant output dividers that may be configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-dividers of NA and NB determine the output frequency of each of the two LVPECL differential outputs. The PLL post-dividers of NA and NB are configured through either the serial or the parallel interfaces, and can provide one of eight division ratios (1, 2, 3, 4, 5, 6, 8, or 16). The selected reference input is available on the REF_CLK output pin.

In addition the MPC92474 has a TEST output that reflects various internal node values, and is controlled by the T[1:0] bits in the serial data stream.

The MPC92474 offers spread spectrum modulation on the output frequency for system EMI reduction if desired. Spread spectrum defaults to a disabled state and is enabled through the serial interface. Both center spread and down spread formats may be selected. Also the amount of spread spectrum modulation is selectable through the serial interface. See the Applications section for additional details on Spread Spectrum operation and configuration.

The MPC92474 is available in a 48 lead LQFP package. A Pb-free package is also available.

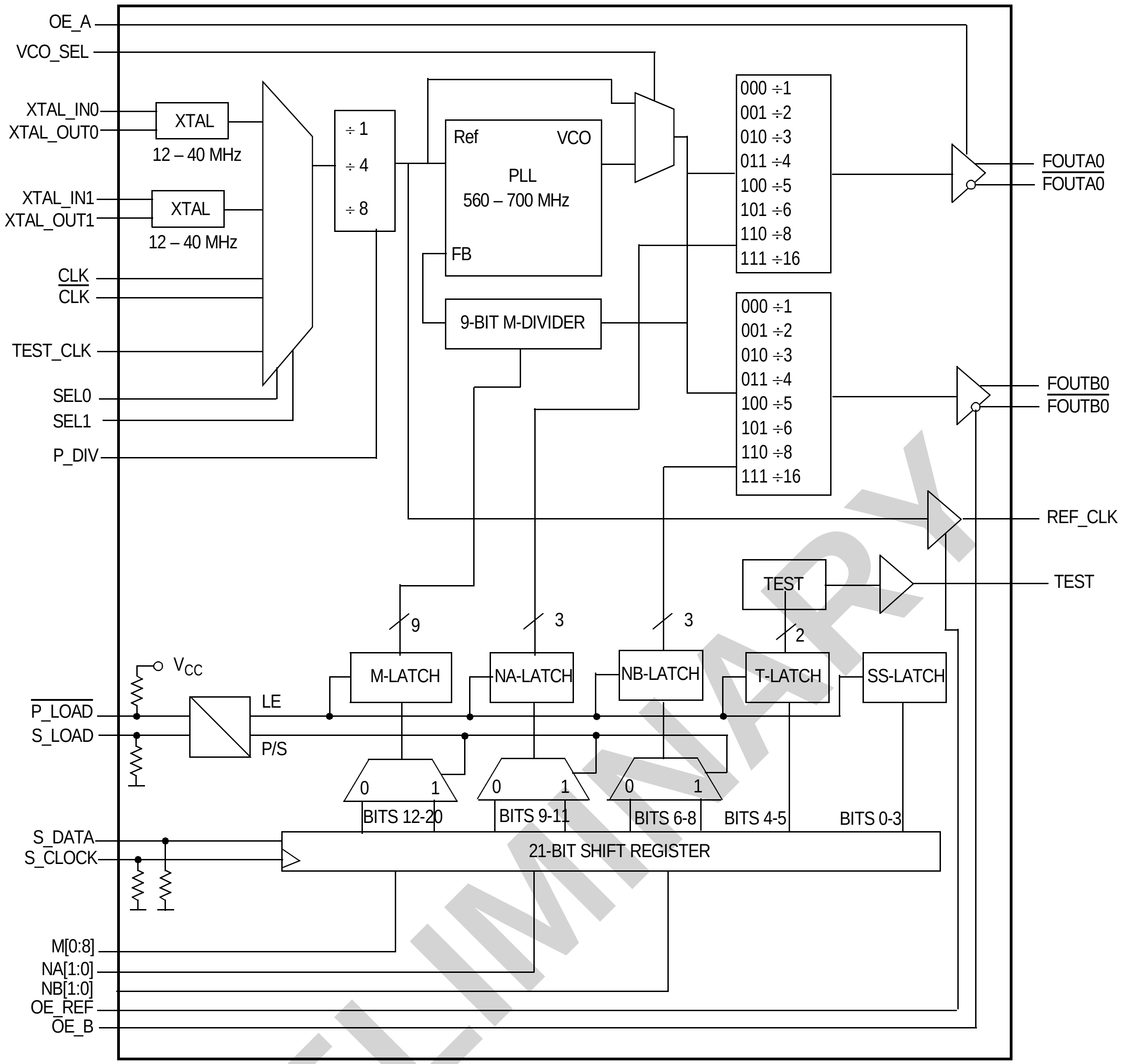
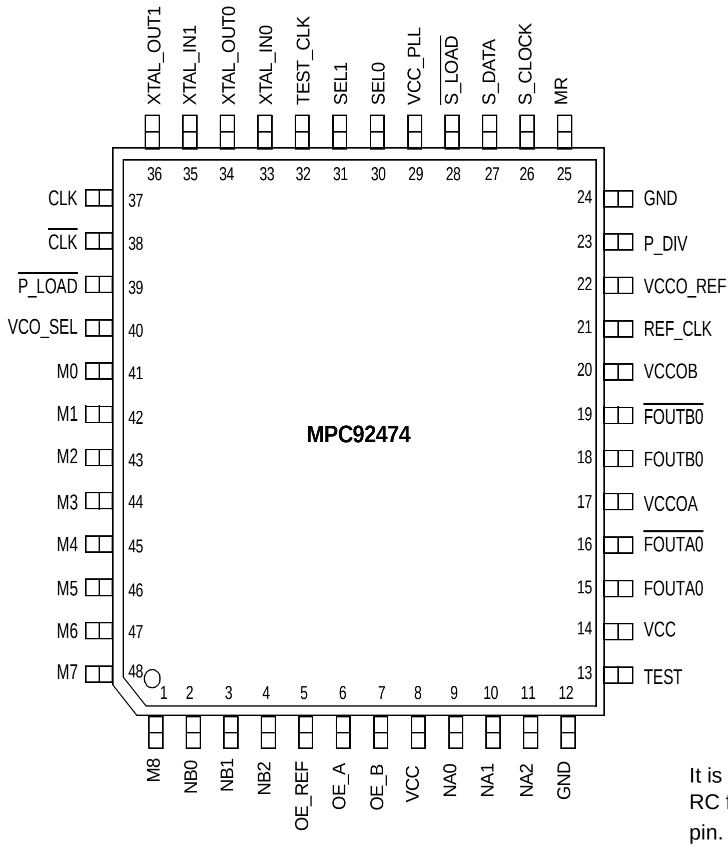


Figure 1. MPC92474 Logic Diagram



It is recommended to use an external RC filter for the analog V_{CC_PLL} supply pin. Please see the application section for details.

Figure 2. MPC92474 48-Lead Package Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default[1]	Type	Function
XTAL_IN0 XTAL_OUT0 XTAL_IN1 XTAL_OUT1			Analog	Crystal oscillators interface. See applications section for recommended crystal specifications.
CLK, $\overline{\text{CLK}}$	Input	0 M	LVPECL	LVPECL clock input.
TEST_CLK	Input	0	LVCMOS	LVCMOS clock input.
FOUTA0, $\overline{\text{FOUTA0}}$ FOUTB0, $\overline{\text{FOUTB0}}$	Output		LVPECL	Differential clock outputs.
SEL0 SEL1	Input	0 0	LVCMOS	Reference input source select.
REF_CLK	Output			Reference clock output.
TEST	Output		LVCMOS	Test and device diagnosis output.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This input controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{\text{P\_LOAD}}$	Input	0	LVCMOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive.

1. A 0 represents an internal pulldown. A 1 represents an internal pullup. A M represents pulldown and pullup Vcc/2 biasing.

Table 1. Pin Configurations (Continued)

Pin	I/O	Default[1]	Type	Function
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:8]	Input	000100000	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
NA[2:0]	Input	011	LVCMOS	Parallel configuration for Post-PLL divider (NA). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
NB[2:0]	Input	011	LVCMOS	Parallel configuration for Post-PLL divider (NB). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
P_DIV	Input	M	LVCMOS	Prescale divider (P) configuration.
OE_A	Input	1	LVCMOS	Output enable (active high) for FOUTA0. The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output. OE = L low stops F_{OUT} in the logic low state (F_{OUT} = L, $\overline{\text{FOUT}}$ = H).
OE_B	Input	1	LVCMOS	Output enable (active high) for FOUTB0. The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output. OE = L low stops F_{OUT} in the logic low state (F_{OUT} = L, $\overline{\text{FOUT}}$ = H).
OE_REF	Input	0	LVCMOS	Output enable (active high) for REF_CLK. The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output. OE = L low stops F_{OUT} in the logic low state (F_{OUT} = L, $\overline{\text{FOUT}}$ = H).
VCO_SEL	Input	1	LVCMOS	PLL bypass selected when = 0. Normal operation when = 1.
MR	Input	0	LVCMOS	Device reset, active high.
GND	Supply	Supply	Ground	Negative power supply (GND).
V_{CC}	Supply	Supply	V_{CC}	Positive power supply for core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CCOA}	Supply	Supply	V_{CC}	Positive power supply for A bank output. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CCOB}	Supply	Supply	V_{CC}	Positive power supply for B bank output. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply	Supply	V_{CC}	PLL positive power supply (analog power supply).

1. A 0 represents an internal pulldown. A 1 represents an internal pullup. A M represents pulldown and pullup Vcc/2 biasing.

Table 2. Output Frequency Range and PLL Post-Divider N

N			Output Division	Output Frequency Range
0	0	0	1	560 - 700 MHz
0	0	1	2	280 - 350 MHz
0	1	0	3	186.66 - 233.33 MHz
0	1	1	4	140 - 175 MHz
1	0	0	5	112 - 140 MHz
1	0	1	6	93.33 - 116.66 MHz
1	1	0	8	70 - 87.5 MHz
1	1	1	16	35 - 43.75 MHz

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 48 Thermal Resistance Junction to Ambient JESD 51-3, single layer test board JESD 51-6, 2S2P multilayer test board		 83.1 73.3 68.9 63.8 57.4 59.0 54.4 52.5 50.4 47.8	 86.0 75.4 70.9 65.3 59.6 60.6 55.7 53.8 51.5 48.8	 °C/W °C/W °C/W °C/W °C/W °C/W °C/W °C/W °C/W °C/W	 Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
θ_{JC}	LQFP 48 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 4. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3. V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs ($\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current(1)			±200	μA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}(2)						
V_{OH}	Output High Voltage(3)	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage(3)	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage(3)	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage(3)			0.55	V	I_{OH} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			100	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to V_{TT} = V_{CC} – 2 V.
3. The MPC92474 TEST output levels are compatible to the MC12429 output levels.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)**[1]**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range	12		40	MHz	
f_{VCO}	VCO Frequency Range[2]	560		700	MHz	
f_{MAX}	Output Frequency N = 000 (÷1) N = 001 (÷2) N = 010 (÷3) N = 011 (÷4) N = 100 (÷5) N = 101 (÷6) N = 110 (÷8) N = 111 (÷16)	560 280 186 140 112 93 70 35		700 350 233 175 140 116 87 43	MHz MHz MHz MHz MHz MHz MHz MHz	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[3]	0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width (S_LOAD, P_LOAD)	50			ns	
t_S	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20			ns ns ns	
t_S	Hold Time S_DATA to S_CLOCK M, N to P_LOAD	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter		TBD		ps	
$t_{JIT(PER)}$	Period Jitter		TBD		ps	
t	Phase Noise		TBD		dBc/Hz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
SSM_{fmod}	Spread Spectrum Modulation Frequency		32		KHz	
SSM_{dev}	Spread Spectrum Modulation Deviation SS[3:0] = 1010 SS[3:0] = 1100 SS[3:0] = 0010 SS[3:0] = 0100		-0.5 -1.0 +-0.25 +-0.5		% % % %	f_{out} = 200 MHz

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \div P * M$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

PROGRAMMING INTERFACE

Programming the MPC92474

Programming the MPC92474 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at each of the two outputs. The output frequency can be represented by this formula:

$$F_{OUTA} = (f_{XTAL} \div P) \times (M) \div (NA) \quad (1)$$

$$F_{OUTB} = (f_{XTAL} \div P) \times (M) \div (NB) \quad (2)$$

where f_{XTAL} is the crystal frequency, P is the prescale divider value, M is the PLL feedback-divider and NA and NB are the PLL post-divider for the outputs A or B. The input frequency, the P divider and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL}, P and M must be configured to match the specified VCO frequency range of 560 to 700 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div f_{XTAL} \div P \text{ and} \quad (2)$$

$$M_{MAX} = f_{VCO,MAX} \div f_{XTAL} \div P \quad (3)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 140 and M = 175. Table 7 shows the output frequencies for the allowable M divider values for P = 4 and P = 8.

Table 7. MPC92474 Frequency Operating Range

P	M	M[8:0]	Output frequency for f_{XTAL} = 16 MHz and for N =							
			1	2	3	4	5	6	8	16
4	140	010001100	560	280	186.66	140	112	93.33	70	35
4	145	010010001	580	290	193.33	145	116	96.66	72.5	36.25
4	150	010010110	600	300	200	150	120	100	75	37.5
4	155	010011011	620	310	206.67	155	124	103.33	77.5	38.75
4	160	010100000	640	320	213	160	128	106.66	80	40
4	165	010100101	660	330	220	165	132	110	82.5	41.25
4	170	010101010	680	340	226	170	136	113.33	85	42.5
4	175	010101111	700	350	233.33	175	140	116.66	87.5	43.75
8	280	100011000	560	280	186.66	140	112	93.33	70	35
8	285	100011101	570	285	190	142.5	114	95	71.25	35.625
8	290	100100010	580	290	193.33	145	116	96.66	72.5	36.25
8	295	100100111	590	295	196.6667	147.5	118	98.33	73.75	36.875
8	300	100101100	600	300	200	150	120	100	75	37.5
8	305	100110001	610	305	203.33	152.5	122	101.6667	76.25	38.125
8	310	100110110	620	310	206.6667	155	124	103.33	77.5	38.75
8	315	100111011	630	315	210	157	126	105	78.75	39.375
8	320	101000000	640	320	213.33	160	128	106.66	80	40
8	325	101000101	650	325	216.6667	162.5	130	108.33	81.25	40.625
8	330	101001010	660	330	220	165	132	110	82.5	41.25
8	335	101001111	670	335	223.33	167.5	134	111.6667	83.75	41.875
8	340	101010100	680	340	226.6667	170	136	113.33	85	42.5
8	345	101011001	690	345	230	172.5	138	115	86.25	43.125
8	350	101011110	700	350	233.33	175	140	116.6667	87.5	43.75

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M, NA and NB counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW-to-HIGH transition will latch the information present on the M[8:0], NA[1:0] and NB[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[8:0], NA[1:0] and NB[1:0] inputs will affect the FOUT output pairs. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 21 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The SS register is loaded with the first four bits,the test register with the next 2 bits, the NB register with the next three bits, the NA register with the next three and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (SS3, T1, NB2, NA2 and M8). A pulse on the

S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH-to-LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MPC92474 synthesizer. M[8:0], NA[2:0] and NB[2:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[1:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the CMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T1 and T0 control bits are preset to ‘00' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC92474 itself.

Table 8. Test and Debug Configuration for TEST

T[1:0]		TEST Output
T1	T0	
0	0	Logic 0
0	1	S Data Shift Register Output
1	0	M Counter out
1	1	LVCMOS FOUTA0

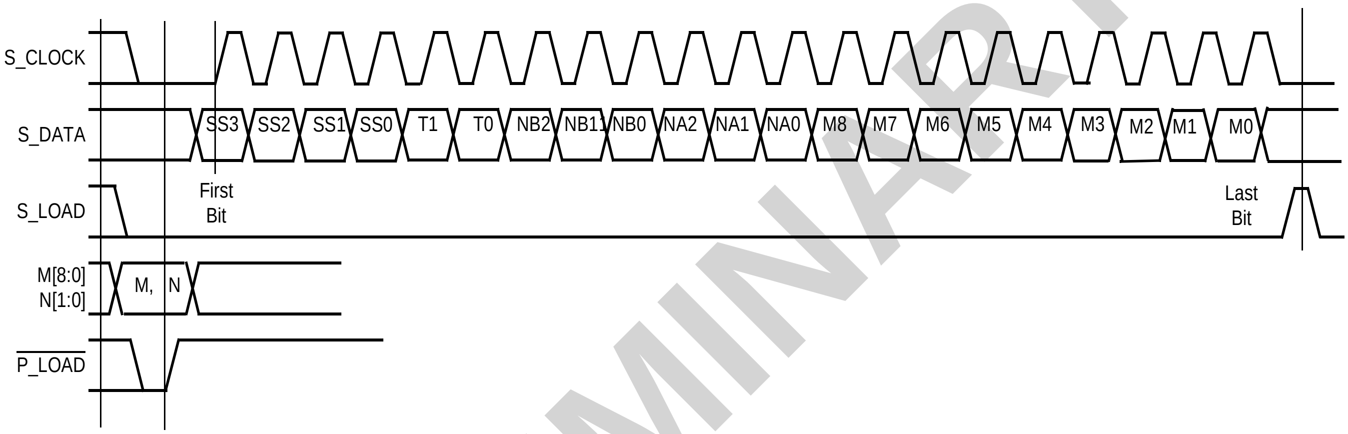


Figure 3. Serial Interface Timing Diagram

Table 9. SSM Operation

SS Bit Pattern				Operation	
SS3	**SS2**	**SS1**	**SS0**	**Mode**	**%**
0	0	0	0	off	0
0	0	0	1	center	TBD
0	0	1	0	center	+-0.25%
0	0	1	1	center	TBD
0	1	0	0	center	+-0.5%
0	1	0	1	center	TBD
0	1	1	0	center	+-1.0%
0	1	1	1	center	TBD
1	0	0	0	off	0
1	0	0	1	down	TBD
1	0	1	0	down	-0.5%
1	0	1	1	down	TBD
1	1	0	0	down	-1.0%
1	1	0	1	down	TBD
1	1	1	0	cown	-2.0%
1	1	1	1	down	TBD

Spread Spectrum Modulation

The MPC92474 offers the option of a spread spectrum modulated output clock. The spread spectrum is controlled via 4 bits in the serial bit stream. These three bits configure the SSM to be enabled and the amount of spread modulation to be selected. See Table 9 for the definition of the four bits. The four additional bits are added at the beginning of the serial data stream and are labeled SS3, SS2, SS1 and SS0. The initial state of SS3, SS2, SS1 and SS0 is 0, 0, 0, 0 which places the MPC92474 in the mode of spread spectrum off. Additionally a parallel load will result in spread spectrum modulation being off. The MPC92469 offers down-spread or center spread using triangle-wave modulation.

Power Supply Filtering

The MPC92474 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC92474 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC92474. Figure 4 illustrates a typical power supply filter scheme. The MPC92474 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC92474 pin of the MPC92474. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 4 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

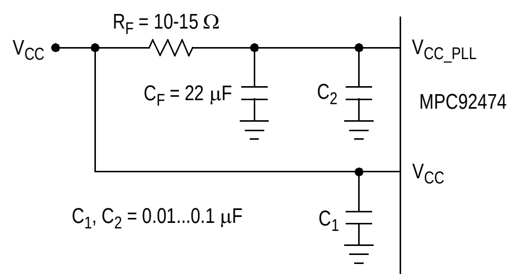


Figure 4. V_{CC_PLL} Power Supply Filter

Using the On-Board Crystal Oscillators

The MPC92474 features two fully integrated Pierce oscillators to minimize system implementation costs. Other than the addition of a crystal no external components are required.The crystal selection should be 10 to 20 MHz, parallel resonant crystal type with a load specification of C_L = 10 pF.

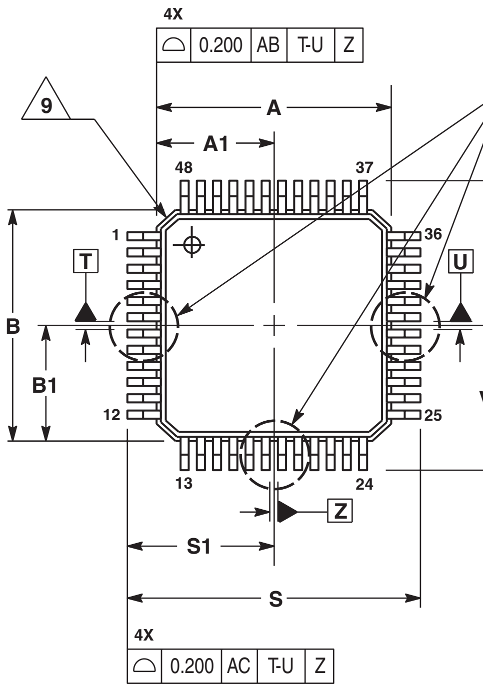
The crystal should be located as close to the MPC92474 XTAL_IN and XTAL_OUT pins as possible to avoid any board level parasitic.

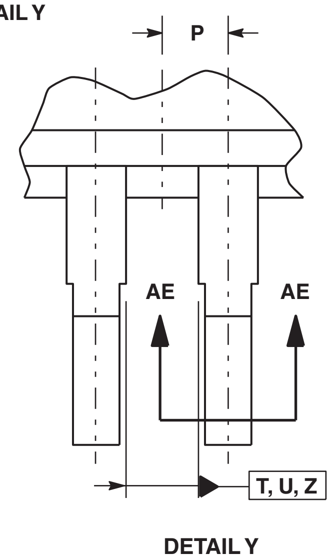
Table 10 specifies the performance requirements of the crystals to be used with the MPC92474.

Table 10. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parrallel Resonance
Shunt Capacitance (C_O)	5–7 pF
Load Capacitance (C_L)	10 pF
Equivalent Series Resistance (ESR)	20 to 60 Ω

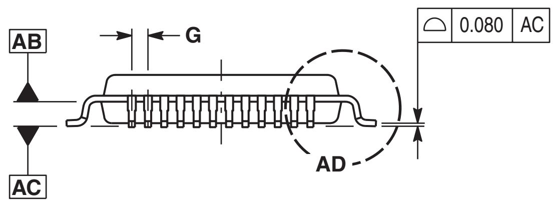
PACKAGE DIMENSIONS

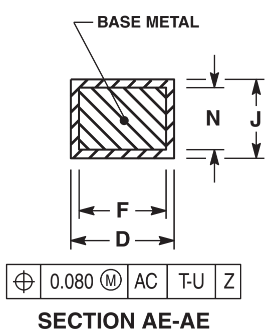


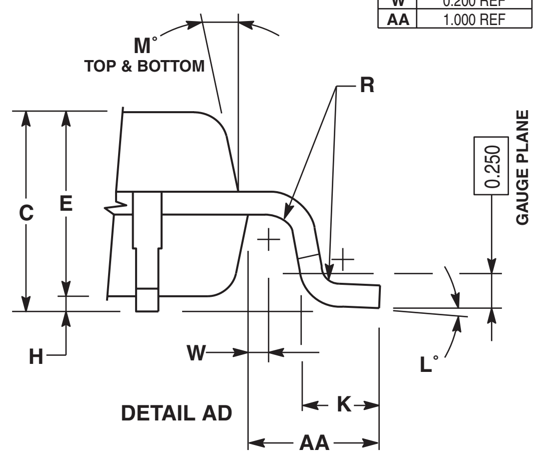


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5m, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLAN AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATAUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0°	7°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	







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How to Reach Us:

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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
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