

MH2M04B1J-7,-8,-10/ MH2M04B1JA-7,-8,-10

NIBBLE MODE 1048576-WORD BY 8-BIT DYNAMIC RAM

DESCRIPTION

The MH2M04B1J, JA is 1048576 word x 8 bit dynamic RAM and consists of eight industry standard 1M x 1 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required.

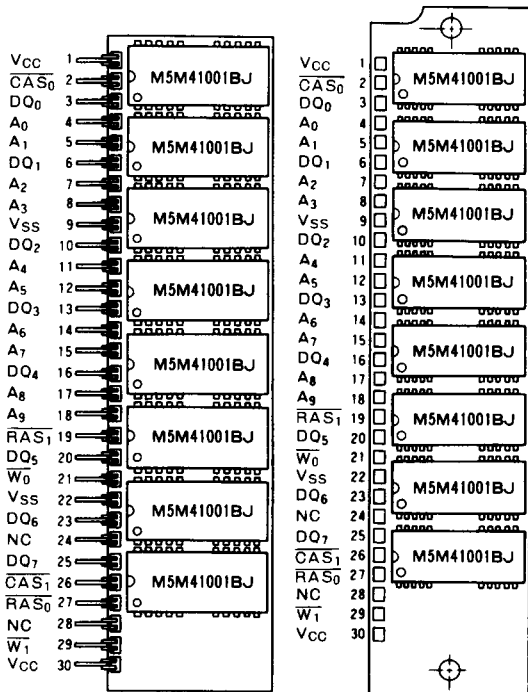
FEATURES

- Performance ranges

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH2M08B1J-7 MH2M04B1JA-7	70	140	1840
MH2M04B1J-8 MH2M04B1JA-8	80	160	1600
MH2M04B1J-10 MH2M04B1JA-12	100	190	1400

- Utilizes industry standard 1M RAMs in SOJ
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation 22mW (max) CMOS input level
- Low operation power dissipation:
MH2M04B1J-7, MH2M04B1JA-7 . . . 3.52W (max)
MH2M04B1J-8, MH2M04B1JA-8 . . . 3.08W (max)
MH2M04B1J-10, MH2M04B1JA-10 . . . 2.64W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22μF x 8) decoupling capacitors
- 512 refresh cycles every 8ms, A₉ Pin is not need for refresh
- Common $\overline{\text{CAS}}$ control for eight common Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operation to prevent contention on Data-In and Data-Out.

PIN CONFIGURATION (TOP VIEW)

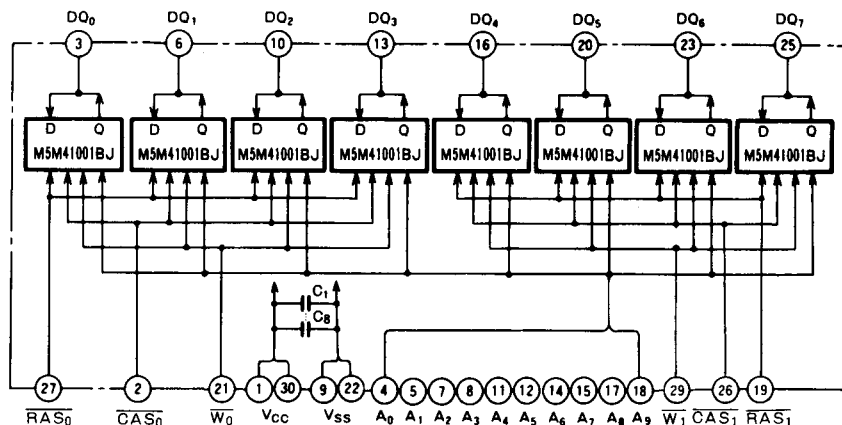


Outline
30N5A (MH2M04B1JA) 30N9A (MH2M04B1J)
NC: NO CONNECTION

APPLICATION

Main memory unit for computers, Refresh memory.

BLOCK DIAGRAM



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FUNCTION

The MH2M04B1J, JA provide, in addition to normal read, and early write operations, a number of other functions, e.g. Nibble mode. $\overline{\text{RAS}}$ -only refresh and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Nibble mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

Table 2 Nibble Mode Addressing Sequence Example

Sequence	Nibble bit	Column address										Row address										
		A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	
$\overline{\text{RAS}}/\overline{\text{CAS}}$	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	External address
toggle $\overline{\text{CAS}}$	2	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	1	
toggle $\overline{\text{CAS}}$	3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	Internal generate address
toggle $\overline{\text{CAS}}$	4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
toggle $\overline{\text{CAS}}$	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a = 25°C	8	W
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage all inputs	-1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} = -5mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current	0V ≤ V _{OUT} ≤ 5.5V	-20		20	μA
I _I	Input current	0V ≤ V _{IH} ≤ 6.5V, Other input pins = 0V	-80		80	μA
I _{CC1(AV)}	Average supply current from V _{CC} operating (Note 3, 4)	MH2M04B1-7	R _{AS} , C _{AS} cycling t _{RC} = t _{WC} = min, output open		640	mA
		MH2M04B1-8			560	
		MH2M04B1-10			480	
I _{CC2}	Supply current from V _{CC} , standby	R _{AS} = C _{AS} = V _{IH} , output open		16	mA	
		R _{AS} = C _{AS} ≥ V _{CC} - 0.5, output open		4		
I _{CC3(AV)}	Average supply current from V _{CC} refreshing (Note 3)	MH2M04B1-7	R _{AS} cycling, C _{AS} = V _{IH} t _{RC} = min, output open		640	mA
		MH2M04B1-8			560	
		MH2M04B1-10			480	
I _{CC5(AV)}	Average supply current from V _{CC} Nibble mode (Note 3, 4)	MH2M04B1-7	R _{AS} = V _{IL} , C _{AS} = cycling t _{NC} = min, output open		320	mA
		MH2M04B1-8			280	
		MH2M04B1-10			240	
I _{CC6(AV)}	Average supply current from V _{CC} C _{AS} before R _{AS} refresh mode (Note 3)	MH2M04B1-7	C _{AS} before R _{AS} refresh cycling t _{NC} = min, output open		640	mA
		MH2M04B1-8			560	
		MH2M04B1-10			480	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1(AV)}, I_{CC3(AV)}, I_{CC5(AV)} and I_{CC6(AV)} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1(AV)} and I_{CC5(AV)} are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _I = V _{SS} f = 1MHz V _I = 25mVrms			55	pF
C _{I(DQ)}	Data input/data output capacitance				17	pF
C _{I(W)}	Input capacitance, write control input				70	pF
C _{I(RAS)}	Input capacitance, R _{AS} input				70	pF
C _{I(CAS)}	Input capacitance, C _{AS} input				70	pF

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SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter	Limits						Unit
		MH2M04B1-7		MH2M04B1-8		MH2M04B1-10		
		Min	Max	Min	Max	Min	Max	
t _{CAC}	Access time from \overline{CAS} (Note 6, 7)		20		20		25	ns
t _{RAC}	Access time from \overline{RAS} (Note 6, 8)		70		80		100	ns
t _{NAC}	Access time from \overline{CAS} (Nibble mode) (Note 6, 9)		20		20		25	ns
t _{CAA}	Column address access time (Note 6, 10)		35		40		50	ns
t _{CLZ}	Output low impedance time from \overline{CAS} low (Note 6)	5		5		5		ns
t _{OFF}	Output disable time after \overline{CAS} high (Note 11)	0	20	0	20	0	25	ns

- Note 5: An initial pause of 500 μ s is required after power-up followed by any 8 \overline{RAS} or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
 Note that \overline{RAS} may be cycled during the initial pause. And any 8 \overline{RAS} or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of \overline{RAS} inactivity before proper device operation is achieved.
 6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
 7: Assume that t_{RCD} ≥ t_{RCD(max)} and t_{RAD(max)} ≥ t_{RAD}.
 8: Assume that t_{RCD} ≤ t_{RCD(max)} and t_{RAD} ≤ t_{RAD(max)}.
 9: Assume that \overline{CAS} access time at the 2nd, 3rd and 4th \overline{CAS} cycles on nibble mode.
 10: Assume that t_{RCD} - t_{RAD} ≤ t_{CAA(max)} - t_{CAC(max)} and t_{RCD} ≥ t_{RCD(max)}.
 11: t_{OFF(max)} defines the time at which the output achieves the high impedance state (I_{OUT} ≤ ±10 μ A) and is not reference to V_{OH(min)} or V_{OL(max)}.

TIMING REQUIREMENTS (For Read, Write, Refresh, and Nibble Mode Cycles)

(T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		MH2M04B1-7		MH2M04B1-8		MH2M04B1-10		
		Min	Max	Min	Max	Min	Max	
t _{REF}	Refresh cycle time		8		8		8	ms
t _{RP}	\overline{RAS} high pulse width	60		70		80		ns
t _{RCD}	Delay time, \overline{RAS} low to \overline{CAS} low (Note 14)	20	50	25	60	25	75	ns
t _{CRP}	Delay time, \overline{CAS} high to \overline{RAS} low (Note 15)	10		10		10		ns
t _{CPN}	\overline{CAS} high pulse width (Note 16)	30		35		35		ns
t _{RAD}	Column address delay time from \overline{RAS} low (Note 17)	15	35	20	40	20	50	ns
t _{ASR}	Row address setup time before \overline{RAS} low	0		0		0		ns
t _{ASC}	Column address setup time before \overline{CAS} low (Note 18)	0	10	0	15	0	20	ns
t _{RAH}	Row address hold time after \overline{RAS} low	10		15		15		ns
t _{CAH}	Column address hold time after \overline{CAS} low	15		20		20		ns
t _T	Transition time (Note 19)	3	50	3	50	3	50	ns

- Note 12: The timing requirements are assumed t_T = 5 ns.
 13: V_{IH(min)} and V_{IL(max)} are reference levels for measuring timing of input signals.
 14: t_{RCD(max)} is specified as a reference point only. If t_{RCD} is less than t_{RCD(max)}, access time is t_{RAC}. If t_{RCD} is greater than t_{RCD(max)}, access time is defined as t_{CAC} and t_{CAA} as shown in notes 7, 10.
 15: t_{CRP} requirement is applicable for All $\overline{RAS}/\overline{CAS}$ cycles.
 16: t_{CPN(min)} is specified as t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} except for t_{NCP} of Nibble mode cycle.
 17: t_{RAD(max)} is specified as a reference point only. If t_{RAD} ≥ t_{RAD(max)}, access time is assumed by t_{CAA} for read cycle.
 18: t_{ASC(max)} is specified as a reference point only of address access time.
 19: t_T is measured between V_{IH(min)} and V_{IL(max)}.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH2M04B1-7		MH2M04B1-8		MH2M04B1-10		
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read cycle time	140		160		190		ns
t _{RAS}	\overline{RAS} low pulse width	70	10000	80	10000	100	10000	ns
t _{CAS}	\overline{CAS} low pulse width	20	10000	20	10000	25	10000	ns
t _{CSH}	\overline{CAS} hold time after \overline{RAS} low	70		80		100		ns
t _{RSH}	\overline{RAS} hold time after \overline{CAS} low	20		20		25		ns
t _{RCS}	Read setup time before \overline{CAS} low	0		0		0		ns
t _{RCH}	Read hold time after \overline{CAS} high (Note 20)	0		0		0		ns
t _{RRH}	Read hold time after \overline{RAS} high (Note 20)	10		10		10		ns
t _{RAL}	Column address to \overline{RAS} setup time	35		40		50		ns
t _{RPC}	Precharge to \overline{CAS} active time	0		0		0		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle

Symbol	Parameter	Limits						Unit	
		MH2M04B1-7		MH2M04B1-8		MH2M04B1-10			
		Min	Max	Min	Max	Min	Max		
t _{WC}	Write cycle time	140		160		190		ns	
t _{RAS}	RAS low pulse width	70	10000	80	10000	100	10000	ns	
t _{CAS}	CAS low pulse width	20	10000	20	10000	25	10000	ns	
t _{CSH}	CAS hold time after RAS low	70		80		100		ns	
t _{RSH}	RAS hold time after CAS low	20		20		25		ns	
t _{WCS}	Write setup time before CAS low	(Note 21) 0						0	ns
t _{WCH}	Write hold time after CAS low	15		15		20		ns	
t _{WP}	Write pulse width	15		15		20		ns	
t _{DS}	Data setup time	0		0		0		ns	
t _{DH}	Data hold time after CAS low	15		15		20		ns	

Note 21: When t_{WCS} < t_{WCS(min)}, Data input will contend with the data output because of the common I/O feature.

CAS before RAS Refresh Cycle (Note 22)

Symbol	Parameter	Limits						Unit
		MH2M04B1-7		MH2M04B1-8		MH2M04B1-10		
		Min	Max	Min	Max	Min	Max	
t _{CSR}	CAS setup time for CAS before RAS refresh	10		10		10		ns
t _{CHR}	CAS hold time for CAS before RAS refresh	15		15		20		ns
t _{RPC}	Precharge to CAS active time	0		0		0		ns

Note 22: Eight or more CAS before RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

Nibble Mode Cycle (Read, Write, Cycle)

Symbol	Parameter	Limits						Unit
		MH2M04B1-7		MH2M04B1-8		MH2M04B1-10		
		Min	Max	Min	Max	Min	Max	
t _{NC}	Nibble mode cycle time	40		40		45		ns
t _{NCAS}	Nibble mode CAS low pulse width	20	10000	20	10000	25	10000	ns
t _{NCP}	Nibble mode CAS precharge time	10		10		10		ns
t _{NRSH}	Nibble mode RAS hold time	20		20		25		ns
t _{NWCS}	Nibble mode Write setup time before CAS	0		0		0		ns
t _{NWCH}	Nibble mode Write hold time after CAS	15		15		20		ns

Nibble-Mode Addressing Sequence Example

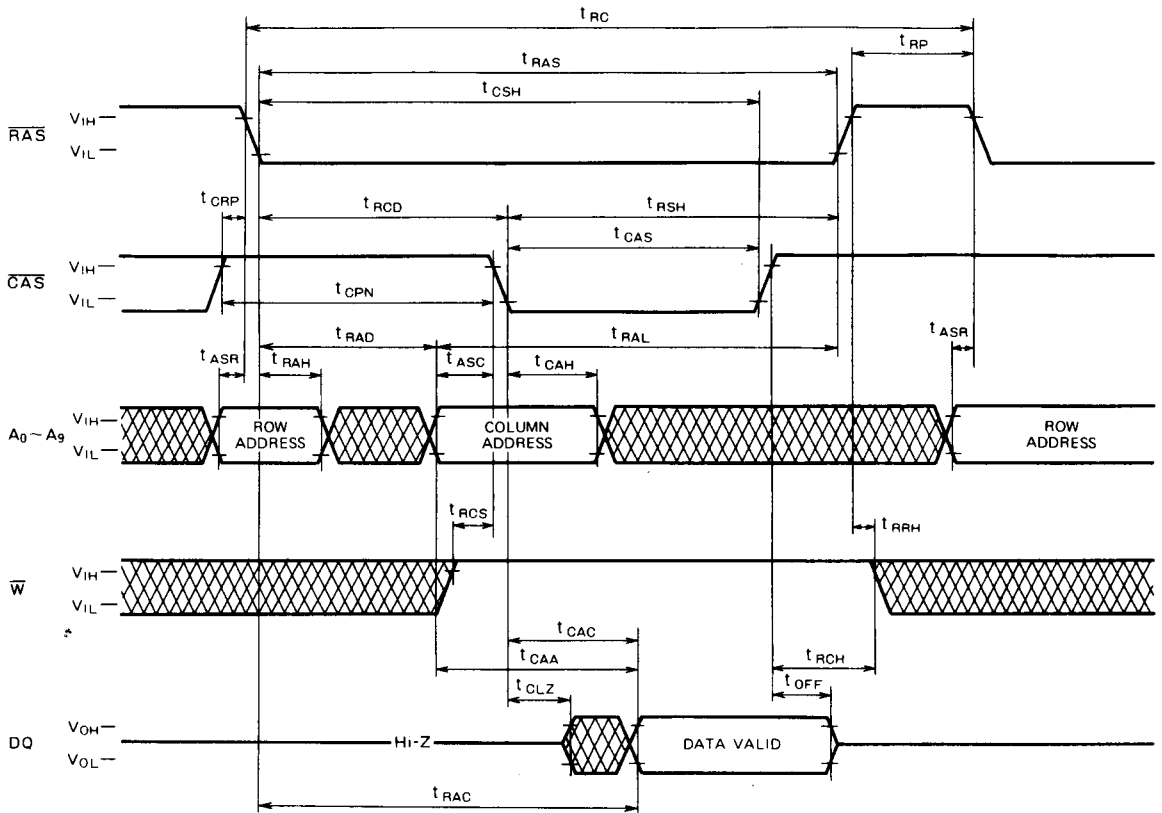
Sequence	Nibble bit	Column address										Row address										
		A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	
RAS/CAS	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	External address
toggle CAS	2	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	1	
toggle CAS	3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	Internally generated address
toggle CAS	4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
toggle CAS	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	

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Timing Diagrams (Note 23)

Read Cycle

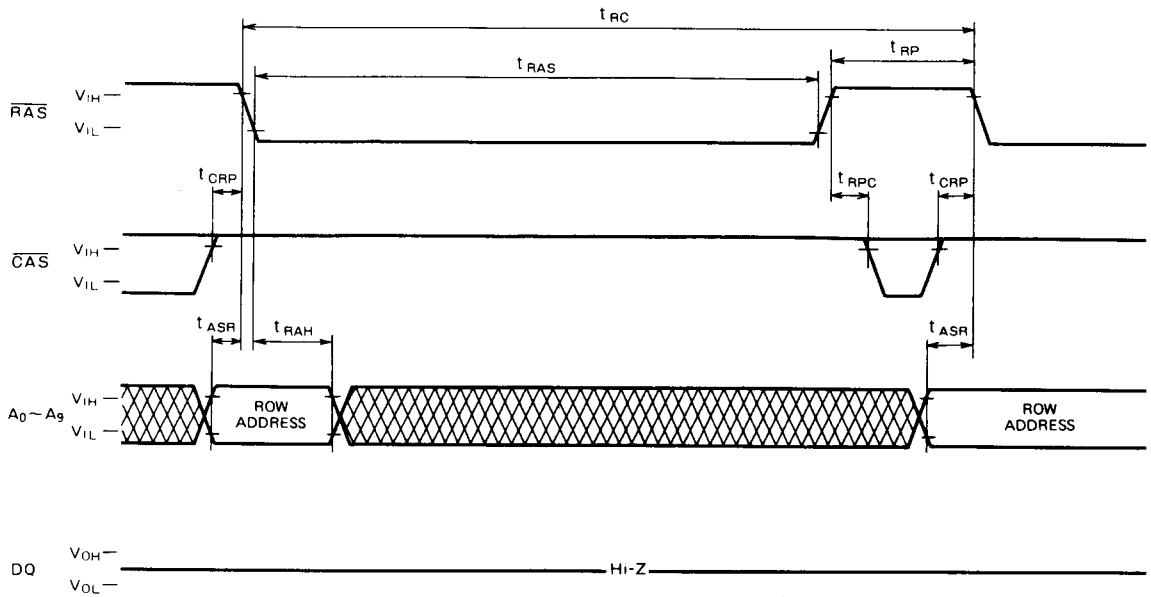


Note 23  Indicates the don't care input.

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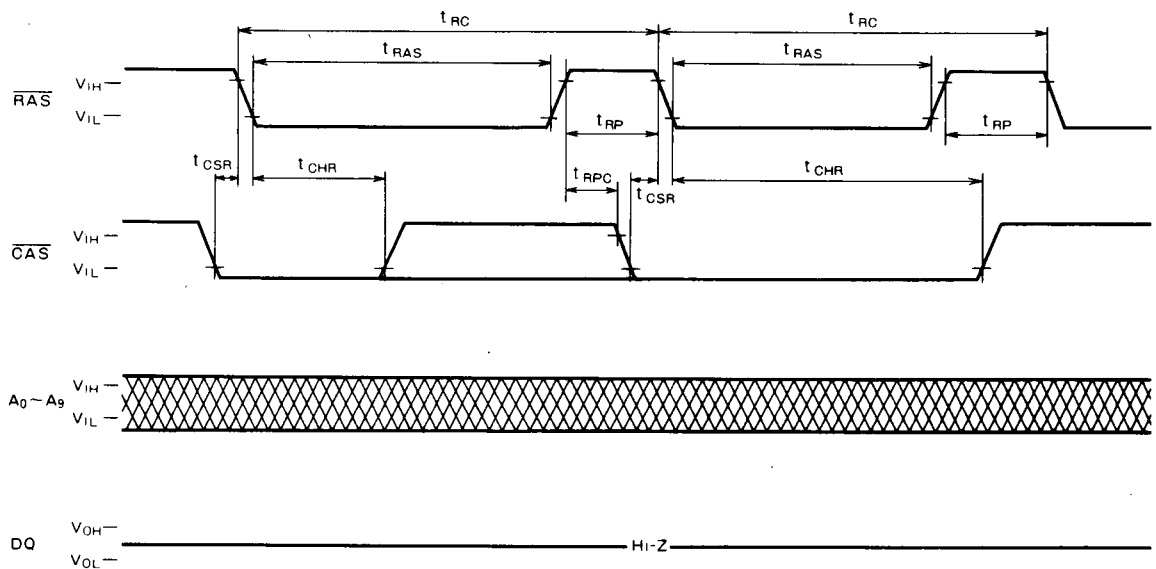
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RAS only Refresh Cycle (Note 24)



Note 24: \bar{W} = don't care, A₉ may be V_{IH} or V_{IL}

CAS before RAS Refresh Cycle (Note 25)

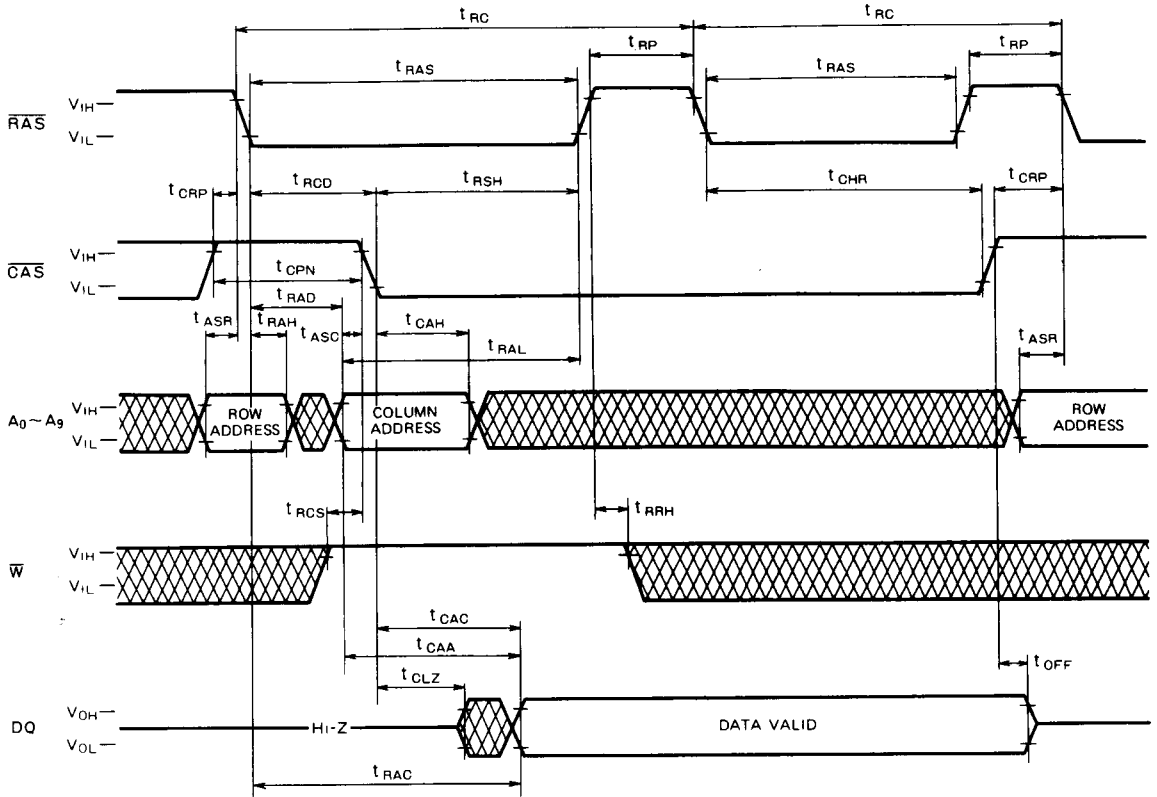


Note 25: \bar{W} = don't care

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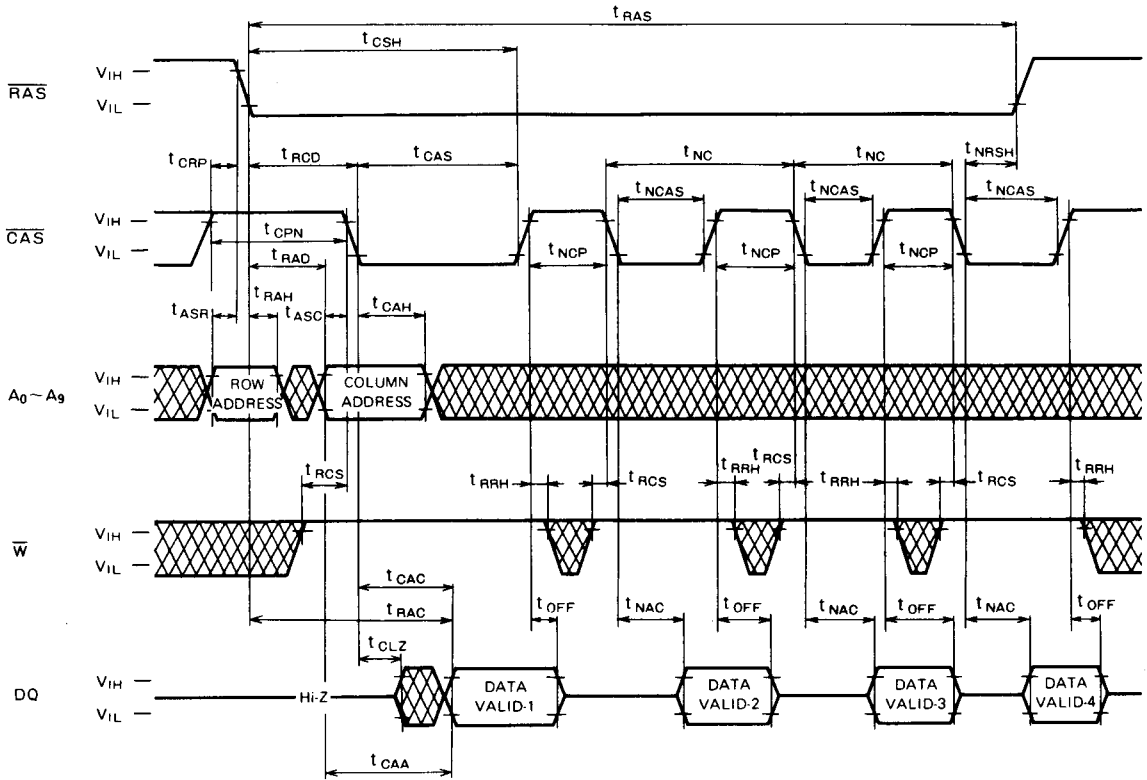
Hidden Refresh Cycle



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Nibble Mode Read Cycle



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Nibble Mode Write Cycle (Early Write)

