

TSLIC-E

Twin Subscriber Line Interface
Circuit Enhanced Feature Set
PEB 4365 Version 1.2

Wired
Communications



Never stop thinking.

TSLIC-E

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Preface

This document describes the Twin High Voltage Subscriber Line Interface Circuit PEB 4365 (TSLIC-E) which is part of the DuSLIC and VINETIC chip set family. For more DuSLIC related documents please see our webpage at <http://www.infineon.com/duslic>.

As the two channels of the TSLIC-E are identical, channel independent pin names are used throughout the document (for example "TIP" in place of "TIPA/TIPB"). Channel related pin names are only used for the pin description and specific figures.

Organization of this Document

This Preliminary Data Sheet is divided into six chapters. It is organized as follows:

- **Chapter 1, Overview**
A general description of the product, its key features, and pin configuration.
- **Chapter 2, Functional Description**
The main functions and operating modes are presented.
- **Chapter 3, Typical Application Circuit for DuSLIC and VINETIC**
Application circuit including bill of material and protection.
- **Chapter 4, Electrical Characteristics**
Parameters, symbols and limit values.
- **Chapter 5, Test Figures**
Test figures including external components.
- **Chapter 6, Package Outlines**
Illustrations and dimensions of the package outlines.

1 Overview

The Twin High Voltage Subscriber Line Interface Circuit PEB 4365 (TSLIC-E) is a reliable two channel interface between the telephone line and the codec devices of the DuSLIC or VINETIC chip sets. It is fabricated using Infineon Technologies' well-proven Smart Power Technology SPT 170.

The PEB 4365 provides battery feeding between -15 V and -85 V and internal balanced ringing up to 85 V_{rms} . In order to achieve this, an auxiliary positive battery voltage is used during ringing to enhance the useable voltage range to 150 V .

The TSLIC-E is designed for a voltage-feeding/current-sensing line interface concept and senses the transversal and longitudinal current.

To minimize system power dissipation, a power-down mode can be used; the TSLIC-E is switched off and the line outputs go to a high-impedance mode. Off-hook supervision is provided by activating a simple line current sensor with negligible power consumption.

For saving power in active mode an integrated switch enables the use of a lower battery voltage in short loop applications.

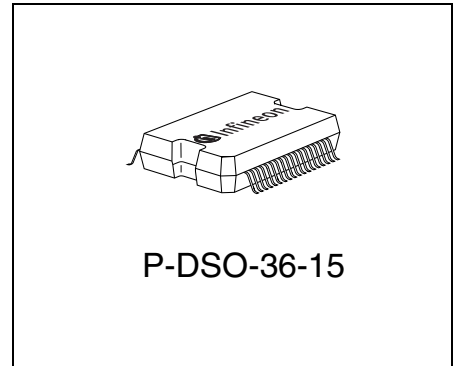
PEB 4365
Twin Subscriber Line Interface Circuit
Enhanced Feature Set

TSLIC-E

Version 1.2

1.1 Features

- Two channels
- High-voltage line feeding
- Two Battery voltages (–15 V ... –85 V)
- Total supply voltage of up to 150 V
- Long loop driving capability
- Integrated balanced ringing up to 85 Vrms
- Power-saving active mode (ACTL) with reduced battery voltage
- Sensing of transversal and longitudinal line currents
- Small P-DSO-36-15 package
- Reliable Smart Power Technology (SPT170)
- Enables high packing densities on board



Type	Package
TSLIC-E	P-DSO-36-15

1.2 Logic Symbol

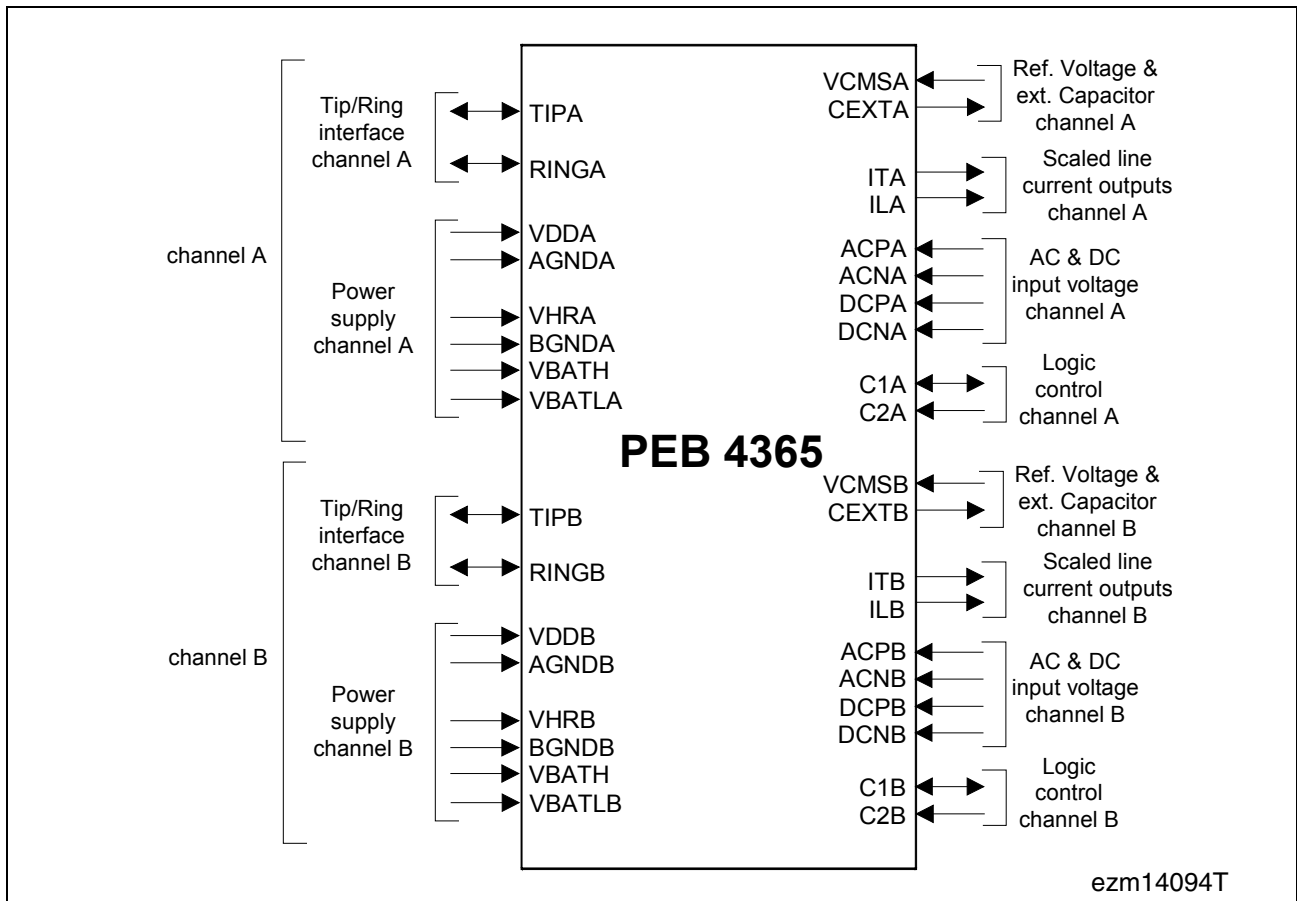


Figure 1 Logic Symbol

1.3 Pin Configuration

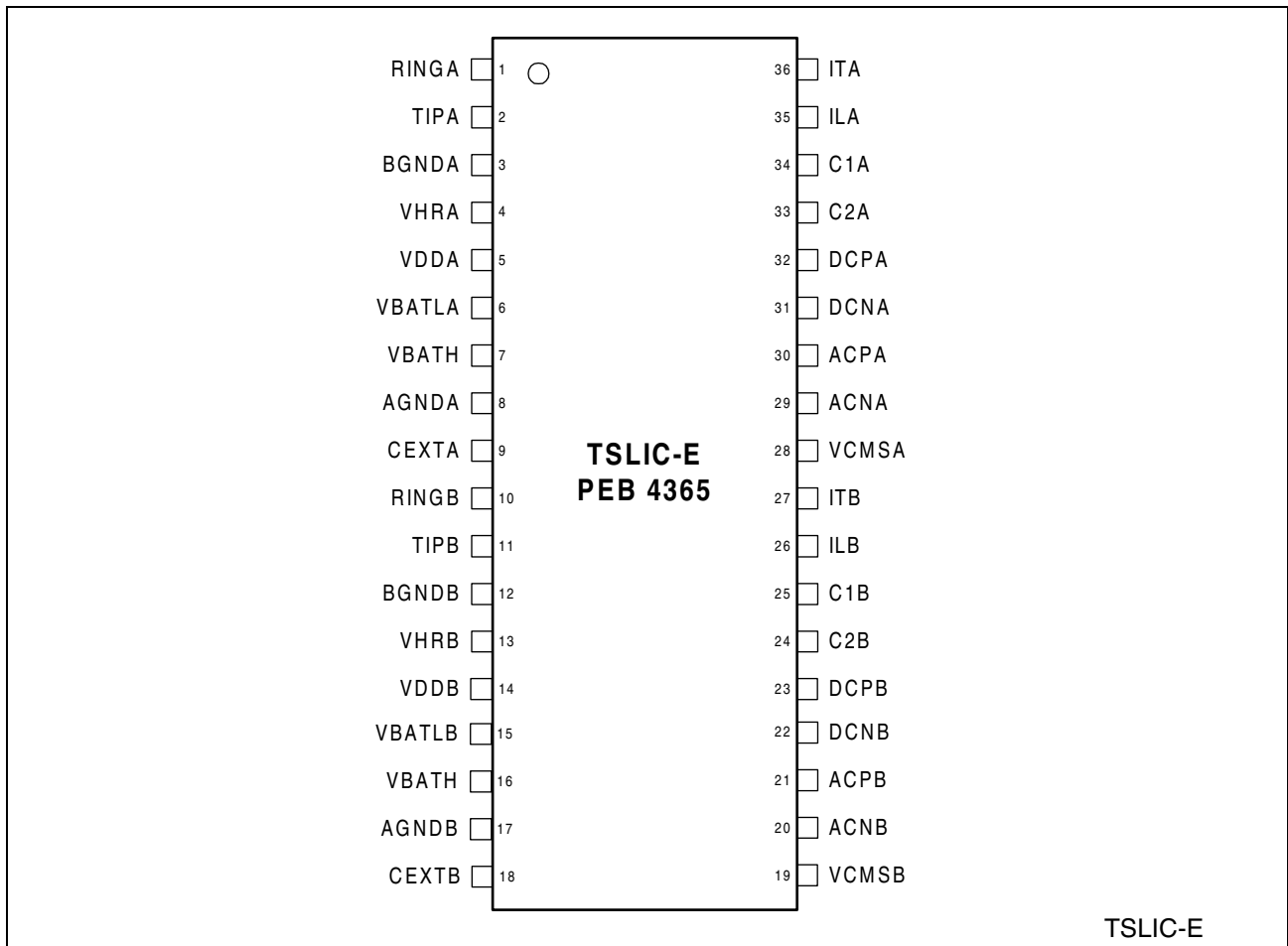


Figure 2 Pin Configuration (top view)

Attention: The heatslug (see [Figure 19](#)) is connected to VBATH via the chip substrate. Due to the high voltages of up to 150 V between VHRA (VHRB) and VBATH, touching of the heatslug or any attached conducting part can be hazardous.

1.4 Pin Definitions and Functions

Table 1 Pin Definitions and Functions TSLIC-E

Pin No.	Symbol	Input (I) Output (O)	Function
1 10	RINGA RINGB	I/O	Subscriber loop connection RING.
2 11	TIPA TIPB	I/O	Subscriber loop connection TIP.
3 12	BGNDA BGND B	Power	Battery ground: TIP, RING, V_{BATH} , V_{BATL} and V_{HR} refer to this pin.
4 13	VHRA VHRB	Power	Auxiliary positive battery supply voltage ($5\text{ V} \leq V_{HR} \leq 85\text{ V}$) used in ringing mode.
5 14	VDDA VDD B	Power	Positive supply voltage (+5 V), referred to AGND.
6 15	VBATLA VBATLB	Power	Negative battery supply voltage ($-15\text{ V} \geq V_{BATL} \geq V_{BATH}$)
7 16	VBATH	Power	Most negative battery supply voltage ($-20\text{ V} \geq V_{BATH} \geq -85\text{ V}$). Same pin name for both channels due to connection via substrate. An external connection via PCB is required!!
8 17	AGNDA AGND B	Power	Analog ground: V_{DD} , and all signal and control pins with the exception of TIP and RING refer to AGND.
9 18	CEXTA CEXT B	O	Output of voltage divider defining DC line potentials; an external capacitance allows supply voltage filtering (output resistance 50 k Ω).
28 19	VCMSA VCMS B	I	Reference voltage for differential two wire interface of typically 1.5 V.
29, 30	ACNA, ACPA	I	Differential two-wire AC input voltage; multiplied by -6 and related to $(V_{HI} + V_{BI})/2^1$, ACN appears at TIP and ACP at RING output, respectively.
20, 21	ACNB, ACPB		

Table 1 Pin Definitions and Functions TSLIC-E (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
31, 32	DCNA, DCPA	I	Differential two-wire DC input voltage; multiplied by -30 (ACTH and ACTL mode) or -60 (ACTR mode) and related to $(V_{HI} + V_{BI})/2$, DCN appears at TIP and DCP at RING output, respectively.
22, 23	DCNB, DCPB		
33 24	C2A C2B	I	Ternary logic input, controlling the operation mode.
34 25	C1A C1B	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding $165\text{ }^{\circ}\text{C}$) this pin sinks a current of typically $150\text{ }\mu\text{A}$.
35 26	ILA ILB	O	Current output: longitudinal line current scaled down by a factor of 100.
36 27	ITA ITB	O	Current output representing the transversal current scaled down by a factor of 50.

¹⁾ V_{HI} is the output voltage of the positive battery switch,
 V_{BI} is the output voltage of the negative battery switch (see [Figure 3](#)).

1.5 Functional Block Diagram

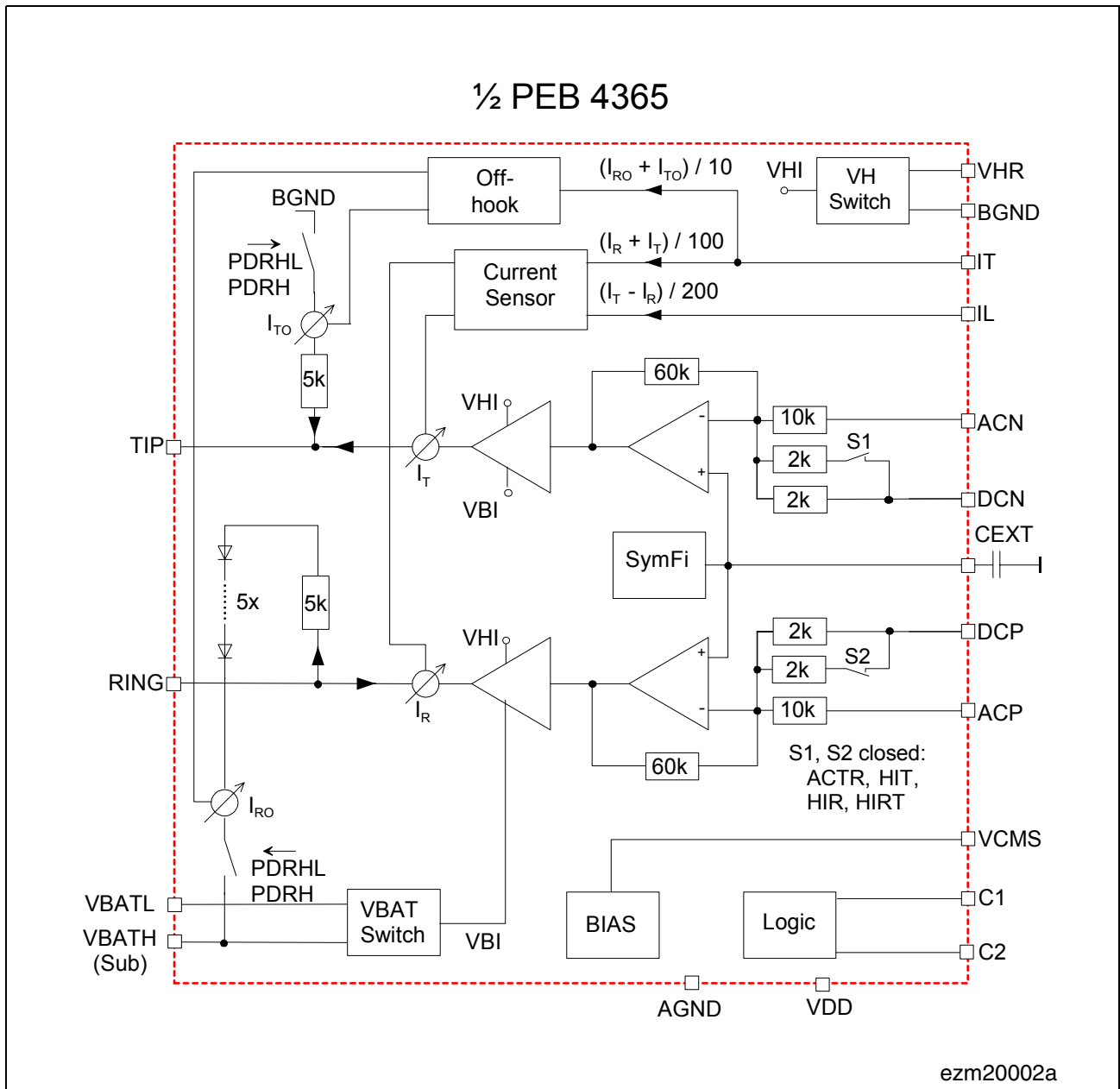


Figure 3 Block Diagram (one Channel)

Note: As the two channels of the TSLIC-E are identical, channel independent pin names are used throughout the document (for example “TIP” in place of “TIPA/TIPB”). Channel related pin names are only used for the pin description and specific figures.

2 Functional Description

The PEB 4365 supports AC and DC control loops for each channel based on feeding a voltage V_{TR} to the line and sensing the transversal line current I_{Trans} and the longitudinal current I_{Long} (Figure 4).

In receive direction DC and AC voltages are handled separately with different gains on the PEB 4365. Both are applied differentially via pins DCP and DCN or ACP and ACN, respectively.

The line voltages V_R and V_T are the amplified input voltages, related to the mean supply voltage $V_M = (V_{HI} + V_{BI})/2$. Depending on the operation mode, V_{HI} is switched either to V_{HR} or to BGND via the VH switch and V_{BI} is switched either to V_{BATL} or to V_{BATH} via the VBAT switch (see Figure 3).

In the active modes ACTH with $V_M = V_{BATH}/2$ and ACTL with $V_M = V_{BATL}/2$, the line voltages are given by

$$V_T = V_{TIP} = V_M - 30 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$

$$V_R = V_{RING} = V_M - 30 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS}),$$

while in ringing mode ACTR with $V_M = [V_{HR} + V_{BATH}]/2$,

$$V_T = V_{TIP} = V_M - 60 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$

$$V_R = V_{RING} = V_M - 60 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS})$$

The transversal line voltage $V_{TR} = V_T - V_R$ is simply related to the input voltages:

$$V_{TR} = V_{TIP} - V_{RING} = V_{ab} =$$

$$= 30 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN}) \quad \text{for modes ACTH, ACTL}$$

$$= 60 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN}) \quad \text{for mode ACTR}$$

A reversed polarity of V_{TR} is easily obtained by changing the sign of $(V_{DCP} - V_{DCN})$.

Functional Description

In transmit direction the transversal and longitudinal currents are measured and scaled images are provided at the IT and IL pin, respectively:

$I_{IT} = (I_T + I_R)/100 = I_{Trans}/50$	$I_{IL} = (I_T - I_R)/200 = I_{Long}/100$
$I_{Trans} = (I_T + I_R)/2$	$I_{Long} = (I_T - I_R)/2$

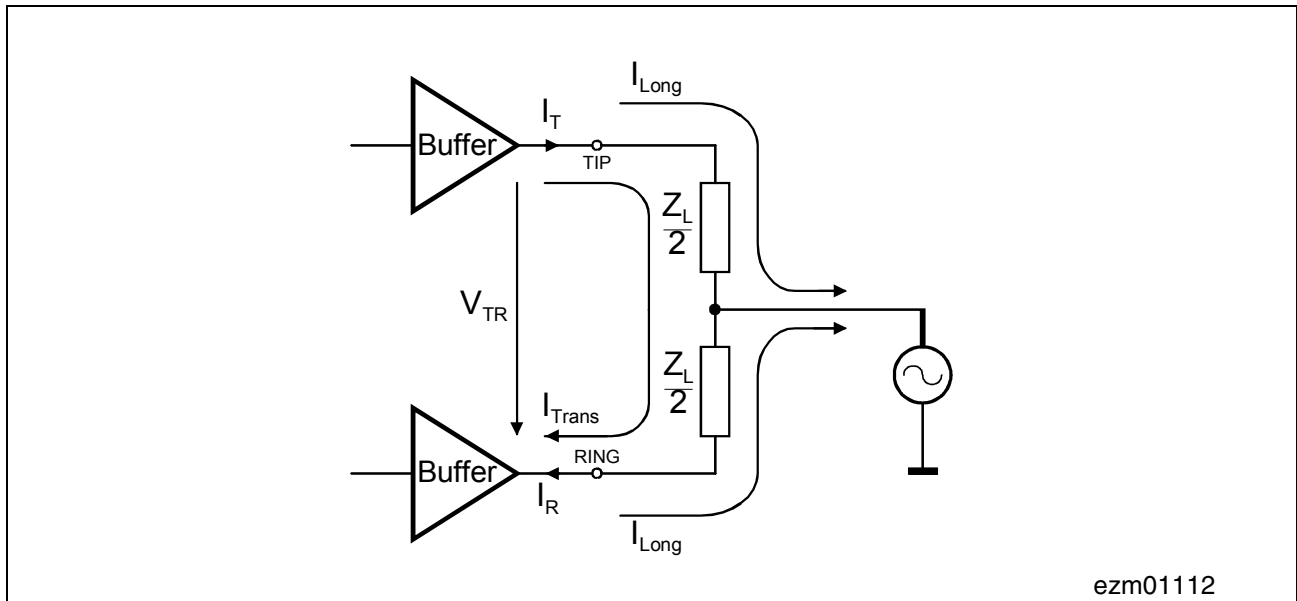


Figure 4 Definition of Output Current Directions

For off-hook detection, in PDRH (and PDRHL) mode 5 kΩ resistors are connected from TIP to BGND and from RING to VBATH, respectively.

The currents through these resistors, I_{T0} and I_{R0} are sensed, scaled and provided at the IT pin (see [Figure 3](#)):

$$I_{IT0} = (I_{T0} + I_{R0})/10 = I_{TRANS0}/5$$

The TSLIC-E consists of two SLICs, which can be operated completely independent. Also the supply voltages V_{HR} and V_{BATL} of each of the SLICs can be chosen independently from each other. That means V_{HRA} and V_{BATLA} might be different from V_{HRB} and V_{BATLB} .

Caution: V_{BATH} supply voltage has to be the same for both SLIC channels. All VBATH pins of TSLIC-E must be connected externally.

2.1 Operating Modes

Each channel of the PEB 4365 (TSLIC-E) operates in one of the following modes controlled by ternary logic signals at the respective C1 and C2 input pins:

Table 2 TSLIC-E Interface Code

		C2 ¹⁾		
		L	M	H
C1 ¹⁾	L ²⁾	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

¹⁾ As the two channels of the TSLIC-E are identical, channel independent pin names are used throughout the document (for example “C1” in place of “C1A/C1B”). Channel related pin names are only used for the pin description and specific figures.

²⁾ No ‘Overtemp’ signaling possible via pin C1 if C1 is low.

The operating modes of channels A and B can be chosen completely independent. Any combination is allowed; thermal restrictions (max. chip temperature), however, have to be obeyed.

Table 3 TSLIC-E Modes

TSLIC-E Mode	Mode Description	Internal Supply Voltages V_{BI} , V_{HI}
PDH	Power Down High Impedance	supply switches open
PDRH	Power Down Resistive High	supply switches open
PDRHL	Power Down Resistive High Load	supply switches open
ACTL	Active Low	V_{BATL} , BGND
ACTH	Active High	V_{BATH} , BGND
ACTR	Active Ring	V_{BATH} , V_{HR}
HIRT	High Impedance on RING and TIP	V_{BATH} , V_{HR}
HIT	High Impedance on TIP	V_{BATH} , V_{HR}
HIR	High Impedance on RING	V_{BATH} , V_{HR}

Power Down High Impedance (PDH)

PDH offers high impedance at TIP and RING; it can be used for testing purposes or when an error condition occurs. In PDH mode all functions are switched off. Off-hook detection is not available.

Power Down Resistive High (PDRH)

Power consumption is reduced to a minimum by switching completely off all voice transmission functions. To allow off-hook detection, PDRH provides a connection of 5 k Ω each from TIP to BGND and RING to VBATH, respectively, while the output buffers show high impedance (see [Figure 3](#)). The current through these resistors is sensed and transferred to the IT pin for off-hook supervision.

Power Down Resistive High Load (PDRHL)

PDRHL is used as a transition state at a mode change from PDRH or PDH to ACTH mode (automatically initiated by the codec device at a mode change). It causes fast preloading of C_{EXT} in order to suppress line voltage transients.

Active Low (ACTL), Active High (ACTH)

These are the regular transmission modes for voiceband. The line-driving section is operated between V_{BATL} or V_{BATH} and BGND.

Active Ring (ACTR)

Utilizing an additional positive battery voltage V_{HR} , this mode allows balanced ringing of up to 85 Vrms or feeding of very long telephone lines.

High Impedance (HIR, HIT, HIRT)

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer can still be measured by IT or IL. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes).

2.2 Current Limitation / Overtemperature

In any operating mode (except Power Down) the total current delivered by the output drivers is limited to approximately 100 mA.

If, however, the junction temperature exceeds 165 °C, the current limit is further reduced to keep the junction temperature constant.

Simultaneously, pin C1 sinks a signalling current I_{therm} . As both TSLIC-E channels are thermally coupled, an overtemperature condition may be indicated on both channels.

Typical Application Circuit for DuSLIC and VINETIC

3 Typical Application Circuit for DuSLIC and VINETIC

Figure 5 (Figure 6) shows one channel of an application circuit including a TSLIC-E and a SLICOFI-2/-2S or VINETIC-4VIP/-4M/-8M chip (for latest information please refer to the DuSLIC or VINETIC Data Sheet). Pins of an unused channel of TSLIC-E can be left open. **Table 4** shows the external passive components needed for a dual-channel solution as shown in **Figure 5** and **Figure 6**.

Table 4 External Components DuSLIC / VINETIC for 2 Channels

No.	Symbol	Value	Unit	Relat. Tol.	Rating	DuSLIC Systems	VINETIC Systems
2	R_{IT1}	470	Ω	1 %		x	
2	R_{IT1}	510	Ω	1 %			x
2	R_{IT2}	680	Ω	1 %		x	x
2	R_{IL}	1.6	k Ω	1 %		x	x
4	R_{STAB}	30	Ω	1 % ¹⁾		x	x
4	R_{PROT} ²⁾	20 ... 50	Ω	1 % ¹⁾		x	x
4	C_{STAB}	15 (typ.)	nF	10 %	100 V	x	x
2	C_{DC}	120	nF	10 %	10 V	x	
2	C_{DC}	220	nF	10 %	10 V		x
2	C_{ITAC}	680	nF	10 %	10 V	x	
2	C_{ITAC}	1	μ F	10 %	10 V		x
1	C_{PRE} ³⁾	18	nF	5 %	10 V		x
2	C_{VCMIT}	680	nF	10 %	10 V	x	
1	C_{REF}	68	nF	20 %	10 V	x	x
2	C_{EXT}	470	nF	20 %	10 V	x	x
7	C_1	typ. 100	nF	10 %	10 V	x	
13	C_1	typ. 100	nF	10 %	10 V		x
6	C_2	typ. 100	nF	10 %	100 V	x	x
1	C_3	4.7	μ F	20 %	10 V, Tantal	x	
2	D_1	BAS 21	–	–	–	x	x
4	D_2	BAS 21	–	–	–	x	x
2	U_1 ²⁾	Overtoltage Protection Element	–	–	–	x	x

¹⁾ Matching tolerance dependent on longitudinal balance requirements (for details see the Application Note *External Components*).

Typical Application Circuit for DuSLIC and VINETIC

- 2) See Application Note *Protection of DuSLIC / VINETIC Linecard Chip Sets against Overvoltages and Overcurrents*.
- 3) C_{PRE} is only necessary when TTX (12 or 16 kHz metering) is used.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Battery voltage low	V_{BATL}	-85	0.4	V	Referred to BGND
Battery voltage high	V_{BATH}	-90	0.4	V	Referred to BGND
Battery voltage difference	$V_{\text{BATL}} - V_{\text{BATH}}$	-0.4	-	V	-
Auxiliary supply voltage	V_{HR}	-0.4	90	V	Referred to BGND
Total battery supply voltage, continuous	$V_{\text{HR}} - V_{\text{BATH}}$	-	160	V	-
V_{DD} supply voltage	V_{DD}	-0.4	7	V	Referred to AGND
Ground voltage difference BGND, AGND	-	-0.4	0.4	V	-
Input voltages	$V_{\text{DCP}}, V_{\text{DCN}}, V_{\text{ACP}}, V_{\text{ACN}}, V_{\text{C1}}, V_{\text{C2}}, V_{\text{CMS}}$	-0.4	$V_{\text{DD}} + 0.4$	V	Referred to AGND
Voltages on current outputs	$V_{\text{IT}}, V_{\text{IL}}$	-0.4	$V_{\text{DD}} + 0.4$	V	Referred to AGND
Junction temperature	T_{j}	-	150	°C	
ESD voltage, all pins	-	-	1	kV	SDM (Socketed Device Model) ¹⁾

¹⁾ EOS/ESD Assn. Standard DS5.3-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.

4.2 Foreign Line Voltages

External voltages applied at the line outputs cause a current flow in the TSLIC-E. The resulting on-chip power dissipation has to be limited to avoid thermal destruction, because overtemperature protection cannot react fast enough at high local power density. The value of allowed power dissipation strongly depends on its duration. It can be expressed in terms of voltage and current limits directly at the TIP/RING outputs.

Table 6 Voltage Limits on Output Pins

Duration of Voltage	pins	min. Voltage [V]	max. Voltage [V]
continuous	TIP, RING	$V_{BATH} - 0.4$	$V_{HR} + 5$
< 10 ms	TIP, RING	$V_{BATH} - 5$	$V_{HR} + 10$
< 100 μ s	TIP, RING	$V_{BATH} - 10$	$V_{HR} + 20$
< 1 μ s	TIP, RING	$V_{BATH} - 15$	$V_{HR} + 40$

Table 7 Current Limits on Output Pins

Duration of Current	pins	min. current [A]	max. current[A]
continuous	TIP, RING	- 0.1	0.1
< 10 ms	TIP, RING	- 0.5	0.5
< 100 μ s	TIP, RING	- 1	1.0
< 1 μ s	TIP, RING	- 1.5	1.5

The above limitations ([Table 6](#) and [Table 7](#)) have to be regarded as typical. They are valid simultaneously. Together with external circuitry they determine protection requirements (see Application Note of the DuSLIC/VINETIC chip set on overvoltages and overcurrents).

4.3 Power Up Sequence of Supply Voltages

It is recommended to apply the TSLIC-E supply voltages for each channel in the following order to the respective pins:

- 1) AGND, BGND
- 2) V_{DD}
- 3) V_{BATH}
- 4) V_{HR}
- 5) V_{BATL}

When powering down the TSLIC-E, the supply voltages have to be removed in reverse order.

With the use of the diodes D_1 and D_2 (see application circuits [Figure 5](#) and [Figure 6](#)) it is not necessary to keep the recommended power up sequence.

4.4 Operating Range

Table 8 Operating Range

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Battery voltage L ¹⁾	V_{BATL}	-80	-15	V	Referred to BGND
Battery voltage H ¹⁾	V_{BATH}	-85	-20	V	Referred to BGND
Auxiliary supply voltage	V_{HR}	5	85	V	Referred to BGND
Total battery supply voltage	$V_{HR} - V_{BATH}$	-	150	V	-
V_{DD} supply voltage	V_{DD}	4.75	5.25	V	Referred to AGND
Ground voltage difference BGND, AGND	-	-0.4	0.4	V	-
Voltage at pins IT, IL	V_{IT}, V_{IL}	-0.4	3.5	V	Referred to AGND
Input range $V_{DCP}, V_{DCN},$ V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	-40	85	°C	-
Junction temperature	T_J	-	125 ²⁾	°C	-

¹⁾ If the battery switch is not used, pins VBATL and VBATH should be connected externally. In this case the full voltage range of -15 V to -85 V can be used.

²⁾ Operation up to $T_J = 150$ °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

4.5 Thermal Resistances

Table 9 Thermal Resistances

Parameter	Symbol	Typical Values	Unit	Condition
Junction to case	$R_{th, jC}$	2	K/W	P-DSO-36-15
Junction to ambient	$R_{th, jA}$	20	K/W	P-DSO-36-15, 4-layer PCB; die pad soldered to 20 x 20 mm ² cooling area (footprint see Chapter 6.1)

The allowed power dissipation can be calculated as:

$$P_{max} = P_A + P_B = (T_{j,max} - T_{amb})/R_{th,jA}$$

P_A ... Power Dissipation Channel A

P_B ... Power Dissipation Channel B

4.6 Electrical Parameters

Minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at $V_{BATH} = -48\text{ V}$, $V_{BATLA} = V_{BATLB} = -24\text{ V}$, $V_{HRA} = V_{HRB} = +32\text{ V}$ and $V_{DDA} = V_{ddb} = +5\text{ V}$.

Functionality and performance is guaranteed for $T_A = 0$ to 70 °C by production testing. Extended temperature range operation at $-40\text{ °C} < T_A < 85\text{ °C}$ is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

The following specification is valid for only one channel. Both channels A and B have identical specifications.

4.6.1 Supply Currents and Power Dissipation (Values per Channel)

Table 10 Supply Currents, Power Dissipation ($I_R = I_T = 0\text{ A}$; $V_{RT} = 0\text{ V}$)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				Min.	Typ.	Max.	

Power Down High Impedance, Power Down Resistive High

1.	V_{DD} current	I_{DD}	PDH, PDRH	–	120	200	μA
2.	V_{BATH} current	I_{BATH}	PDH, PDRH	–	80	120	μA
3.	V_{BATL} current	I_{BATL}	PDH, PDRH	–	0	10	μA
4.	V_{HR} current	I_{HR}	PDH, PDRH	–	0	10	μA

Active Low

5.	V_{DD} current	I_{DD}	ACTL	–	0.9	1.2	mA
6.	V_{BATH} current	I_{BATH}	ACTL	–	20	40	μA
7.	V_{BATL} current ¹⁾	I_{BATL}	ACTL	–	2.5	3.3	mA
8.	V_{HR} current	I_{HR}	ACTL	–	0	10	μA

Active High

9.	V_{DD} current	I_{DD}	ACTH	–	1	1.3	mA
10.	V_{BATH} current ¹⁾	I_{BATH}	ACTH	–	3	4	mA
11.	V_{BATL} current	I_{BATL}	ACTH	–	0	10	μA
12.	V_{HR} current	I_{HR}	ACTH	–	0	10	μA

Electrical Characteristics
Table 10 Supply Currents, Power Dissipation ($I_R = I_T = 0$ A; $V_{RT} = 0$ V) (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				Min.	Typ.	Max.	

Active Ring

13.	V_{DD} current	I_{DD}	ACTR	–	0.5	0.7	mA
14.	V_{BATH} current ¹⁾	I_{BATH}	ACTR	–	2.8	3.7	mA
15.	V_{BATL} current	I_{BATL}	ACTR	–	0	10	μ A
16.	V_{HR} current ¹⁾	I_{HR}	ACTR	–	2.1	2.8	mA

High Impedance on RING, High Impedance on TIP

17.	V_{DD} current	I_{DD}	HIR, HIT	–	0.5	0.7	mA
18.	V_{BATH} current ¹⁾	I_{BATH}	HIR, HIT	–	1.9	2.5	mA
19.	V_{BATL} current	I_{BATL}	HIR, HIT	–	0	10	μ A
20.	V_{HR} current ¹⁾	I_{HR}	HIR, HIT	–	1.3	1.8	mA

High Impedance on RING and TIP

21.	V_{DD} current	I_{DD}	HIRT	–	0.5	0.7	mA
22.	V_{BATH} current ¹⁾	I_{BATH}	HIRT	–	1	1.4	mA
23.	V_{BATL} current	I_{BATL}	HIRT	–	0	10	μ A
24.	V_{HR} current ¹⁾	I_{HR}	HIRT	–	0.5	0.8	mA

¹⁾ Current depending on supply voltage (see [Table 11](#))

Electrical Characteristics

The total power dissipated in the SLIC consists of the quiescent power P_Q due to the supply currents and the output stage power P_O caused by any line current I_{TRANS} (see [Table 12](#)).

$$P_{tot} = P_Q + P_O$$

The **TSLIC-E**'s total power dissipation can be estimated by adding the power dissipated in channel A and channel B:

$$P_{tot} = P_{Q,A} + P_{Q,B} + P_{out,A} + P_{out,B}$$

with $P_Q = V_{DD} \times I_{DD} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL} + V_{HR} \times I_{HR}$

The supply currents I_{BATL} , I_{BATH} and I_{HR} are dependent on the respective supply voltages. They can be calculated from the specified values I_{BATL} (-24 V), I_{BATH} (-48 V) and I_{HR} (32 V) by the formulas in [Table 11](#).

Table 11 Voltage Dependence of Supply Currents

Operating Mode	Equation for I Calculation
ACTL	$I_{BATL}(V_{BATL}) = I_{BATL}(-24V) + (V_{BATL} - 24)/50 \text{ k}\Omega$
ACTH	$I_{BATH}(V_{BATH}) = I_{BATH}(-48V) + (V_{BATH} - 48)/50 \text{ k}\Omega$
ACTR ¹⁾	$I_{BATH}(V_{BATH}) = I_{BATH}(-48V) + (V_{BATH} - 48)/50 \text{ k}\Omega$ $I_{HR}(V_{HR}) = I_{HR}(32V) + (V_{HR} - 32)/200 \text{ k}\Omega$

¹⁾ valid for $|V_{BATH}| > V_{HR}$

Table 12 Output Stage Power Dissipation

Operating Mode	Equation for P_O Calculation
ACTL	$P_O = (1.05 \times V_{BATL} - V_{TR}) \times I_{Trans}$
ACTH	$P_O = (1.05 \times V_{BATH} - V_{TR}) \times I_{Trans}$
ACTR	$P_O = (1.02 \times V_{HR} + 1.05 \times V_{BATH} - V_{TR}) \times I_{Trans}$ (ohmic load) $P_O = [4 \times (V_H + V_{BATH}) - \pi \times V_P \times \cos \phi] \times V_P / (2 \times \pi \times Z_L)$ (complex load $Z = Z_L e^{i\phi}$, V_P ... peak ring voltage)

Electrical Characteristics

4.6.2 DC Characteristics

Table 13 DC Characteristics

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
25.	DC line voltage	$V_{TR, DC}$	ACTL, ACTH, ACTR	-0.4	0	0.4	V	$V_{DCP} = V_{DCN} = V_{ACP} =$ $V_{ACN} = 1.5 V$
26.		$V_{TIP, DC}$	ACTL	-13	-12	-11	V	
27.			ACTH	-25	-24	-23	V	
28.			ACTR	-10.5	-9.5	-8.5	V	
29.		$V_{TR, DC}$	ACTH	23.5	24	24.5	V	$V_{DCP} - V_{DCN} = 0.8 V,$ $V_{ACP} = V_{ACN} = 1.5 V$
30.				-24.5	-24	-23.5	V	$V_{DCP} - V_{DCN} = -0.8 V,$ $V_{ACP} = V_{ACN} = 1.5 V$
31.	DC line voltage drop (see Figure 7)	$-V_{BATH}$ $-V_{TR, max}$	ACTH	-	2	3	V	$I_{Trans, DC} = 20 mA,$ $V_{DCP} - V_{DCN} = 2.5 V,$ $V_{ACP} = V_{ACN} = 1.5 V$
32.	Output current limit (see Figure 11)	$ I_{R, max} ,$ $ I_{T, max} $	ACTL, ACTH, ACTR, HIR HIT	80		130	mA	
33.	Open loop resistance TIP to V_{BGND} (see Figure 12)	R_{TG}	PDRH	4.25	5.0	5.75	k Ω	$I_T = 2 mA,$ Temp = 25 °C ¹⁾
34.	Open loop resistance RING to V_{BATH} (see Figure 12)	R_{RB}	PDRH	4.25	5.0	5.75	k Ω	$I_R = 2 mA,$ Temp = 25 °C ¹⁾
35.	Open loop line voltage	V_{TR}	PDRH		45		V	
36.	Power down	$I_{Leak, R}$	PDH	-30		30	μA	$V_{BATH} < V_R < V_{HR}$
37.	output leakage current	$I_{Leak, T}$		-30		30	μA	$V_{BATH} < V_T < V_{HR}$

Electrical Characteristics

Table 13 DC Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
38.	High impedance	$I_{Leak,R}$	HIR, HIRT	-30		30	μA	$V_{BATH} < V_R < V_{HR} - 3$
39.	output leakage current	$I_{Leak,T}$	HIT, HIRT	-30		30	μA	$V_{BATH} < V_T < V_{HR} - 3$

Inputs DCP, DCN, ACP, ACN, Output C_{EXT}

40.	Input resistance DCP, DCN	R_{DC}	ACTR, HIR, HIT	-	1	-	k Ω	
41.			ACTL, ACTH	-	2	-	k Ω	
42.	Input resistance ACP, ACN	R_{AC}	all	-	10	-	k Ω	
43.	Output resistance on C _{EXT}		all	-	50	-	k Ω	

Current Outputs I_T, I_L

44.	IT output current (see Figure 13)	I_{IT}	ACTx	-15	0	15	μA	$I_R = I_T = 0 \text{ mA}$
45.				380	400	420	μA	$I_R = I_T = 20 \text{ mA}$
46.				-420	-400	-380	μA	$I_R = I_T = -20 \text{ mA}$
47.	Transversal current ratio (guaranteed by design, see Figure 13)	$I/G_{IT,DC}^{2)}$	ACTx	49.5	50	50.5	-	$I_R = I_T = 20 \text{ mA}, I_R = I_T = -20 \text{ mA}$
48.	Off-hook output current on IT		PDRH	750	800	1050	μA	TIP/RING shorted Temp = 25 °C ³⁾
49.	IL output current (see Figure 13)	I_{IL}	ACTx	-20	0	20	μA	$I_R = I_T = 20 \text{ mA}$
50.				30	50	70	μA	$I_R = 15 \text{ mA}, I_T = 25 \text{ mA}$
51.				-160	-125	-90	μA	$I_R = 62.5 \text{ mA}, I_T = 37.5 \text{ mA}$

Electrical Characteristics

Table 13 DC Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		

Control Inputs C1, C2

52.	H-input voltage	V_{IH}	–	2.7		$V_{DD} + 0.3$	V	–
53.	M-input voltage	V_{IM}	–	1.2		2.1	V	–
54.	L-input voltage	V_{IL}	–	–0.3		0.6	V	–
55.	Input leakage current	I_{Leak}	–	–5	0	5	μA	–
56.	Thermal overload current C1	I_{therm}	ACTx, Hlx	120	150	250	μA	$V_{C1} = 1.20 V$
57.	Max. junction temperature ⁴⁾	T_{jLIM}	ACTx, Hlx	–	165	–	$^{\circ}C$	–

- 1) The systematic temperature dependency of this resistance is $+0.1\%/^{\circ}C$.
- 2) The offset ($I_R = I_T = 0 mA$) has to be taken into account.
- 3) The systematic temperature dependency of this current is $-0.1\%/^{\circ}C$.
- 4) Overtemperature protection (guaranteed by design)

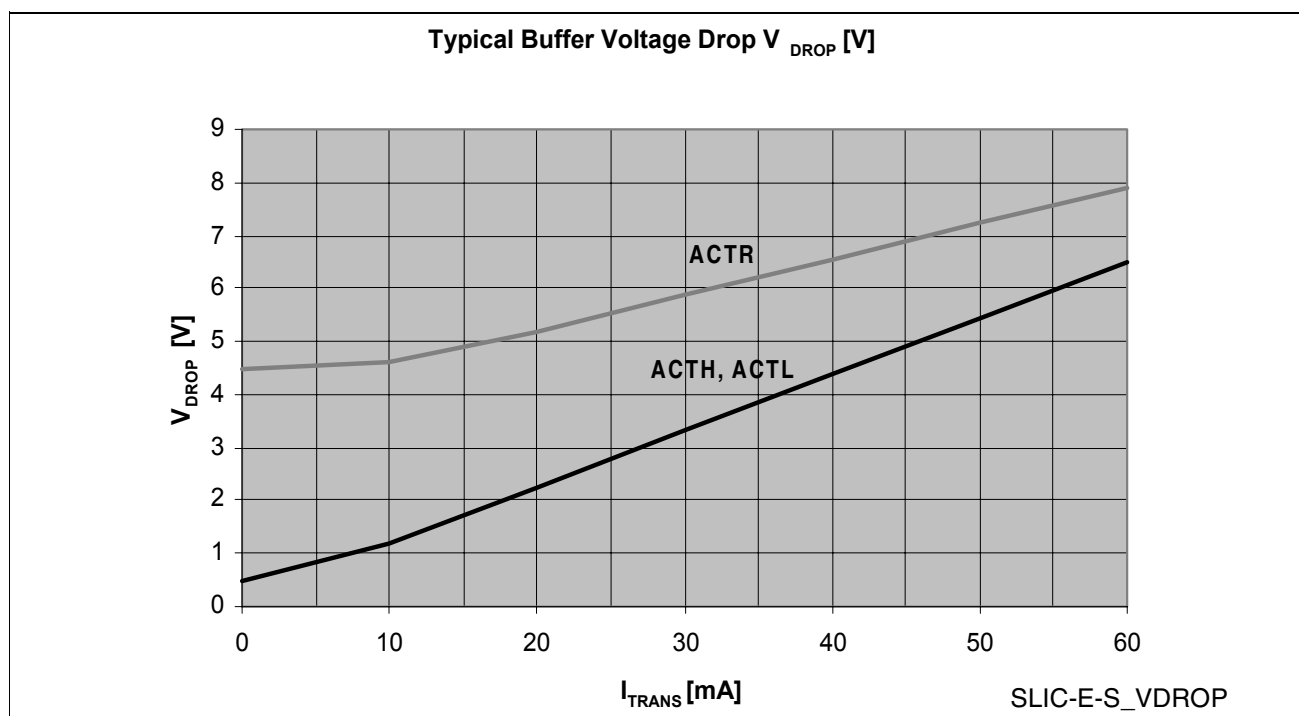


Figure 7 Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR

4.6.3 AC Characteristics

If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA and –25 mA, respectively; they are valid in all active modes.

Table 14 AC Characteristics

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		

Line Termination TIP, RING

58.	Receive gain (see Figure 14)	G_r		5.925	6.0	6.075	–	$V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$
59.	Total harmonic distortion V_{TR} (see Figure 14)	THD		–	0.03	0.3	%	$V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$
60.	Teletax distortion	THD_{TTX}		–	0.1	1	%	$V_{TR,AC} = 5 \text{ Vrms}$ $f = 16 \text{ kHz}, R_L = 200 \Omega$
61.				–	1	3	%	$V_{TR,AC} = 5 \text{ Vrms}$ $f = 16 \text{ kHz}, R_L = 200 \Omega,$ $I_{Trans,DC} = 0 \text{ mA}$
62.	Psophometric noise (see Figure 14)	N_{pVTR}		–	–80	–76	dBmp	
63.	Longitudinal to transversal rejection ratio V_{long}/V_{TR} (see Figure 15)	$LTRR$		60	70	–	dB	$V_{long} = 3 \text{ Vrms}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$
64.	Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop) (see Figure 16)	$LTRR_{loop}$		54	58	–	dB	$V_{long} = 3 \text{ Vrms}$ $300 \text{ Hz} < f < 1 \text{ kHz}$
65.				52	56	–	dB	3.4 kHz
66.	Transversal to longitudinal rejection ratio V_{TR}/V_{long} (see Figure 17)	$TLRR$		48	58	–	dB	$V_{ACP} - V_{ACN} = 1920 \text{ mVrms}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$

Electrical Characteristics

Table 14 AC Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
67.	Power supply rejection ratio V_{BATL}/V_{TR}	$PSRR$		40	60		dB	$V_{SupplyAC} = 100 \text{ mVp}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$ modes ACTH, ACTL
68.	V_{BATH}/V_{TR}			40	60			
69.	V_{HR}/V_{TR}			33	50			
70.	V_{DD}/V_{TR} (see Figure 8, 9, 10)			33	50			
71.	Interchannel crosstalk $V_{TR,B}/V_{TR,A}$		Ch. A: ACTL, ACTH, ACTR, Ch. B: ACTL, ACTH, ACTR	–	–80	t.b.d.	dB	Voiceband
72.			Ch. A: ACTL, ACTH, ACTR, Ch. B: PDH	–	–80	t.b.d.		
73.	Ringing amplitude TIP/RING	V_{RNG0}	ACTR		85		Vrms	$V_{DCP} - V_{DCN} = 0.15 \text{ V}$ (DC) + 1.42 Vrms (sine wave), $R_R = 450 \Omega$, $C_R = 3.4 \mu\text{F}$, $f = 20 \text{ Hz}$
74.	Ringing distortion (see Figure 18)	RD		–	0.1	2	%	

Transversal Current I_T

75.	Transversal current ratio (see Figure 14)	I/G_{it}		49.5	50	50.5	–	$V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$ $I_{Trans,DC} = 25 \text{ mA}$ $I_{Trans,DC} = -25 \text{ mA}$
76.				49	50	51		
77.	Total harmonic distortion V_{IT}	THD_{IT}		–	0.02	0.3	%	$I_{Trans,DC} = 25 \text{ mA}$ $V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$

Electrical Characteristics

Table 14 AC Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
78.	Psophometric noise (see Figure 14)	N_{pVIT}		–	–110	–105	dBmp	
79.	Longitudinal to transversal current output rejection ratio V_{long}/V_{IT} (see Figure 15)	$LITRR$		78			dB	$V_{long} = 3 V_{rms}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$
80.	Power supply rejection ratio V_{BATL}/V_{IT}	$PSRR$		50	70	–	dB	$V_{SupplyAC} = 100 \text{ mVp}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$
81.	V_{BATH}/V_{IT}							
82.	V_{HR}/V_{IT}							
83.	V_{DD}/V_{IT}							

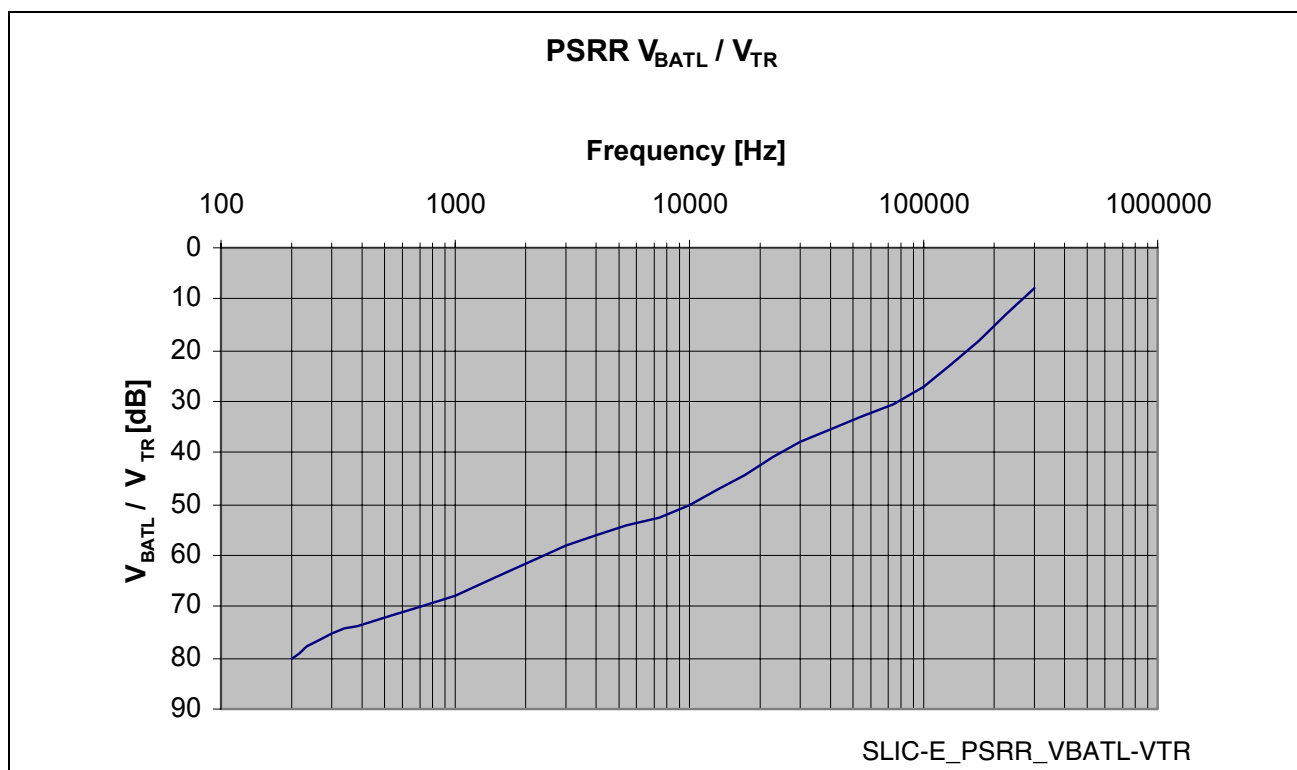


Figure 8 Typical Frequency Dependence of PSRR V_{BATL}/V_{TR}

Electrical Characteristics

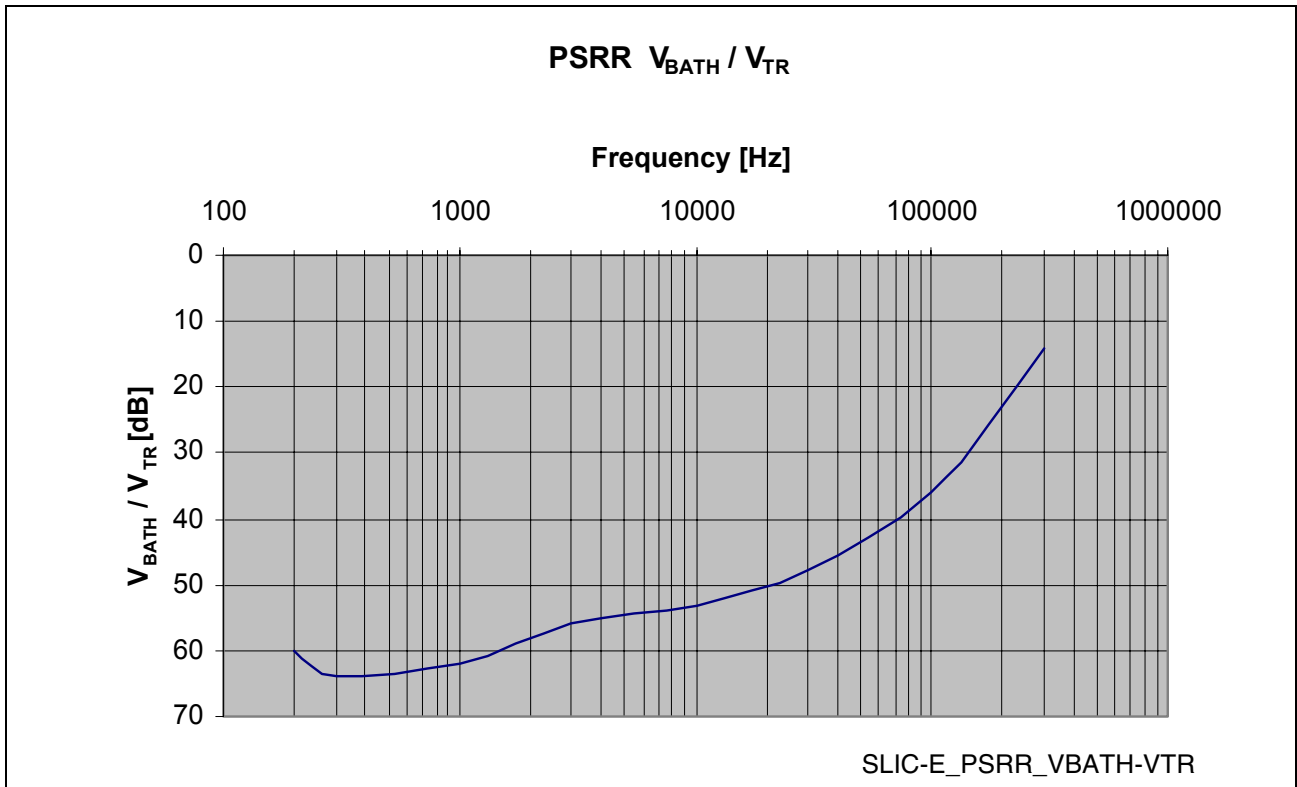


Figure 9 Typical Frequency Dependence of PSRR VBATH/VTR

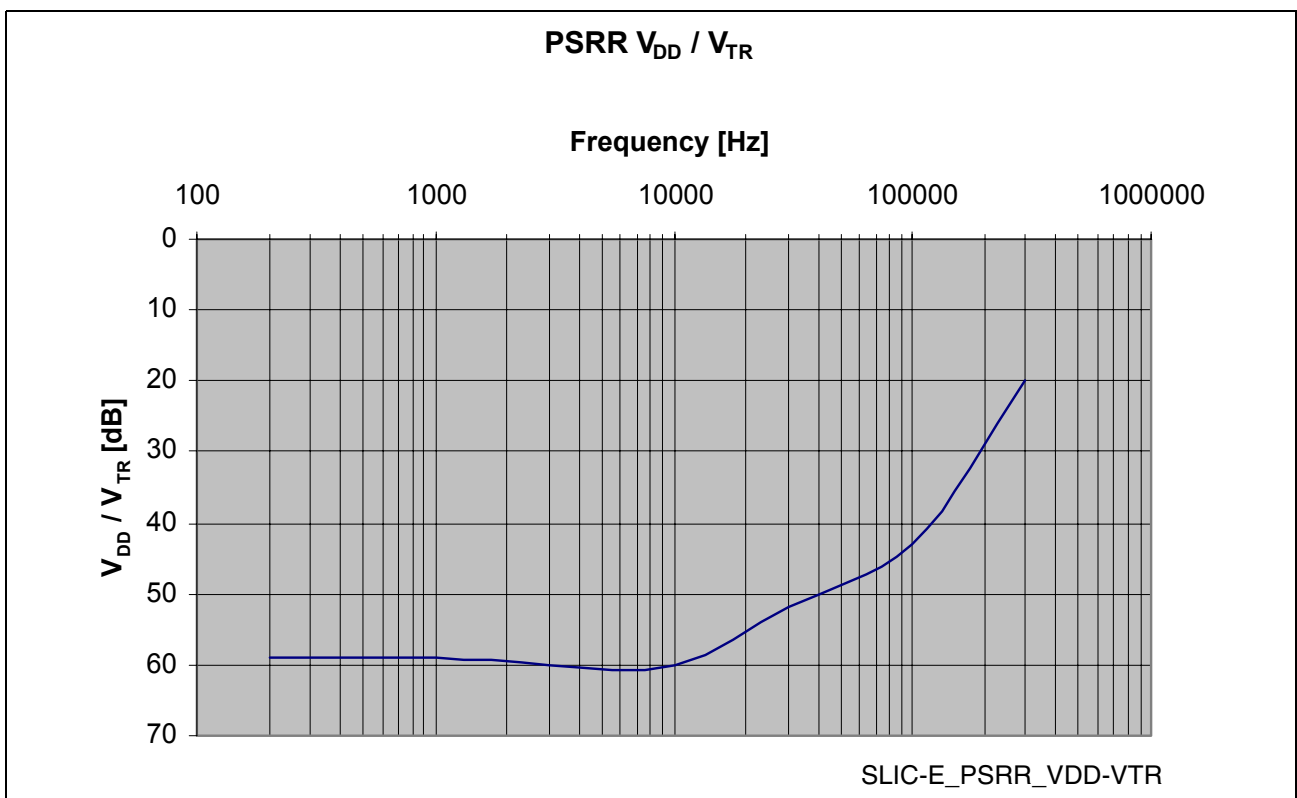


Figure 10 Typical Frequency Dependence of PSRR VDD/VTR

5 Test Figures

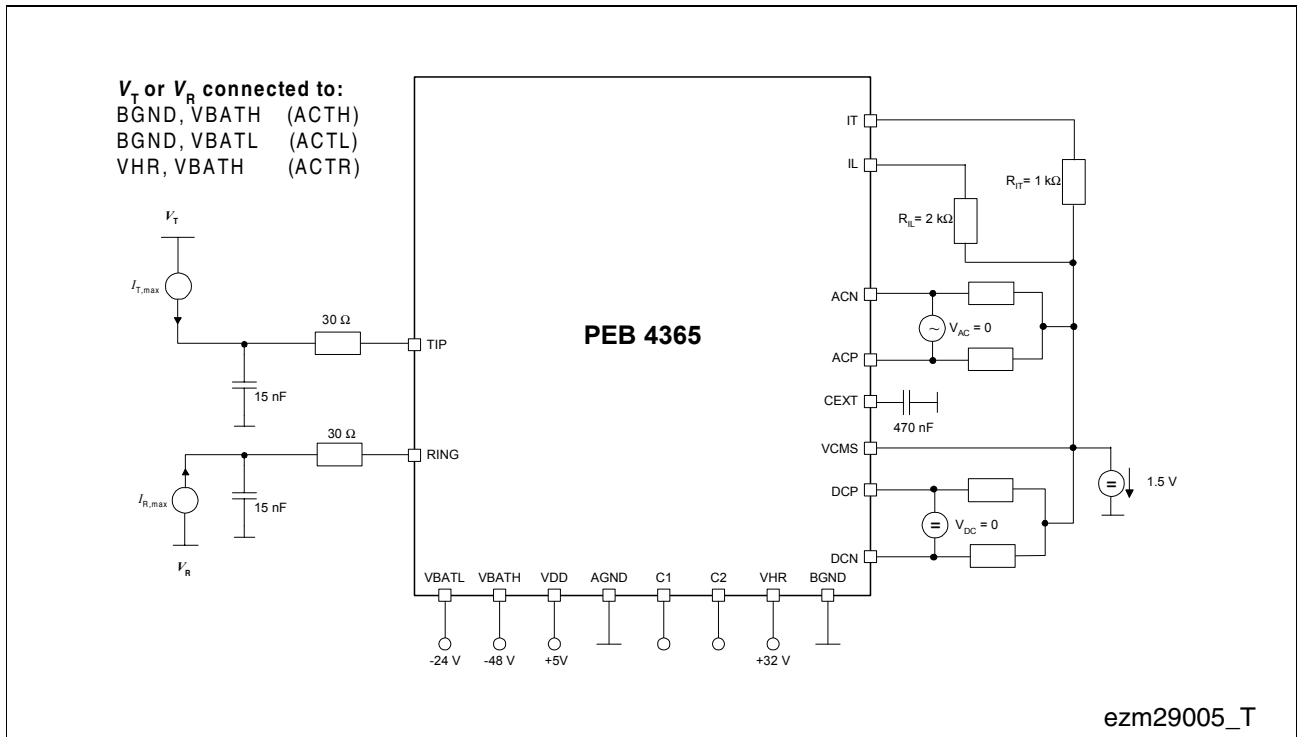


Figure 11 Output Current Limit (one Channel)

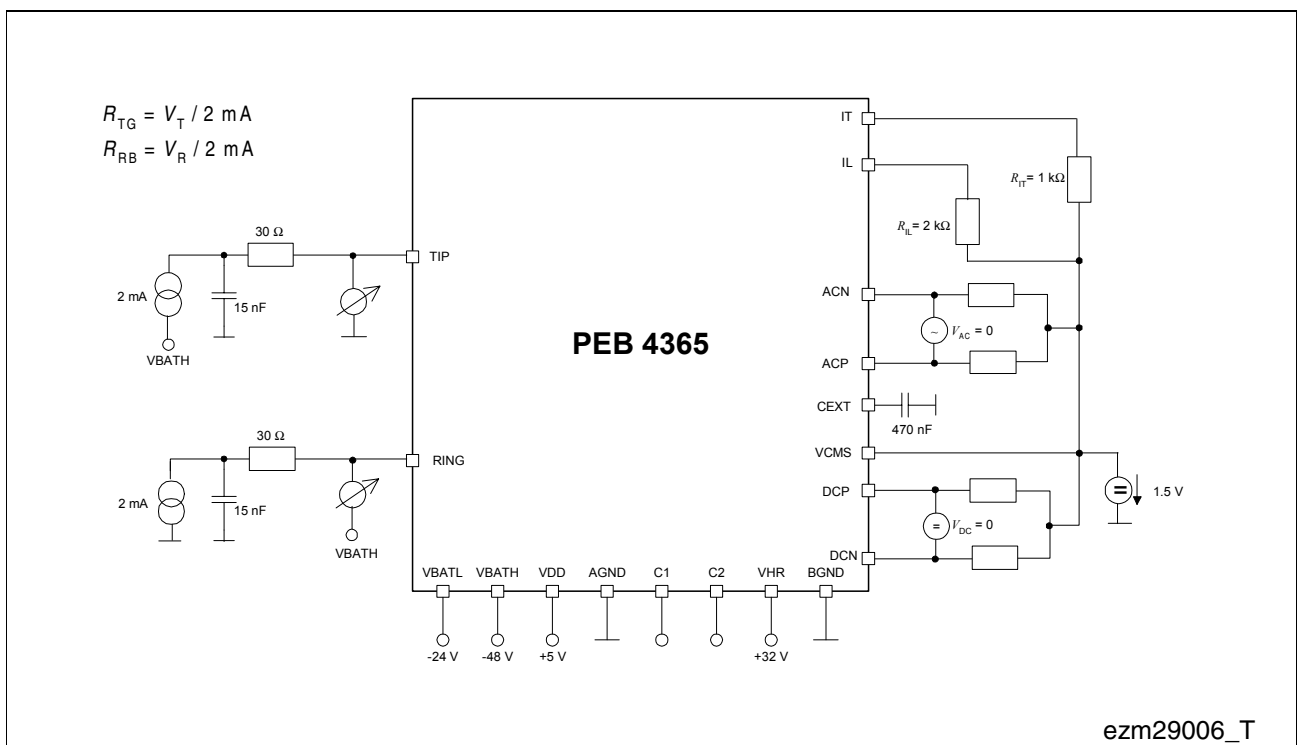


Figure 12 Output Resistance PDRH, PDRHL (one Channel)

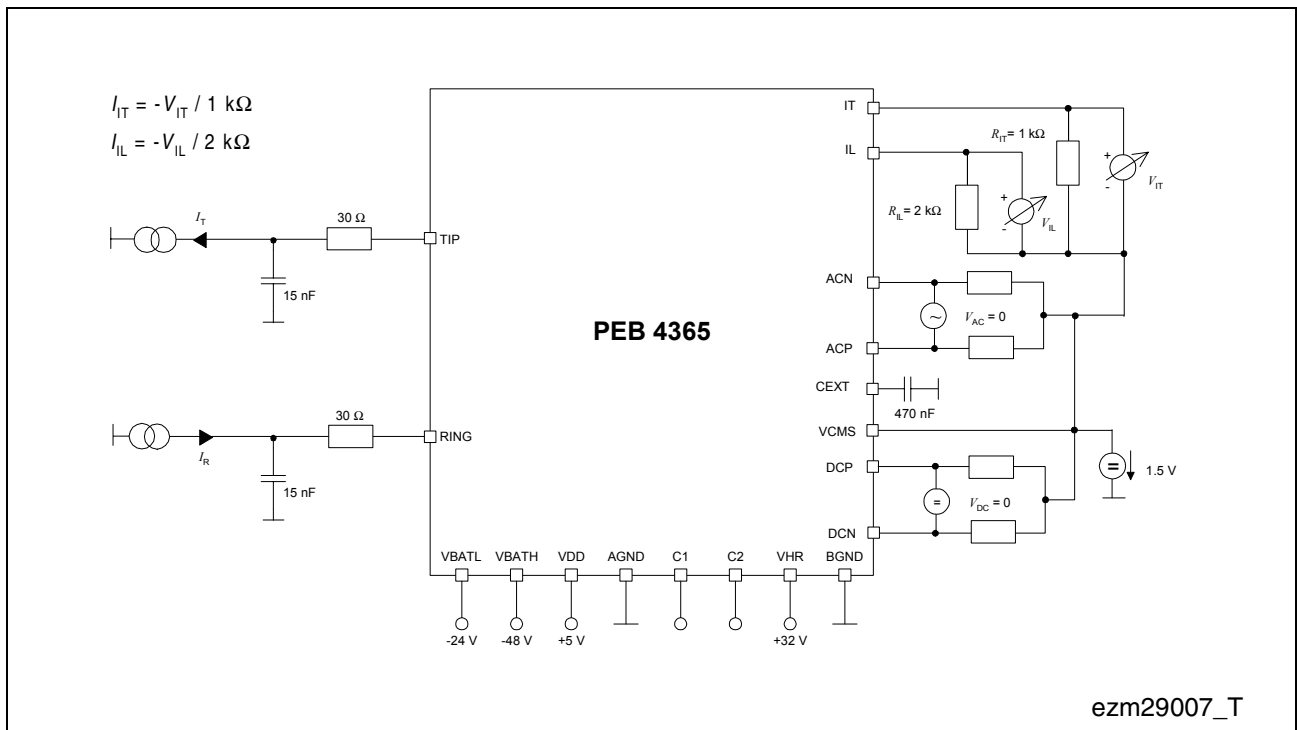


Figure 13 Current Outputs IT, IL (one Channel)

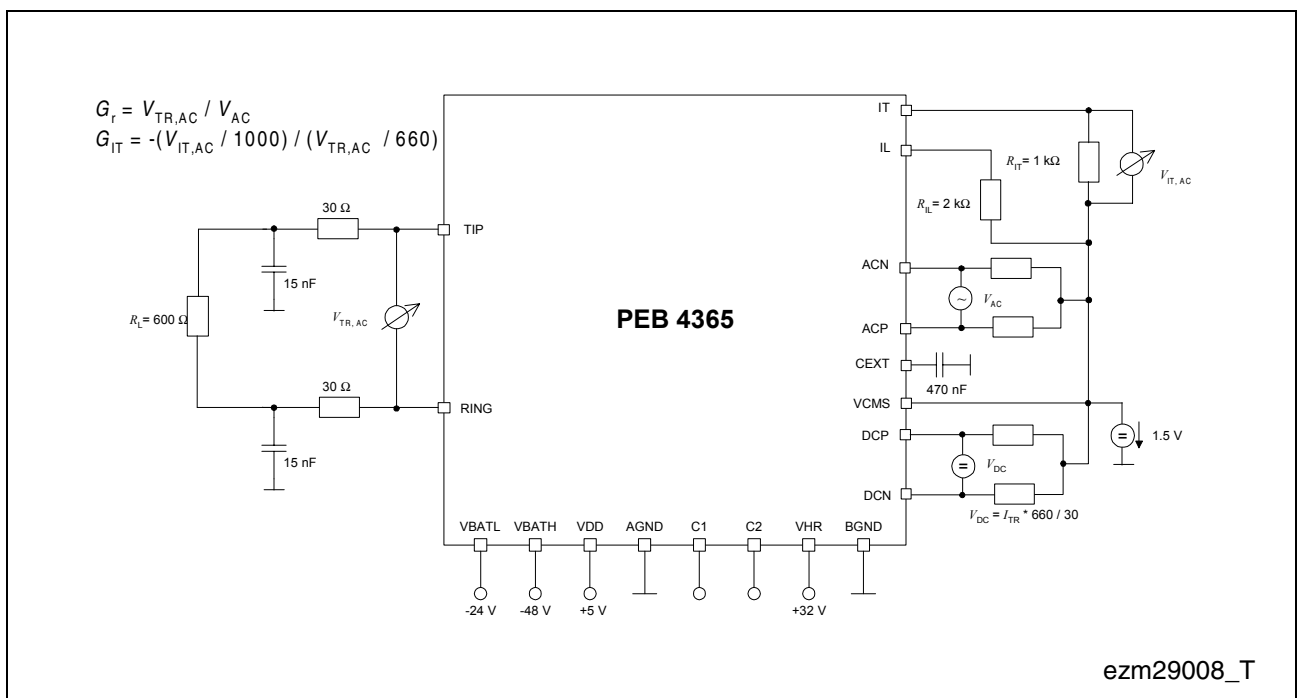


Figure 14 Transmission Characteristics (one Channel)

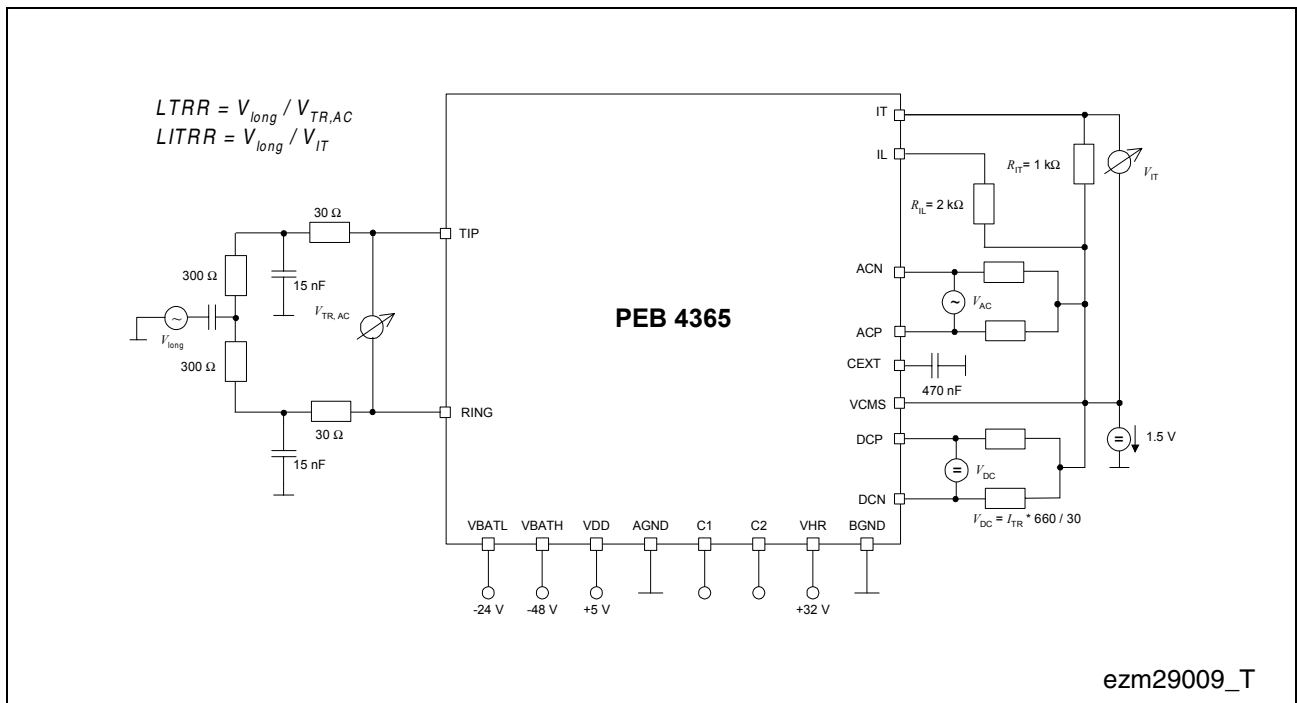


Figure 15 Longitudinal to Transversal Rejection (one Channel)

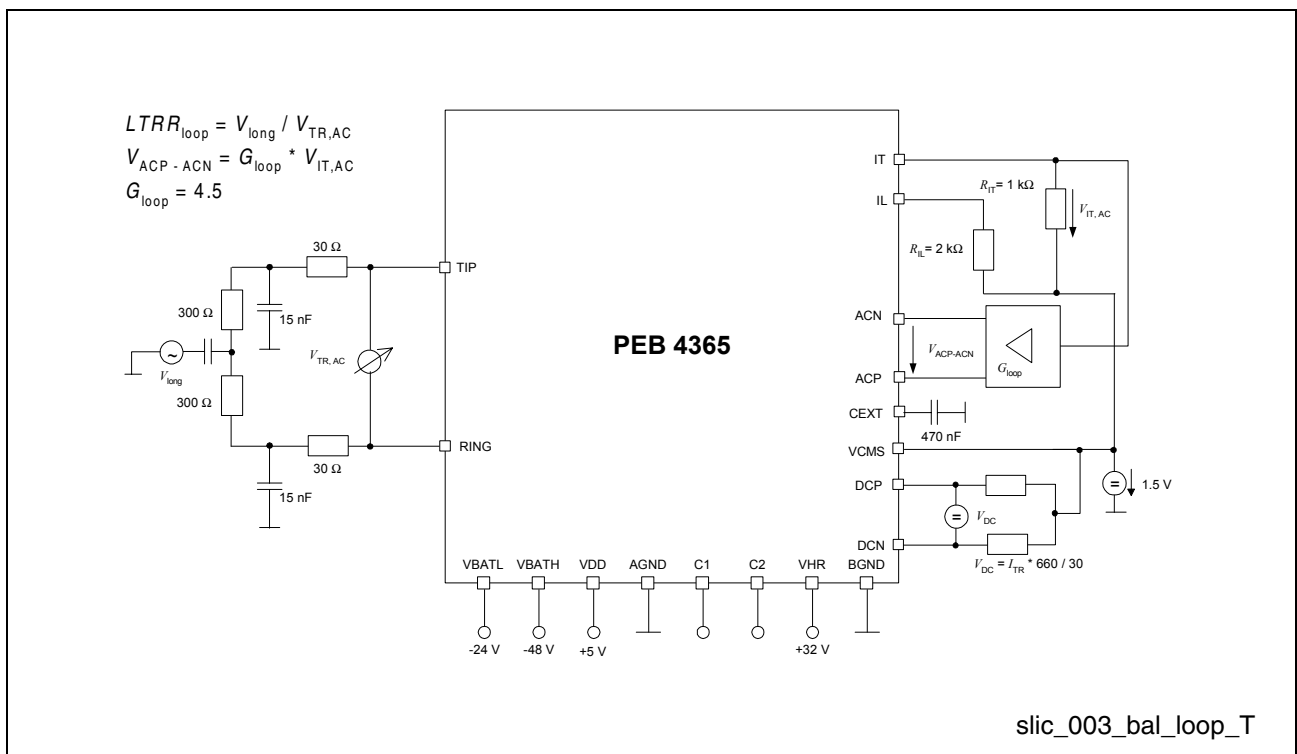


Figure 16 Longitudinal to Transversal Rejection Loop (one Channel)

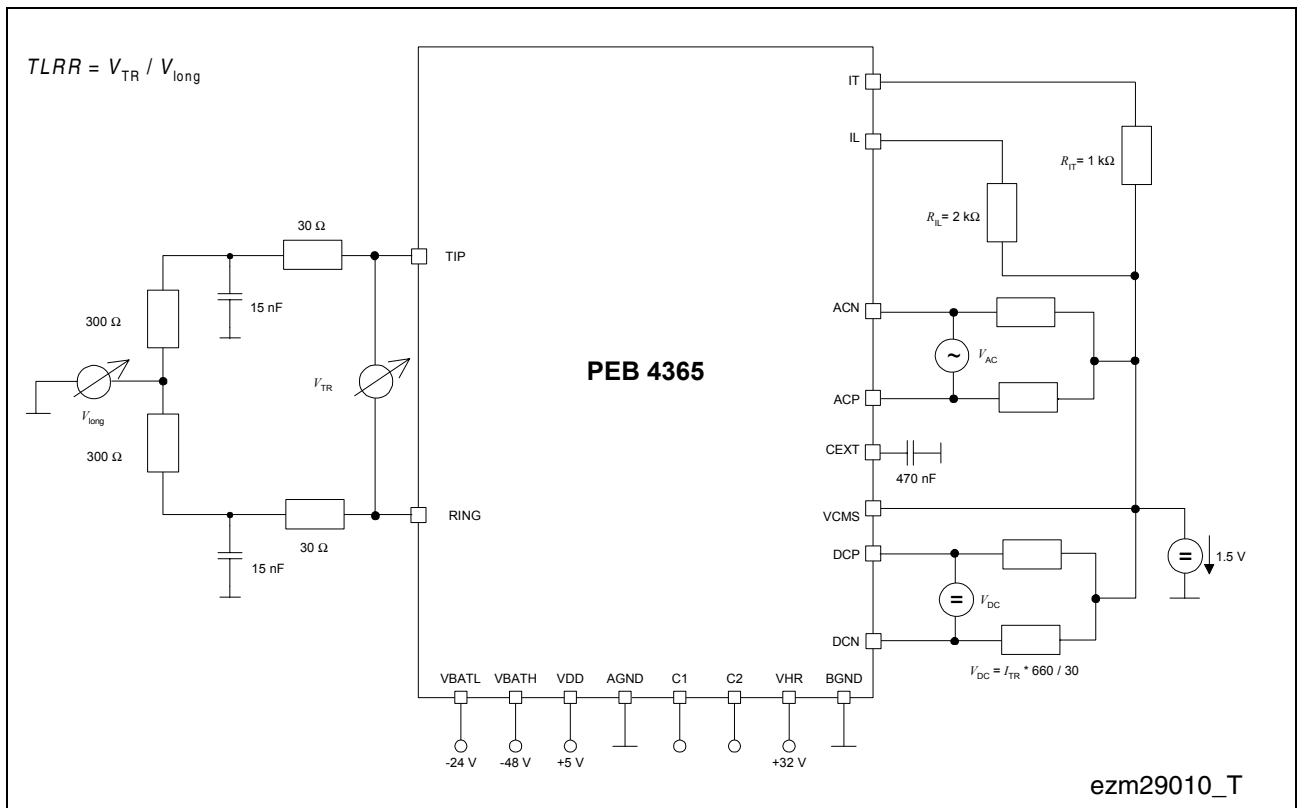


Figure 17 Transversal to Longitudinal Rejection (one Channel)

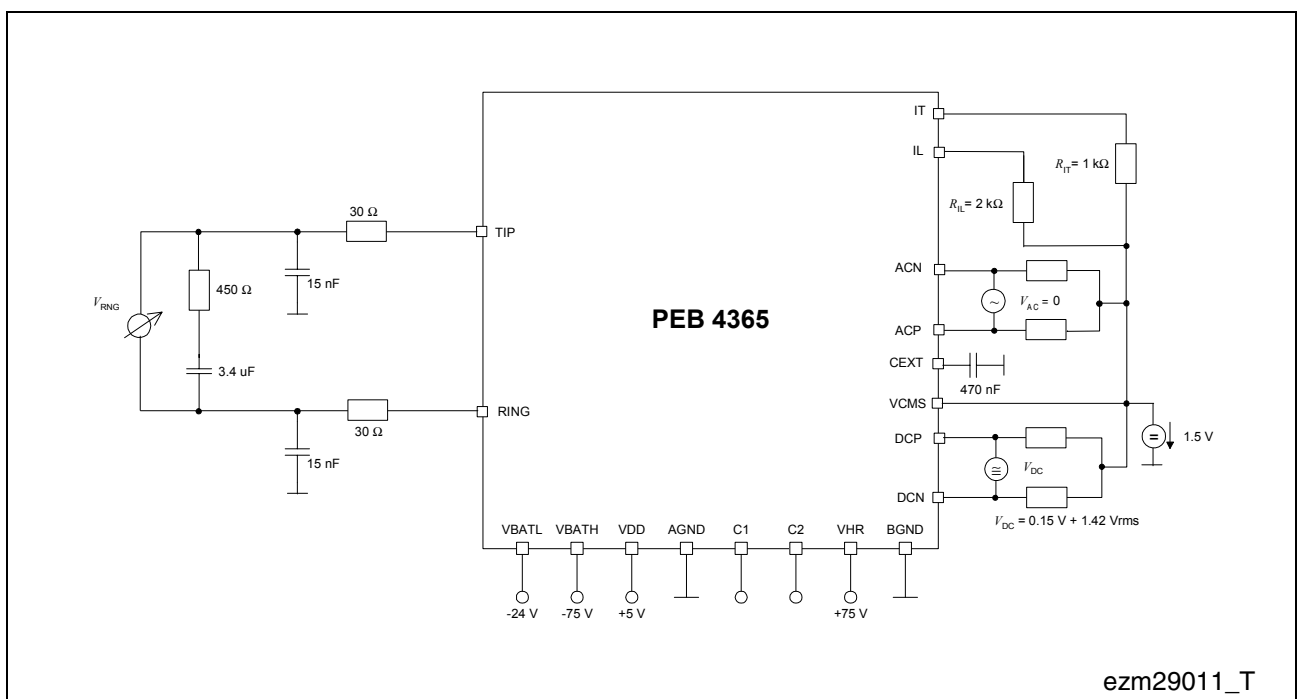


Figure 18 Ring Amplitude (one Channel)

6 Package Outlines

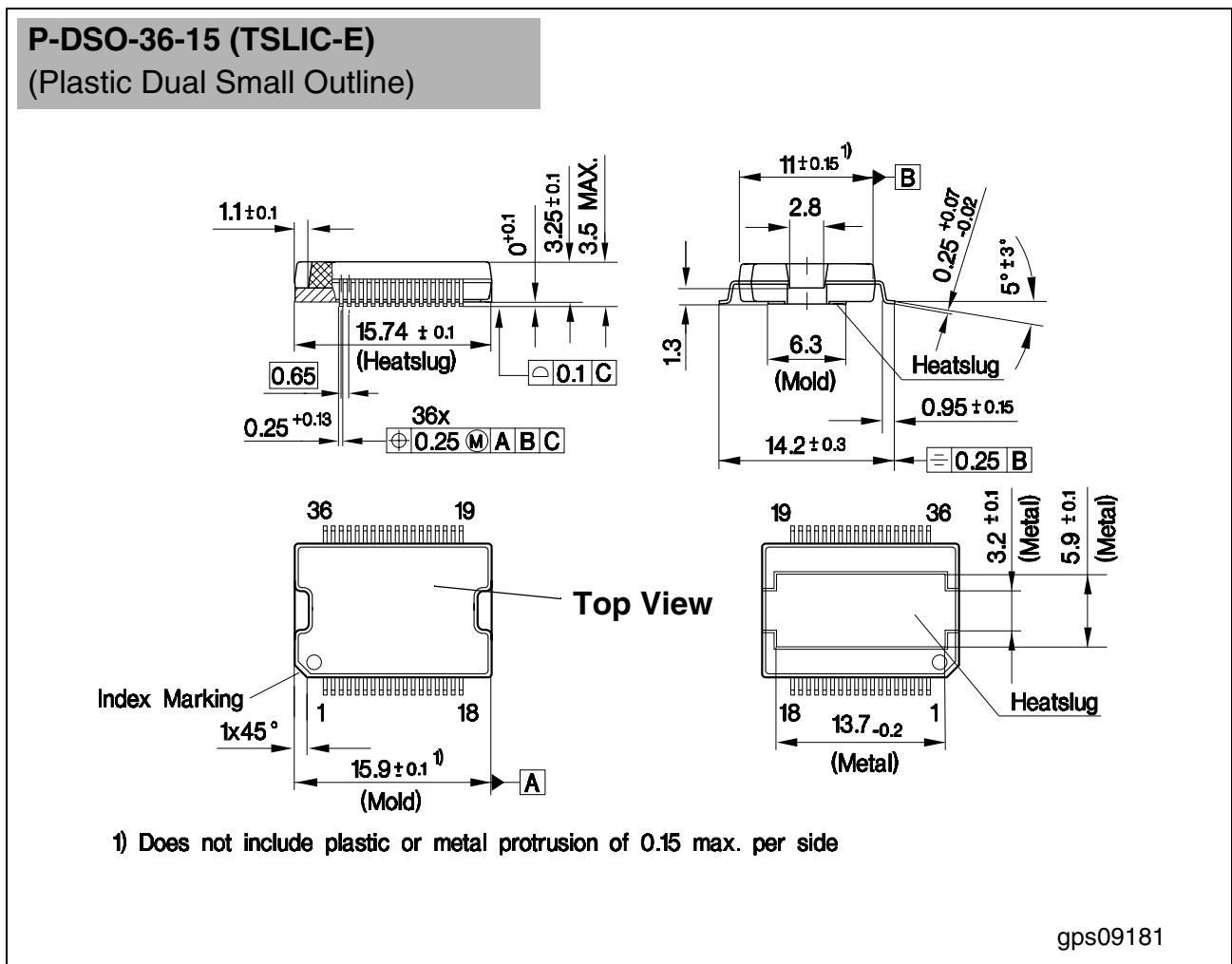


Figure 19 Package Outline P-DSO-36-15

Attention: The heatslug (see Figure 19) is connected to VBATH via the chip substrate. Due to the high voltages of up to 150 V between VHRA (VHRB) and VBATH, touching of the heatslug or any attached conducting part can be hazardous.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm

6.1 Recommended PCB Foot Print Pattern for the P-DSO-36-15

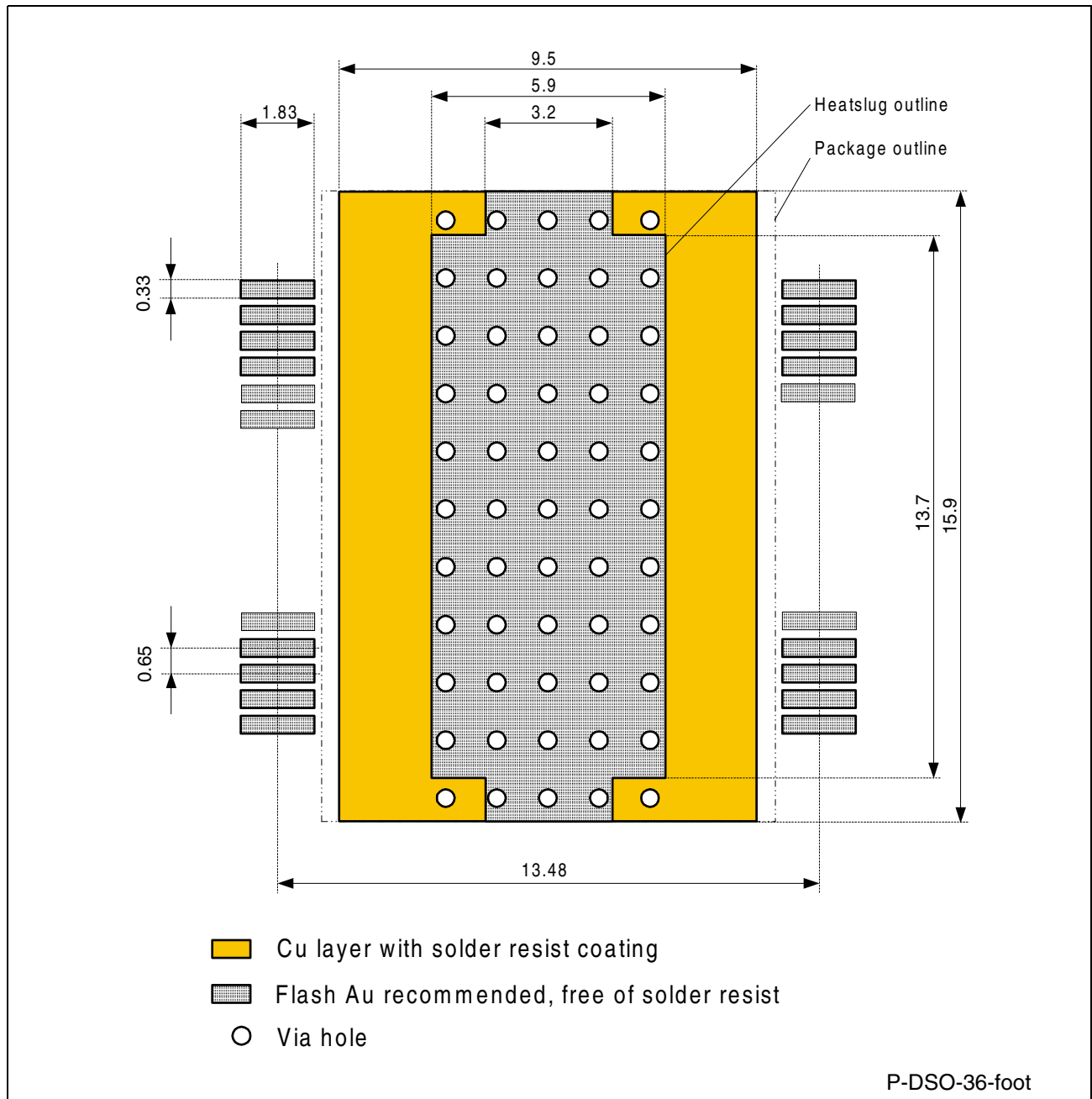


Figure 20 Foot Print for P-DSO-36-15

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