

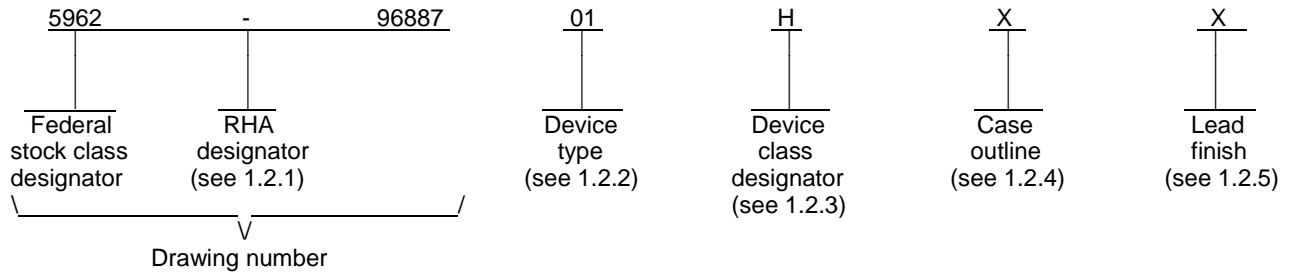
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R344-97.	97-06-12	K. A. Cottongim
B	Correct table II.	98-05-14	K. A. Cottongim
C	Correct dimensioning for figure 1, case outline Z.	01-09-25	Raymond Monnin
D	Add device type 07. Redefine table I for device types 01 through 06.	03-06-18	Raymond Monnin
E	Rewrite paragraphs 4.2.a.2. and 4.3.3.b.2 to add T _C .	04-11-15	Raymond Monnin
F	Add device types 08 through 13. Figure 1, add case outline U.	05-05-11	Raymond Monnin
G	Add devices types 14 through 17. 1.3: Correct footnote 2/ from "Hottest die." to "Since there are multiple components in this part. Thermal impedance is provided only for the hottest die". 1.4: Correct footnotes 1/ through 4/, from V _{CC} to V logic. Table I; Added supply current limits for 50 percent and 100 percent duty cycles. V _{TH} correct max limit from 700 mVp-p to 860 mVp-p. Table III, change pins "TXINHA and TXINHB" TO "TX INH OUT A and TX INH OUT B" Add terminal symbol "TX INH IN A an d TX INH IN B". -gc	13-03-19	Charles F. Saffle

REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G												
SHEET	15	16	17	18	19	20	21	22												
REV STATUS OF SHEETS	REV			G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			
PMIC N/A	PREPARED BY Gary Zahn								DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/											
STANDARD MICROCIRCUIT DRAWING	CHECKED BY Michael C. Jones																			
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY Kendall A. Cottongim								MICROCIRCUIT, HYBRID, LINEAR, MIL-STD-1553, BC/RTU/MT, MULTIPLEXED TERMINAL											
	DRAWING APPROVAL DATE 97-02-10																			
	REVISION LEVEL G																			
AMSC N/A									SHEET		1 OF 22									

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	BU61582X1	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-15 V transceiver
02	BU61582X2	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-12 V transceiver
03	BU61583X1	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-15 V transceiver, RT address latch
04	BU61583X2	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-12 V transceiver, RT address latch
05	BU61582X0	MIL-STD-1553, BC/RT/MT, 32K RAM, transceiverless
06	BU61583X0	MIL-STD-1553, BC/RT/MT, 32K RAM, transceiverless, RT address latch
07	BU61582X3	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/+5 V transceiver
08	BU63825X1	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-15 V transceiver
09	BU63825X2	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-12 V transceiver
10	BU63925X1	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-15 V transceiver, RT address latch
11	BU63925X2	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-12 V transceiver, RT address latch
12	BU63825X0	MIL-STD-1553, BC/RT/MT, 32K RAM, transceiverless
13	BU63925X0	MIL-STD-1553, BC/RT/MT, 32K RAM, transceiverless, RT address latch
14	BU63825X3	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/+5 V transceiver
15	BU63825X6	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/+5 V transceiver with "TX INHIBIT" (Transmit Inhibit)
16	BU63925X3	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/+5 V transceiver, RT address latch
17	BU63925X6	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/+5 V transceiver, RT address latch with "TX INHIBIT" (Transmit Inhibit)

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

<u>Device class</u>	<u>Device performance documentation</u>
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.

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G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
U	See figure 1	70	Flat package with ceramic tie bars
X	See figure 1	70	Dual-in-line
Y	See figure 1	70	Flat package
Z	See figure 1	70	Gull wing

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. ^{1/}

Transceiver, channels A and B, positive input supply voltage range (+5VA, +5VB): Device types 01 through 04, and 07.....	-0.3 V dc to +6.0 V dc
Transceiver, channels A and B, positive input supply voltage range (+5VA, +5VB): Device types 08 through 11, and 14 through 17.....	-0.5 V dc to +7.0 V dc
Transceiver, channels A and B, negative input supply voltage range (-VA, -VB): Device types 01, 02, 03, and 04.....	+0.5 V dc to -18 V dc
Transceiver, channels A and B, negative input supply voltage range (-VA, -VB): Device types 08, 09, 10, and 11.....	+0.5 V dc to -18 V dc
Logic supply voltage range (+5 V logic): Device types 01 through 07.....	-0.3 V dc to +6.0 V dc
Device types 08 through 17.....	-0.5 V dc to +6.5 V dc
Power dissipation (P _D): ^{1/} ^{2/} ^{3/} Device types 01, 03, 08, and 10.....	3.77 W
Device types 02, 04, 09, and 11.....	3.71 W
Device types 05, 06, 12, and 13.....	0.75 W
Device type 07, and 14 through 17.....	2.23 W
Storage temperature range.....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction to case (θ _{JC}): Device types 01 through 07.....	6.99°C/W ^{2/}
Device types 08, 09, 10, and 11.....	7.82°C/W ^{2/}
Device types 12 and 13.....	7.10°C/W ^{2/}
Device types 14 through 17.....	12°C/W ^{2/}

^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Applies up to T_C = +125°C.

^{2/} Since there are multiple components in this part. Thermal impedance is provided only for the hottest die.

^{3/} Assumes 100 percent transmitter duty cycle on one channel and 0 percent duty cycle on the other channel.

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1.4 Recommended operating conditions.

Transceiver, channels A and B, positive input supply voltage range (+5VA, +5VB):	
Device types 01 through 04 and 08 through 11	+4.5 V dc to +5.5 V dc
Device types 07, and 14 through 17	+4.75 V dc to +5.25 V dc
Logic supply voltage range (+5 V logic):	
Device types 01 through 06 and 08 through 17	+4.5 V dc to +5.5 V dc
Device type 07	+4.75 V dc to +5.25 V dc
Transceiver, channels A and B, negative input supply voltage range (-VA, -VB):	
Device types 01, 03, 08 and 10	-14.25 V dc to -15.75 V dc
Device types 02, 04, 09, and 11	-11.40 V dc to -12.60 V dc
Minimum logic high input voltage (V _{IH}):	
Device types 01 through 07	3.9 V dc
Device types 08 through 17	3.85 V dc <u>1/</u>
Device types 08 through 17	2.0 V dc <u>2/</u>
Maximum logic low input voltage (V _{IL}):	
Device types 01 through 07	1.3 V dc
Device types 08 through 17	1.3 V dc
Device types 08 through 17	1.35 V dc <u>3/</u>
Device types 08 through 17	0.8 V dc <u>4/</u>
Operating frequency (F _{OP})	12 MHz or 16 MHz
Case operating temperature range (T _C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

- 1/ At V logic = 5.5 V dc, MSTCLR, CLOCK IN, STRBD inputs.
2/ At V logic = 5.5 V dc, all other inputs.
3/ At V logic = 4.5 V dc, MSTCLR, CLOCK IN, STRBD inputs.
4/ At V logic = 4.5 V dc, all other inputs.

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3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Pin functions. The pin functions shall be as specified in table III.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime -VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime -VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) T_A or T_C as specified in the approved manufacturer's QM plan.
 - (3) Burn-in test shall be for 320 hours.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- c. 100% Nondestructive bond pull test.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
+5 volt supply current, Idle 2/	I _{CC1}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V	1,2,3	01-04	5	190	mA
		+5 V logic = +5.5 V		05,06	5	150	
		+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V		07	5	250	
		+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V		08-11	5	240	
		+5 V logic = +5.5 V		12,13	5	190	
		+5 V logic = +5.5 V, +5VA = +5VB = +5.25 V		14-17	5	250	
+5 volt supply current, 25% duty cycle (One Channel Transmitting) 2/	I _{CC2}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V	1,2,3	01-04	5	190	mA
		+5 V logic = +5.5 V		05,06	5	150	
		+5 V logic = +5.5 V, +5VA = +5VB = +5.25 V		07	5	250	
		+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V		08-11	5	240	
		+5 V logic = +5.5 V		12,13	5	190	
		+5 V logic = +5.5 V, +5VA = +5VB = +5.25 V		14-17	5	355	
+5 volt supply current, 50% duty cycle (One Channel Transmitting) 2/	I _{CC3}	+5VA = +5VB = +5.5 V +5VA = +5VB = +5.5 V	1,2,3	01-04,	5	190	mA
				08-11		240	
		+5 V logic = +5.5 V		05,06	5	150	
				12,13		190	
		+5VA = +5VB = +5.5 V, +5VA = +5VB = +5.25 V		07	5	335	
				14-17		460	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
+5 volt supply current, 100% duty cycle (One Channel Transmitting) <u>2/</u>	I _{CC4}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V	1,2,3	08-11	5	240	mA
		+5 V logic = +5.5 V		12,13	5	190	
		+5 V logic = +5.5 V, +5VA = +5VB = +5.25 V		14-17	5	670	
Negative supply current <u>3/</u>	I _{EE1}	+5 V logic = +5.5 V, -VA = -VB = -12.60 V for device types 02 and 04. -VA = -VB = -15.75 V for device types 01 and 03.	1,2,3	01-04	5	60	mA
		+5 V logic = +5.5 V, -VA = -VB = -12.60 V for device types 09 and 11. -VA = -VB = -15.75 V for device types 08 and 10.		08-11	5	60	
Negative supply current, 25% duty cycle (One Channel Transmitting) <u>3/</u>	I _{EE2}	+5 V logic = +5.5 V, -VA = -VB = -12.60 V for device types 02 and 04. -VA = -VB = -15.75 V for device types 01 and 03.	1,2,3	01,03	25	108	mA
				02,04	25	120	
		+5 V logic = +5.5 V, -VA = -VB = -12.60 V for device types 09 and 11. -VA = -VB = -15.75 V for device types 08 and 10.		08,10	25	108	
				09,11	25	120	
Negative supply current, 50% duty cycle (One Channel Transmitting) <u>3/</u>	I _{EE3}	+5 V logic = +5.5 V, -VA = -VB = -12.60 V for device types 02,04, 09 and 11. -VA = -VB = -15.75 V for device types 01, 03, 08, and 10.	1,2,3	01,03	25	175	mA
				02,04	25	185	
Negative supply current, 50% duty cycle (One Channel Transmitting) <u>3/</u>	I _{EE4}	+5 V logic = +5.5 V, -VA = -VB = -12.60 V for device types 09 and 11. -VA = -VB = -15.75 V for device types 08 and 10.	1,2,3	08,10	25	270	
				09,11	25	305	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input current 4/	I _{IL1}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V, V _{IN} = 0 V	1,2,3	01-04	-550	-60	μA
		+5 V logic = +5.5 V, V _{IN} = 0 V		05,06	-550	-60	
		+5 V logic = +5.25 V, +5VA = +5VB = +5.25 V, V _{IN} = 0 V		07	-550	-60	
Low level input current 5/	I _{IL2}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V, V _{IN} = 0 V	1,2,3	01-04	-10	+10	μA
		+5 V logic = +5.5 V, V _{IN} = 0 V		05,06	-10	+10	
		+5 V logic = +5.25 V, +5VA = +5VB = +5.25 V, V _{IN} = 0 V		07	-10	+10	
Low level input current 4/ 5/ (All but pin 19, CLOCK IN)	I _{IL3}	+5 V logic = +5.5 V, V _{IN} = 0 V	1,2,3	08-17	-600	-60	μA
Low level input current (Pin 19, CLOCK IN, only)	I _{IL4}	+5 V logic = +5.5 V, V _{IN} = 0 V	1,2,3	08-17	-10	+10	μA
High level input current 4/	I _{IH1}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V, V _{IN} = 2.4 V	1,2,3	01-04	-150	-25	μA
		+5 V logic = +5.5 V, V _{IN} = 2.4 V		05,06	-150	-25	
		+5 V logic = +5.25 V, +5VA = +5VB = +5.25 V, V _{IN} = 2.4 V		07	-150	-25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input current <u>5/</u>	I _{IH2}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V, V _{IN} = 2.4 V	1,2,3	01-04	-10	+10	μA
		+5 V logic = +5.5 V, V _{IN} = 2.4 V		05,06	-10	+10	
		+5 V logic = +5.25 V, +5VA = +5VB = +5.25 V, V _{IN} = 2.4 V		07	-10	+10	
High level input current <u>4/ 5/</u> (All but pin 19, CLOCK IN)	I _{IH3}	+5 V logic = +5.5 V, V _{IN} = 2.7	1,2,3	08-17	-400	-20	μA
High level input current (Pin 19, CLOCK IN, only)	I _{IH4}	+5 V logic = +5.5 V, V _{IN} = 2.7	1,2,3	08-17	-10	+10	μA
Output voltage low <u>6/</u>	V _{OL}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V, I _{OL} = -6.4 mA	1,2,3	01-04		0.5	V
		+5 V logic = +5.5 V, I _{OL} = -6.4 mA		05,06		0.5	
		+5 V logic = +5.25 V, +5VA = +5VB = +5.25 V, I _{OL} = -6.4 mA		07		0.5	
		+5 V logic = +4.5 V, I _{OL} = -8 mA		08-17		0.5	
Output voltage high <u>6/</u>	V _{OH}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V, I _{OH} = 6.4 mA	1,2,3	01-04	4.0		V
		+5 V logic = +5.5 V, I _{OH} = 6.4 mA		05,06	4.0		
		+5 V logic = +5.25 V, +5VA = +5VB = +5.25 V, I _{OH} = 6.4 mA		07	4.0		
		+5 V logic = +4.5 V, I _{OH} = 8 mA		08-17	4.0		
Functional tests		See 4.3.1b.	7,8	All			Pass/ fail
Receiver threshold	V _{TH}	Transformer coupled into a 70 Ω resistive load	4,5,6	All	500	860	mVp-p

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Transmitter differential output voltage	V _O	Transformer coupled into a 70 Ω resistive load	4,5,6	All	18	27	Vp-p
Transmitter output rise time	t _R	Transformer coupled into a 70 Ω resistive load	4,5,6	All	100	300	ns
Transmitter output fall time	t _F	Transformer coupled into a 70 Ω resistive load	4,5,6	All	100	300	ns
Transmitter output offset voltage <u>7/</u>	V _{OS}	Transformer coupled into a 70 Ω resistive load	4,5,6	All	-250	+250	mVp-p

1/ Unless otherwise specified:

+5 V logic = +5.0 V for all device types.

+5VA = +5VB = +5.0 V for all device types.

-VA = -VB = -15.0 V for device types 01, 03, 08, and 10.

-VA = -VB = -12.0 V for device types 02, 04, 09, and 11.

2/ Measured at the following pins: Pins 38, 54, and 68.

3/ Measured at the following pins: Pins 36 and 70.

4/ Measured at the following pins: Pins 8-17, 20-25, 29-32, 39-44, 46-53, and 55-62.

5/ Measured at the following pins: Pins 3-7, 19, 26, 27, 33, 63, and 64.

6/ Measured at the following pins: Pins 8-17, 20-25, 28-32, 45-53, 55-62, and 65-67.

7/ Parameter shall be tested as part of the initial characterization of these devices and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.

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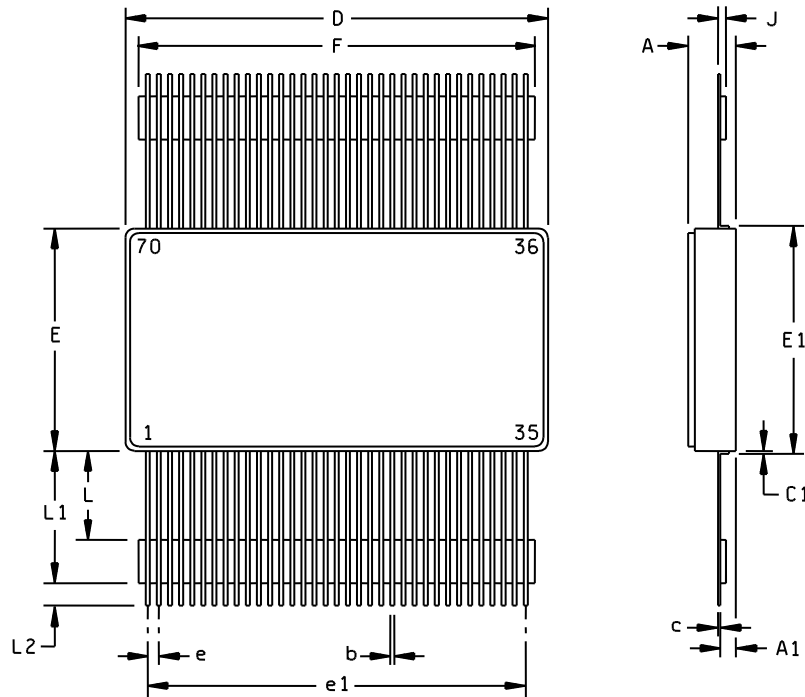
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A

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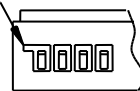
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Case outline U.



INDEX DENOTES
PIN 1



Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	5.46	---	.215
A1	1.52	2.03	.060	.080
b	0.41	0.51	.016	.020
c	0.20	0.30	.008	.012
C1	---	0.30	---	.012
D	---	48.26	---	1.900
E	---	25.40	---	1.000
E1	---	26.01	---	1.024
e	1.27 TYP		.050 TYP	
e1	43.05	43.31	1.695	1.705
F	44.20	45.21	1.740	1.780
J	0.89 TYP		.035 TYP	
L	10.29	---	.405	---
L1	---	15.11	---	.595
L2	---	2.54	---	.100

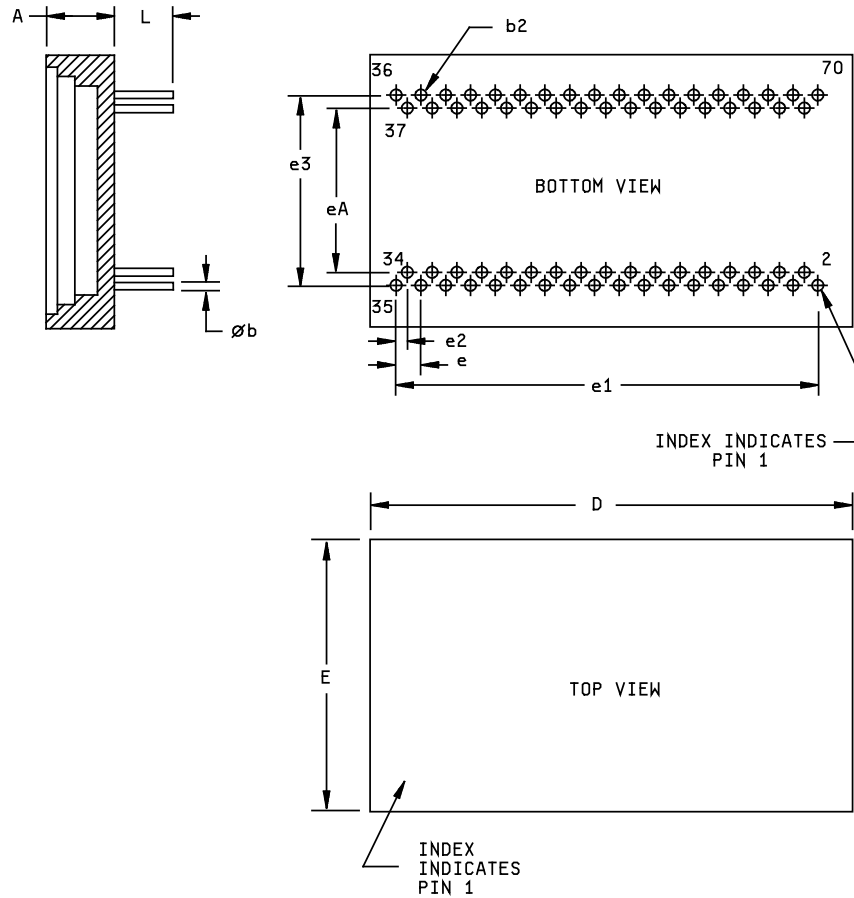
NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s).

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Case outline X.



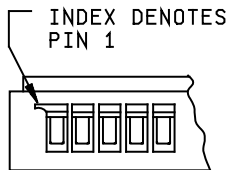
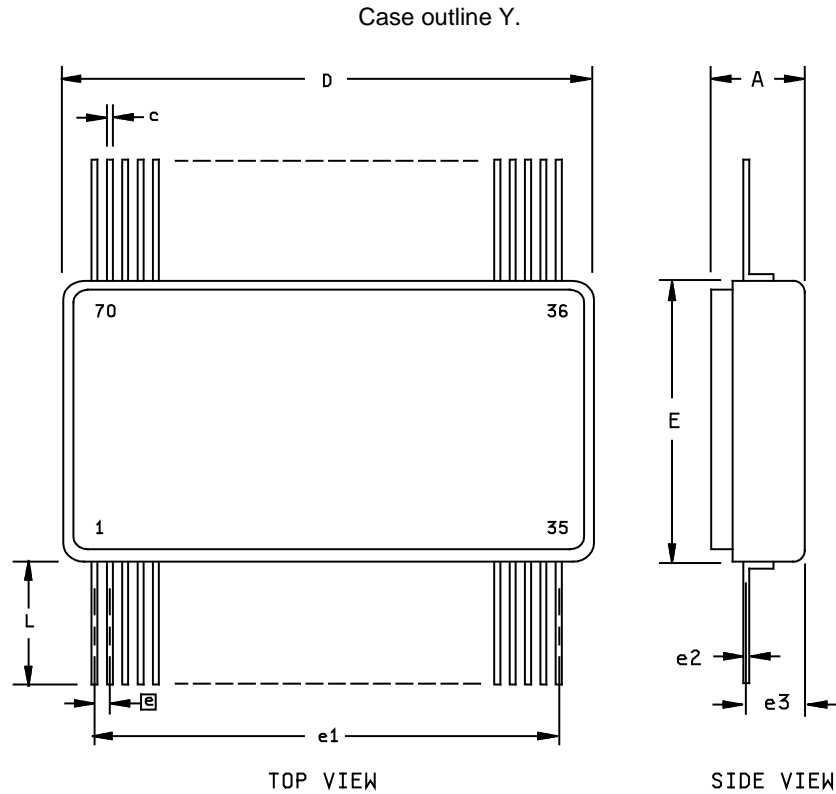
Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	5.46	---	.215
øb	0.41	0.51	.016	.020
b2	1.65	1.91	.065	.075
D	---	48.26	---	1.900
e	2.41	2.67	.095	.105
eA	10.03	10.29	.395	.405
e1	43.05	43.31	1.695	1.705
e2	1.14	1.40	.045	.055
e3	15.11	15.37	.595	.605
E	---	25.40	---	1.000
L	4.32	4.83	.170	.190

NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	5.46	---	.215
c	0.41	0.51	.016	.020
D	---	48.26	---	1.900
e	1.14	1.40	.045	.055
e1	43.05	43.31	1.695	1.705
e2	0.20	0.30	.008	.012
e3	1.52	2.03	.060	.080
E	---	25.40	---	1.000
L	10.16	---	.400	---

NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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Case outline Z.

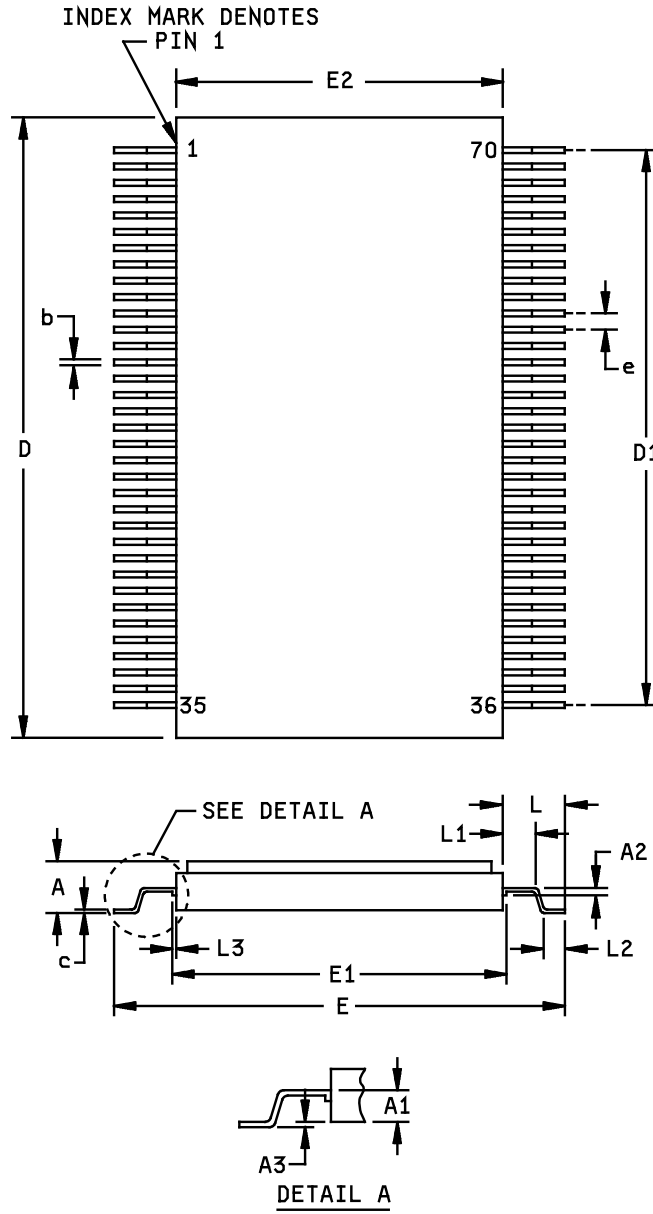


FIGURE 1. Case outline(s) - Continued.

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Case outline Z - Continued.

Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	5.46	---	.215
A1	1.65 REF		.065 REF	
A2	1.02 TYP		.040 TYP	
A3	0.08	0.38	.003	.015
b	0.41	0.51	.016	.020
c	0.20	0.30	.008	.012
D	---	48.26	---	1.900
D1	43.05	43.31	1.695	1.705
E	34.54	35.56	1.360	1.400
E1	---	26.01	---	1.024
E2	---	25.40	---	1.000
e	1.27 TYP		.050 TYP	
L	4.57	5.08	.180	.200
L1	2.03	---	.080	---
L2	1.27	---	.050	---
L3	---	0.30	---	.012

NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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Device types	All		
Case outlines	U, X, Y, and Z		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	<u>TX/RX-A</u> 1/	36	-VB 1/ 2/ 3/
2	<u>TX/RX-A</u> 1/	37	GNDB 1/
3	<u>SELECT</u>	38	+5VB 1/
4	<u>STRBD</u>	39	RTAD0
5	<u>MEM/REG</u>	40	RTAD1
6	<u>RD/WR</u>	41	RTAD2
7	<u>MSTCLR</u>	42	RTAD3
8	A15	43	RTAD4
9	A14	44	<u>RTADP</u>
10	A13	45	INCMD
11	A12	46	D00
12	A11	47	D01
13	A10	48	D02
14	A09	49	D03
15	A08	50	D04
16	A07	51	D05
17	A06	52	D06
18	LOGIC GND	53	D07
19	CLOCK_IN	54	+5 V LOGIC
20	A05	55	D08
21	A04	56	D09
22	A03	57	D10
23	A02	58	D11
24	A01	59	D12
25	<u>A00</u>	60	D13
26	<u>DTGRT/MSB/LSB</u>	61	D14
27	<u>SSFLAG/EXT_TRIG</u>	62	D15
28	<u>MEMENA_OUT</u>	63	TAG_CLK
29	<u>MEMOE/ADDR_LAT</u>	64	<u>TRANSPARENT/BUFFERED</u>
30	<u>MEMWR/ZERO_WAIT</u>	65	<u>INT</u>
31	<u>DTREQ/16/8</u>	66	<u>READYD</u>
32	<u>DTACK/POLARITY_SEL</u>	67	IOEN
33	<u>MEMENA_IN/TRIGGER_SEL</u>	68	+5VA 1/
34	<u>TX/RX-B</u> 1/	69	GNDA 1/
35	<u>TX/RX-B</u> 1/	70	-VA 1/ 2/ 3/

NOTES:

- 1/ For device types 05, 06, 12, and 13; pin 1 is RXA, pin 2 is RXA, pin 34 is RXB, pin 35 is RXB, pin 36 is TX INH OUT B, pin 37 is TXB, pin 38 is TXB, pin 68 is TX INH OUT A, pin 69 is TXA, and pin 70 is TXA.
- 2/ For device types 01, 03, 08, and 10; pin 36 and pin 70 are -15 V.
For device types 02, 04, 09, and 11; pin 36 and pin 70 are -12 V.
For device type 07, 14, and 16; pin 36 and pin 70 are no connects (N/C).
- 3/ For device types 15 and 17: pin 36 is TX INH IN B pin 70 is TX INH IN A.

FIGURE 2. Terminal connections.

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6,7,8
Final electrical parameters	1*,2,3,4,5,6,7,8
Group A test requirements	1,2,3,4,5,6,7,8
Group C end-point electrical parameters	1,2,3,4,5,6,7,8
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 9, 10, and 11 shall be omitted
- c. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendors test tape and shall be maintained and available from the approved source of supply.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) T_A or T_C as specified in the approved manufacturer's QM plan.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Post Office Box 3990, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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TABLE III. Pin functions.

Terminal symbol	I/O	Description
D00	I/O	Data bus bit 0 (LSB).
D02	I/O	Data bus bit 2.
D04	I/O	Data bus bit 4.
D06	I/O	Data bus bit 6.
D08	I/O	Data bus bit 8.
D10	I/O	Data bus bit 10.
D12	I/O	Data bus bit 12.
D14	I/O	Data bus bit 14.
RTAD1	I	Remote terminal address bit 1.
RTAD0	I	Remote terminal address bit 0 (LSB).
RTAD4	I	Remote terminal address bit 4 (MSB).
+5 V LOGIC	I	+5 volt supply input for digital logic section.
TAG CLK	I	External Time Tag Clock Input for BC/RT modes.
-VB	I	Input power supply connection for the B channel transceiver. -15 V for device types 01, 03, 08, and 10. -12 V for device types 02, 04, 09, and 11.
TX INH OUT A and TX INH OUT B	O	Digital transmit inhibit outputs. Asserted high to inhibit transmitting on the respective bus. For device types 05, 06, 12, and 13.
GNDB	-	Ground B. Power supply return connection for the B channel transceiver.
TX/RX-B	I/O	Transmit/receive transceiver-B. Input/output to the coupling transformer that connects to the B channel of the 1553 bus.
LOGIC GND	-	Logic ground. Power supply return for the digital logic section.
A01	I/O	Address bit 1.
A03	I/O	Address bit 3.
A05	I/O	Address bit 5.
A07	I/O	Address bit 7.
A09	I/O	Address bit 9.
A11	I/O	Address bit 11.
A13	I/O	Address bit 13.
A15	I/O	Address bit 15 (MSB).
TX INH OUT A and TX INH OUT B	I	Transmitter inhibit inputs for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel A and/or Channel B, a value of logic "1" should be applied to the respective TX INH IN input. For device types 15 and 17.

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{MEMOE}}/\text{ADDR_LAT}$	I/O	Memory Output Enable/Address Latch. In transparent mode, used to enable data outputs for external RAM. In buffered mode, input used to configure the internal address buffers.
$\overline{\text{MEMENA-OUT}}$	O	Memory enable out. <u>Logic 0</u> output enables external RAM. Used with $\overline{\text{MEMOE}}$ to read data or with $\overline{\text{MEMWR}}$ to write data into external RAM.
CLOCK IN	I	Clock input. 16 MHz TTL clock.
$\overline{\text{MEM/REG}}$	I	Memory/register. Input from CPU to select memory or register data transfer.
$\overline{\text{STRBD}}$	I	Strobe data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate a data transfer cycle to/from CPU.
$\overline{\text{TRANSPARENT/}}/\text{BUFFERED}$	I	Used to select between the transparent and buffered modes for the host processor interface.
D11	I/O	Data bus bit 11.
D13	I/O	Data bus bit 13.
D15	I/O	Data bus bit 15 (MSB).
RTAD3	I	Remote terminal address bit 3.
RTAD2	I	Remote terminal address bit 2.
RTADP	I	Remote terminal address parity input.
$\overline{\text{RD/WR}}$	I	Read/write. Input from the CPU which defines the data bus transfer as a read or write operation.
GNDA	-	Ground A. Power supply return connection for the A channel transceiver.
-VA	I	Input power supply connection for the A channel transceiver. -15 V for device types 01, 03, 08, and 10. -12 V for device types 02, 04, 09, and 11.
TX/RX-A	I/O	Transmit/receive transceiver-A. Input/output to the coupling transformer that connects to the A channel of the 1553 bus.
D01	I/O	Data bus bit 1.
D03	I/O	Data bus bit 3.
D05	I/O	Data bus bit 5.
D07	I/O	Data bus bit 7.
D09	I/O	Data bus bit 9.

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
+5 VB	I	+5 V power supply connection for the B channel transceiver.
$\overline{\text{TX/RX-B}}$	I/O	Transmit/receive transceiver-B. Inverted input/output to coupling transformer that connects to channel B of the 1553 bus.
A00	I/O	Address bit 0 (LSB).
A02	I/O	Address bit 2.
A04	I/O	Address bit 4.
A06	I/O	Address bit 6.
A08	I/O	Address bit 8.
A10	I/O	Address bit 10.
A12	I/O	Address bit 12.
A14	I/O	Address bit 14.
$\overline{\text{MEMWR/ZERO WAIT}}$	O/I	Memory write. Output pulse to write data into memory.
$\overline{\text{MEMENA-IN/ TRIGGER SEL}}$	I	Memory enable input. Enables internal RAM only: connect directly to MEMENA-OUT
$\overline{\text{INCMD}}$	O	Input command. Indicates BC to RTU currently in message transfer sequence.
$\overline{\text{MSTRCLR}}$	I	Master clear. Power-on reset from CPU.
$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
$\overline{\text{IOEN}}$	O	Input/out enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.
$\overline{\text{SELECT}}$	I	Select. Input from the CPU. When active selects device for operation.
$\overline{\text{READYD}}$	O	Ready data. When active indicates data has been received from, or is available to, the CPU.
+5 VA	I	+5 V power supply connection for the channel A transceiver.
$\overline{\text{TX/RX-A}}$	I/O	Transmit/receive transceiver-A. Inverted input/output to the coupling transformer that connects to A channel of the 1553 bus.
$\overline{\text{DTREQ/16/8}}$	O/I	Data Transfer Request or 16 Bit/8 Bit Transfer Mode Select. In transparent mode, active low output signal used to request access to the RAM interface bus (address, data, and control buses). In buffered mode, input signal used to select between the 16 bit data transfer mode (16/8 = Logic 1) and the 8 bit data transfer mode (16/8 = Logic 0).

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{MEMWR/ZERO_WAIT}}$	O/I	Memory Write or Zero Wait State. In transparent mode, active low output signal asserted low during memory write transfers to strobe data into internal or external RAM (normally connected to the WR signal on external RAM chips). In buffered mode, input signal used to select between the zero wait state mode ($\overline{\text{ZEROWAIT}} = \text{logic 0}$) and the non-zero wait state mode ($\overline{\text{ZEROWAIT}} = \text{logic 1}$).
$\overline{\text{MEMENA-IN/ TRIGGER_SEL}}$	I	Memory Enable Input or Trigger Select. In transparent mode, active low Chip Select (CS) input to the 4K X 16 of internal shared RAM. If only internal RAM is used connect directly to MEMENA-OUT. In buffered mode, input signal used to indicate the order in which byte pairs are transferred to or from the device by the host processor. This signal has no operation in the 16-bit buffered mode. In the 8-bit buffered mode, TRIGGER_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB followed LSB. TRIGGER_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB followed MSB.
$\overline{\text{DTACK/POLARITY_SEL}}$	O/I	Data Transfer Acknowledge or Polarity Select. In transparent mode, active low output signal used to indicate acceptance of the RAM interface bus in response to a data transfer grant (DTGRT). In 16-bit buffered mode ($\overline{\text{TRANSPARENT/BUFFERED}} = \text{LOGIC 0 AND } 16/8 = \text{LOGIC 1}$), input signal used to control the logic sense of the RD/WR signal. If POLARITY_SEL is connected to logic 1, RD/WR should be asserted high (logic 1) for a read operation and low (logic 0) for a write operation. If POLARITY_SEL is connected to logic 0, RD/WR should be asserted low (logic 0) for a read operation and high (logic 1) for a write operation. In 8-bit buffered mode ($\overline{\text{TRANSPARENT/BUFFERED}} = \text{LOGIC 0 AND } 16/8 = \text{LOGIC 0}$), input signal used to control the logic sense of the MSB/LSB signal. If POLARITY_SEL is connected to logic 0, MSB/LSB should be asserted low (logic 0) to indicate the transfer of the least significant byte and high (logic 1) to indicate the transfer of the most significant byte. If POLARITY_SEL is connected to logic 1, MSB/LSB should be asserted high (logic 1) to indicate the transfer of the least significant byte and low (logic 0) to indicate the transfer of the most significant byte.
$\overline{\text{DTGRT/MSB/LSB}}$	I	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In transparent mode, active low input signal asserted, in response to the DTREQ output, to indicate that control of the RAM interface bus has been granted to the device. In buffered mode, input signal used to indicate which byte is currently being transferred (MSB or LSB). The logic sense of MSB/LSB is controlled by the POLARITY_SEL input. MSB/LSB is only used in the 8-bit buffered mode.
$\overline{\text{SSFLAG/EXT_TRIG}}$	I	Sub System Flag/External Trigger Input. In the Remote Terminal mode, if this input is asserted low, the subsystem flag bit will be set in the device's RT Status Word. In the Bus Controller mode if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the Monitor mode if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a monitor trigger. This input has no effect in RT mode.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-03-19

Approved sources of supply for SMD 5962-96887 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9688701HXA 5962-9688701HXC 5962-9688701HYA 5962-9688701HYC 5962-9688701HZA 5962-9688701HZC	<u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> /	BU61582D1-140 BU61582D1-110 BU61582F1-140 BU61582F1-110 BU61582G1-140 BU61582G1-110
5962-9688702HXA 5962-9688702HXC 5962-9688702HYA 5962-9688702HYC 5962-9688702HZA 5962-9688702HZC	<u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> /	BU61582D2-140 BU61582D2-110 BU61582F2-140 BU61582F2-110 BU61582G2-140 BU61582G2-110
5962-9688703HXA 5962-9688703HXC 5962-9688703HYA 5962-9688703HYC 5962-9688703HZA 5962-9688703HZC	<u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> /	BU61583D1-140 BU61583D1-110 BU61583F1-140 BU61583F1-110 BU61583G1-140 BU61583G1-110
5962-9688704HXA 5962-9688704HXC 5962-9688704HYA 5962-9688704HYC 5962-9688704HZA 5962-9688704HZC	<u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> /	BU61583D2-140 BU61583D2-110 BU61583F2-140 BU61583F2-110 BU61583G2-140 BU61583G2-110
5962-9688705HXA 5962-9688705HXC 5962-9688705HYA 5962-9688705HYC 5962-9688705HZA 5962-9688705HZC	<u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> /	BU61582D0-140 BU61582D0-110 BU61582F0-140 BU61582F0-110 BU61582G0-140 BU61582G0-110
5962-9688706HXA 5962-9688706HXC 5962-9688706HYA 5962-9688706HYC 5962-9688706HZA 5962-9688706HZC	<u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> /	BU61583D0-140 BU61583D0-110 BU61583F0-140 BU61583F0-110 BU61583G0-140 BU61583G0-110

See notes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

DATE: 13-03-19

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9688707HXA 5962-9688707HXC 5962-9688707HYA 5962-9688707HYC 5962-9688707HZA 5962-9688707HZC	<u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> / <u>3</u> /	BU61582D3-140 BU61582D3-110 BU61582F3-140 BU61582F3-110 BU61582G3-140 BU61582G3-110
5962-9688708HUA 5962-9688708HUC 5962-9688708HXA 5962-9688708HXC 5962-9688708HZA 5962-9688708HZC	19645 19645 19645 19645 19645 19645	BU63825F1-140 BU63825F1-110 BU63825D1-140 BU63825D1-110 BU63825G1-140 BU63825G1-110
5962-9688708KUA 5962-9688708KUC	19645 19645	BU63825F1-603 BU63825F1-603
5962-9688709HUA 5962-9688709HUC 5962-9688709HXA 5962-9688709HXC 5962-9688709HZA 5962-9688709HZC	19645 19645 19645 19645 19645 19645	BU63825F2-140 BU63825F2-110 BU63825D2-140 BU63825D2-110 BU63825G2-140 BU63825G2-110
5962-9688710HUA 5962-9688710HUC 5962-9688710HXA 5962-9688710HXC 5962-9688710HZA 5962-9688710HZC	19645 19645 19645 19645 19645 19645	BU63925F1-140 BU63925F1-110 BU63925D1-140 BU63925D1-110 BU63925G1-140 BU63925G1-110
5962-9688711HUA 5962-9688711HUC 5962-9688711HXA 5962-9688711HXC 5962-9688711HZA 5962-9688711HZC	19645 19645 19645 19645 19645 19645	BU63925F2-140 BU63925F2-110 BU63925D2-140 BU63925D2-110 BU63925G2-140 BU63925G2-110
5962-9688712HUA 5962-9688712HUC 5962-9688712HXA 5962-9688712HXC 5962-9688712HZA 5962-9688712HZC	19645 19645 19645 19645 19645 19645	BU63825F0-140 BU63825F0-110 BU63825D0-140 BU63825D0-110 BU63825G0-140 BU63825G0-110
5962-9688713HUA 5962-9688713HUC 5962-9688713HXA 5962-9688713HXC 5962-9688713HZA 5962-9688713HZC	19645 19645 19645 19645 19645 19645	BU63925F0-140 BU63925F0-110 BU63925D0-140 BU63925D0-110 BU63925G0-140 BU63925G0-110

See notes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

DATE: 13-03-19

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9688714HUA 5962-9688714HUC 5962-9688714HXA 5962-9688714HXC 5962-9688714HZA 5962-9688714HZC	19645 19645 19645 19645 19645 19645	BU63825F3-140 BU63825F3-110 BU63825D3-140 BU63825D3-110 BU63825G3-140 BU63825G3-110
5962-9688715HUA 5962-9688715HUC 5962-9688715HXA 5962-9688715HXC 5962-9688715HZA 5962-9688715HZC	19645 19645 19645 19645 19645 19645	BU63825F6-140 BU63825F6-110 BU63825D6-140 BU63825D6-110 BU63825G6-140 BU63825G6-110
5962-9688716HUA 5962-9688716HUC 5962-9688716HXA 5962-9688716HXC 5962-9688716HZA 5962-9688716HZC	19645 19645 19645 19645 19645 19645	BU63925F3-140 BU63925F3-110 BU63925D3-140 BU63925D3-110 BU63925G3-140 BU63925G3-110
5962-9688717HUA 5962-9688717HUC 5962-9688717HXA 5962-9688717HXC 5962-9688717HZA 5962-9688717HZC	19645 19645 19645 19645 19645 19645	BU63925F6-140 BU63925F6-110 BU63925D6-140 BU63925D6-110 BU63925G6-140 BU63925G6-110

- 1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ No longer available from an approved source of supply.

Vendor CAGE
number

19645

Vendor name
and address

Data Device Corporation
105 Wilbur Place
Bohemia, NY 11716-2482