MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33091

Advance Information

High Side TMOS Driver

HIGH SIDE TMOS DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

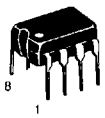
The MC33091 is a high side TMOS driver designed for use in harsh automotive switching applications which require the capability of handling high voltages attributed to load and field dump transients, as well as reverse and double battery conditions. Few external components are required to drive a wide variety of N-Channel TMOS applications. The MC33091, driving an appropriate TMOS device, offers an economical systems solution to high side switching large currents. The MC33091 has CMOS compatible input control, charge pump to drive the TMOS power transistor, basic fault detection circuit, V_{DS} monitoring circuit used to detect a shorted TMOS load, and an over current protection timer with associated current squaring circuitry.

Short circuit protection is made possible by having a unique V_{DS} voltage to current converter drive an externally programmable integrator circuit. This circuit affords quick detection of a shorted load while allowing difficult loads, such as lamps having high in-rush currents, additional time to turn on.

The $\overline{\text{Fault}}$ output is comprised of an open collector NPN transistor requiring a single pull-up resistor for operation. A fault is reported whenever the MOSFET on-current exceeds an externally programmed set level.

The MC33091 is available in the plastic 8 pin DIP as well as the 8 pin surface mount package.

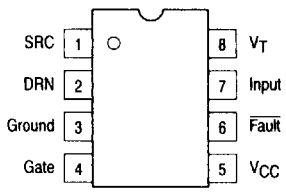
- Designed for Automotive High Side Drive Applications
- Works with a Wide Variety of N-Channel Power MOSFETs
- Drives Inductive Loads with No External Clamp Circuitry Required
- CMOS Logic Compatible Input Control
- Low Standby Current (<3.0 μA)
- On Board Charge Pump with No External Components Required
- Shorted Load Detection and Protection
- Forward Overvoltage and Reverse Battery Protection
- Load and Field Dump Protection
- Extended Operating Temperature Range
- $\overline{\text{Fault}}$ Output to Report an Over MOSFET Current Condition



P SUFFIX
PLASTIC PACKAGE
CASE 626

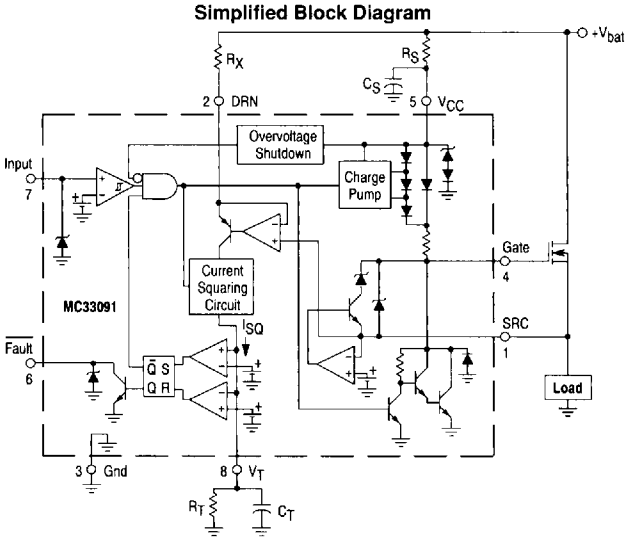
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC33091P	–40° to +125°C	Plastic DIP
MC33091D		SO-8

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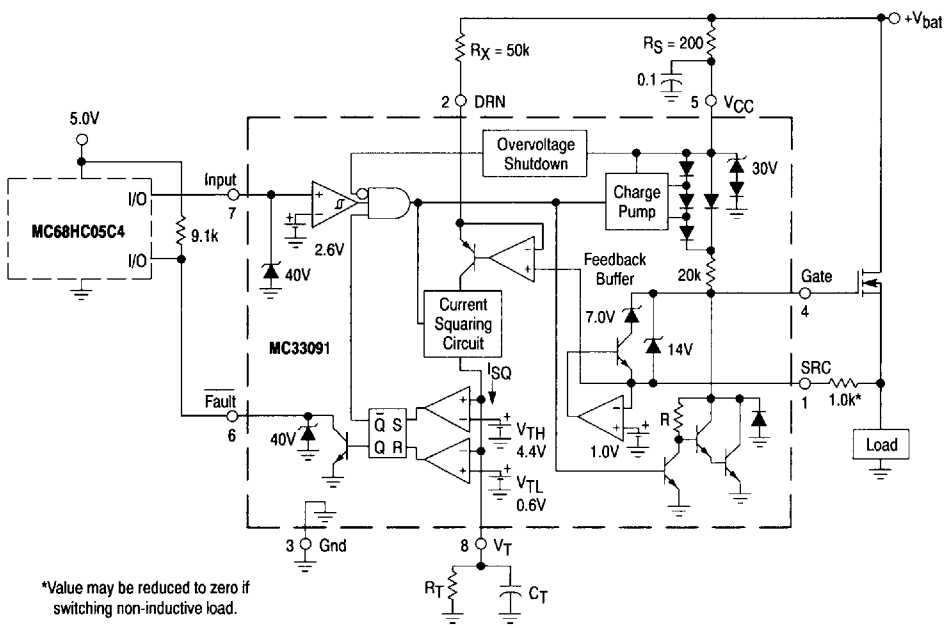
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Pin 5) (Note 1) Continuous (without activating clamp) Operational	V_{CC}	 –0.7 to +28 +7.0 to +28	V
Continuous Supply Clamp Current (Pin 5) DIP Package (Case 626) SO-8 Package (Case 751)	I_C	 10 1.0	mA
Input Control Voltage Range (Pin 7) Continuous	V_{in}	 –0.7 to +28	V
$\overline{\text{Fault}}$ Pull-up Voltage Range (Pin 6) Continuous	V_{out}	 –0.7 to +28	V
Minimum ESD Voltage Capability (Note 2)	ESD	2000	V
Operating Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Ambient Temperature Range	T_A	–40 to +125	°C
Thermal Resistance (Junction-to-Ambient) DIP Package (Case 626) SO-8 Package (Case 751)	θ_{JA}	 100 145	°C/W

NOTES: 1. An internal zener diode is incorporated to protect the device from overvoltage transients in excess of 30 V.
2. ESD testing performed in accordance with Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).

Figure 1. Typical Application



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ELECTRICAL CHARACTERISTICS (Values are noted under conditions of 7.0 V ≤ V_{CC} ≤ 24 V, –40°C ≤ T_A ≤ +125°C, unless otherwise noted. Typical values reflect approximate mean at T_A = 25°C at time of device characterization.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Supply Current (Note 1) V_{in}= 0 V V_{in} = 5.0 V (R_X = 100 k)	2	I_{CC}	 — —	 0.026 2.5	 3.0 6.0	 µA mA
Supply Clamp Voltage (Note 2)		V_Z	29	—	35	V
Gate to Source Voltage Range (Pin 4)	3,4,5,7	V_{GS}	8.0	12	15	V
Gate Current (Pin 4) V_G = V_{CC}	3,4	I_G	 30	 —	 400	µA
Short Circuit Gate Clamp Voltage (Note 4)	5	V_{GC}	6.4	7.0	7.7	V
Input Control Threshold Voltage (Pin 7)	7	 V_{IL} V_{IH}	 — 3.5	 2.7 2.7	 1.5 —	V
Input Control Current (Pin 7) (V_{in} = 5.0 V)	8	I_{in}	—	100	250	µA
Timer Current Constant (Pin 8) (R_X = 100 k, V_T = 0, V_{DS} = 1.0 V) (Note 3)	9,10	K	 0.7	 1.1	 1.5	µA/V²
Timer (Pin 8) Lower Threshold Voltage Upper Threshold Voltage	 16,17 18,19	 V_{TL} V_{TH}	 0.4 4.1	 0.6 4.4	 1.2 4.8	V
$\overline{\text{Fault}}$ Sink Current (Pin 6) V_F = 5.0 V V_F = 0	11	 I_{OL} I_{OH}	 500 —	 — 2.0	 — 100	 µA nA
$\overline{\text{Fault}}$ Saturation Voltage (Pin 6) (I_F = 500 µA)	11	V_{OL}	—	0.2	0.8	V
Gate Saturation Voltage (I_G = 10 µA)	20,21	$V_{G(sat)}$	0	1.2	1.4	V

NOTES: 1. The total supply current into Pin 2 and Pin 5 with R_X = 100 k (from Pin 2 to supply) and 45 k pull-up resistor from Pin 6 to supply.
2. An internal zener clamp is provided to protect the device from overvoltage transients on the supply line.
3. The timer current constant is the proportionality constant of the voltage to current converter used to monitor the V_{DS} voltage developed across the FET (from Pin 1 to the supply).
4. The gate voltage will be clamped at approximately 7.0 V above the source voltage whenever the source voltage is less than approximately 1.0 V above ground.

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Figure 2. Supply Current versus Supply Voltage

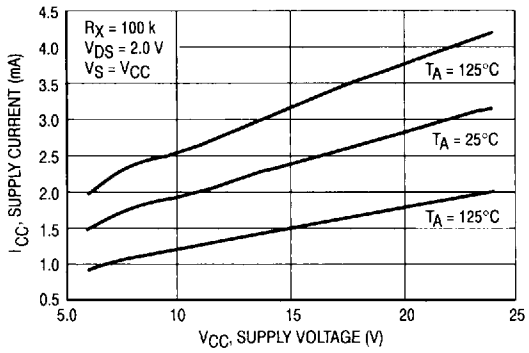

Figure 3. Gate Voltage versus Supply Voltage

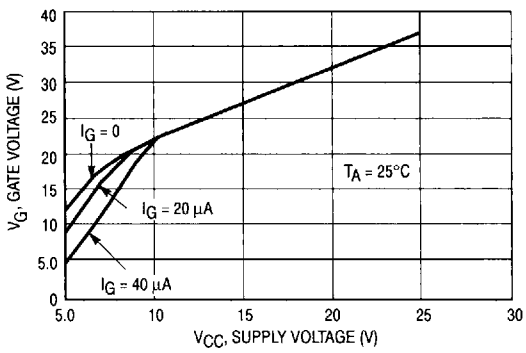

Figure 4. Gate Voltage versus Gate Current

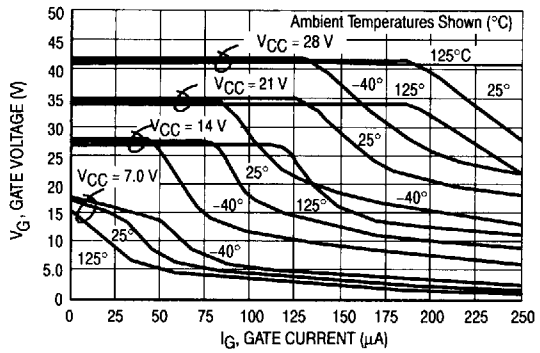

Figure 5. Gate to Source Voltage versus Source Voltage

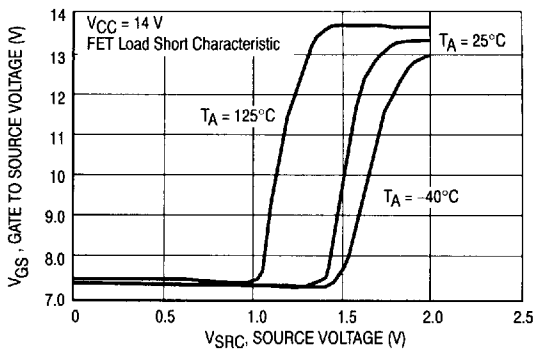

Figure 6. Gate Voltage versus Supply Voltage

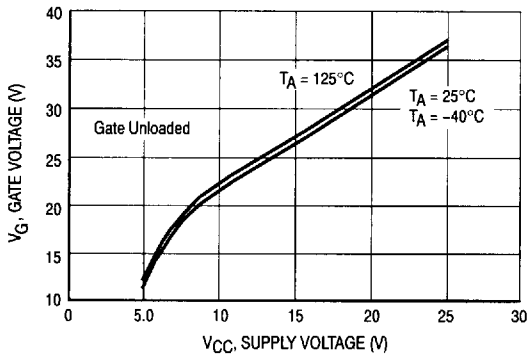

Figure 7. Gate Voltage versus Input Control Voltage

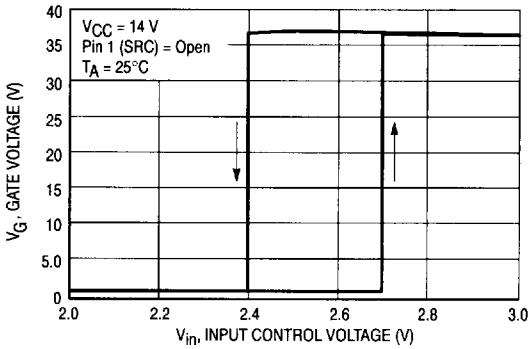

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Figure 8. Input Control Current versus Input Control Voltage

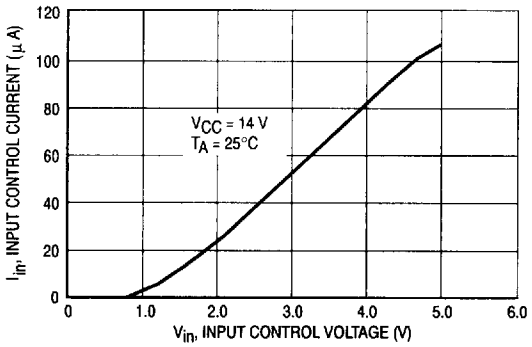

Figure 9. Squaring Constant "K" versus Supply Voltage

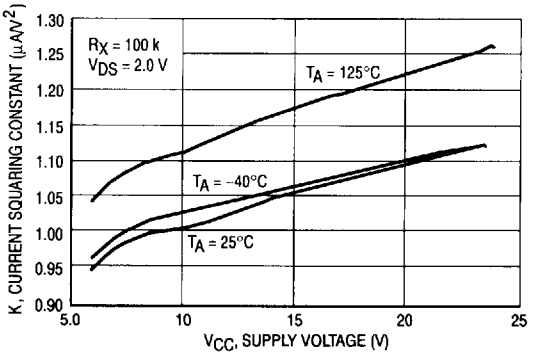

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Figure 10. Timer Current versus Drain to Source Voltage Squared

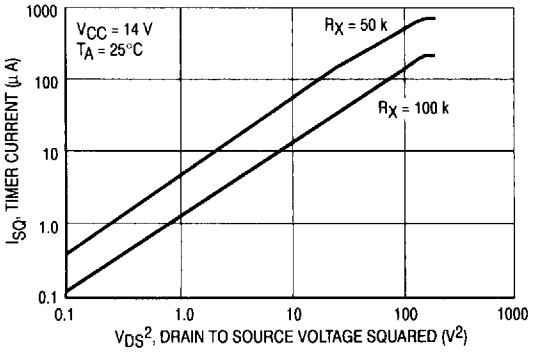

Figure 11. $\overline{\text{Fault}}$ Voltage versus $\overline{\text{Fault}}$ Sink Current

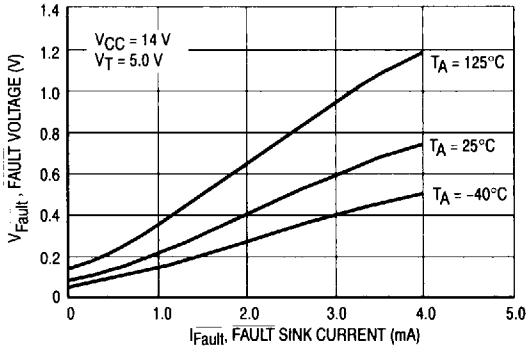

Figure 12. FET Comparison Gate Response

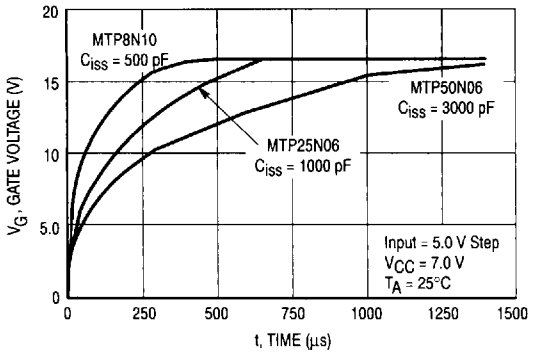

Figure 13. FET Comparison Gate Response

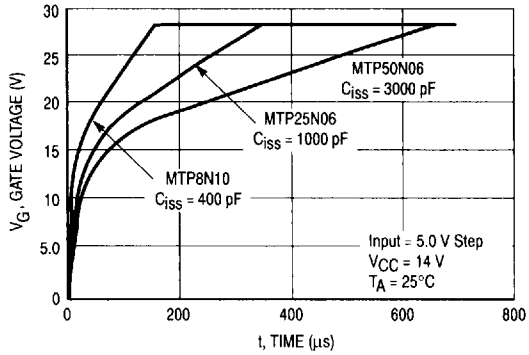

Figure 14. FET Comparison Gate Response

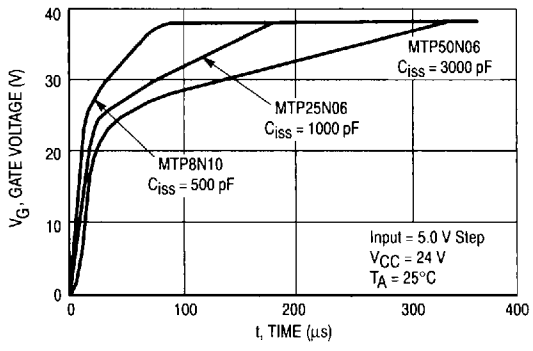

Figure 15. MTP25N06 Gate Response

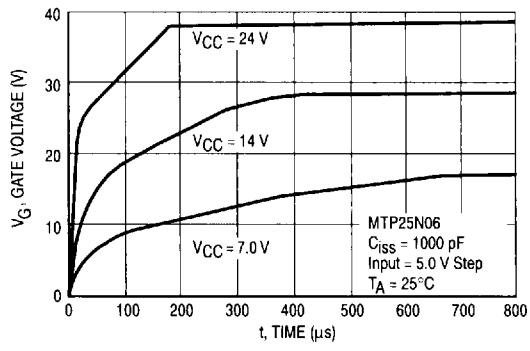

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Figure 16. Timer Lower Threshold Voltage versus Temperature

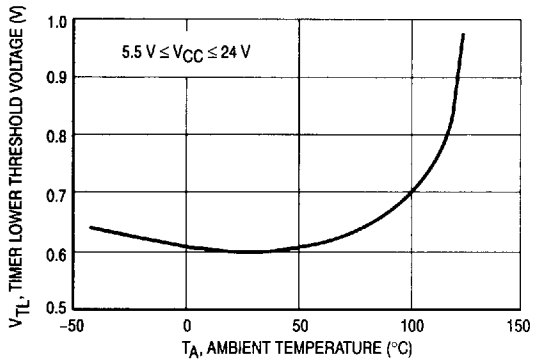

Figure 17. Timer Lower Threshold Voltage versus Supply Voltage

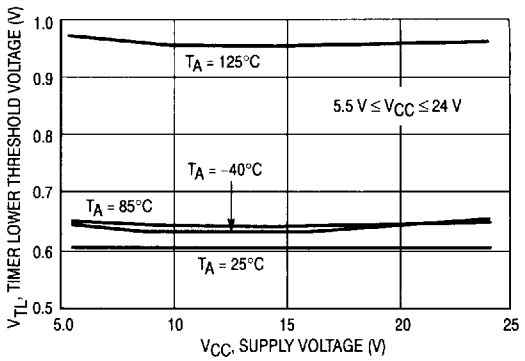

Figure 18. Timer Upper Threshold Voltage versus Temperature

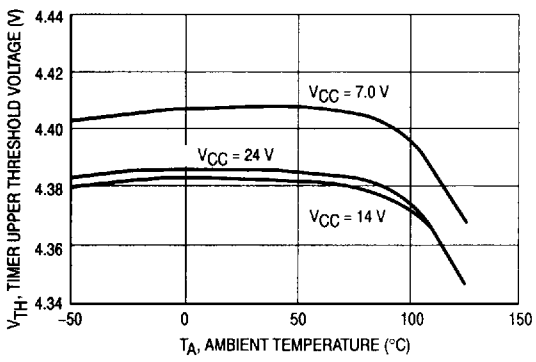

Figure 19. Timer Upper Threshold Voltage versus Supply Voltage

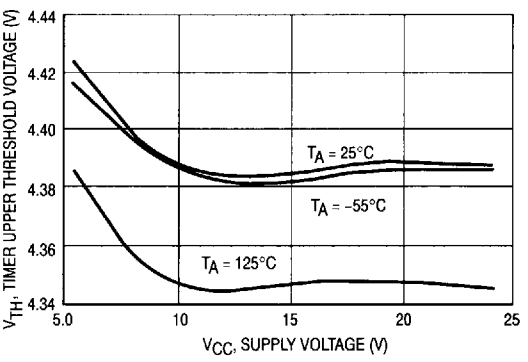

Figure 20. Gate Saturation Voltage versus Gate Current

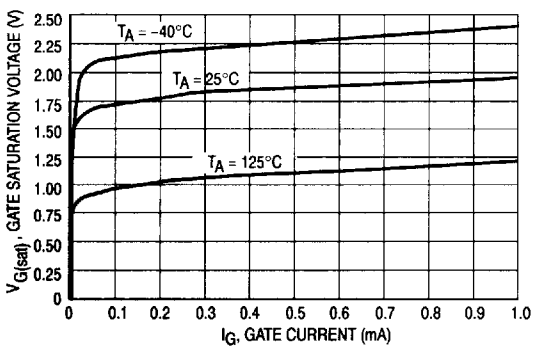

Figure 21. Gate Saturation Voltage versus Gate Current (Expanded Scale)

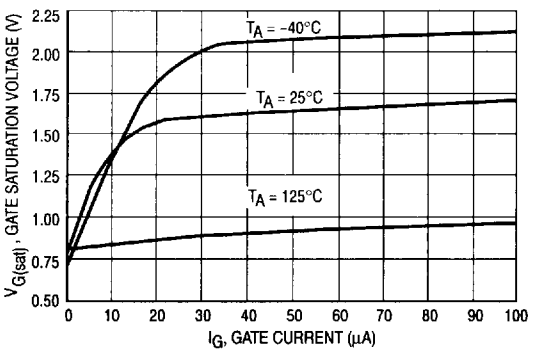

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Figure 22. Gate to Source Voltage versus External R_T Timer Resistor

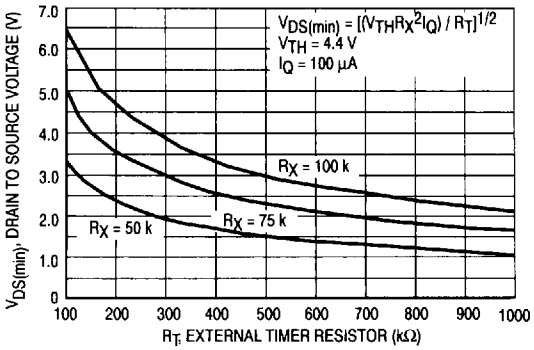


Figure 23. Timer Response versus $V_{DS(min)}/V_{bat}$ Ratio

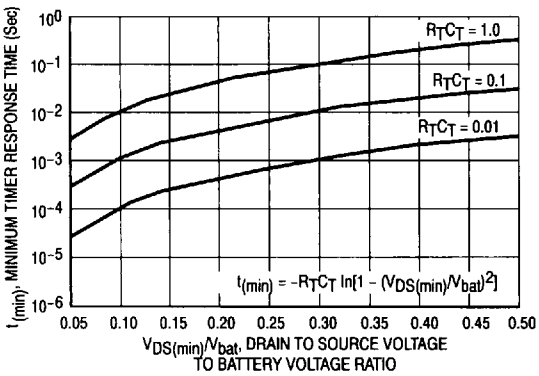
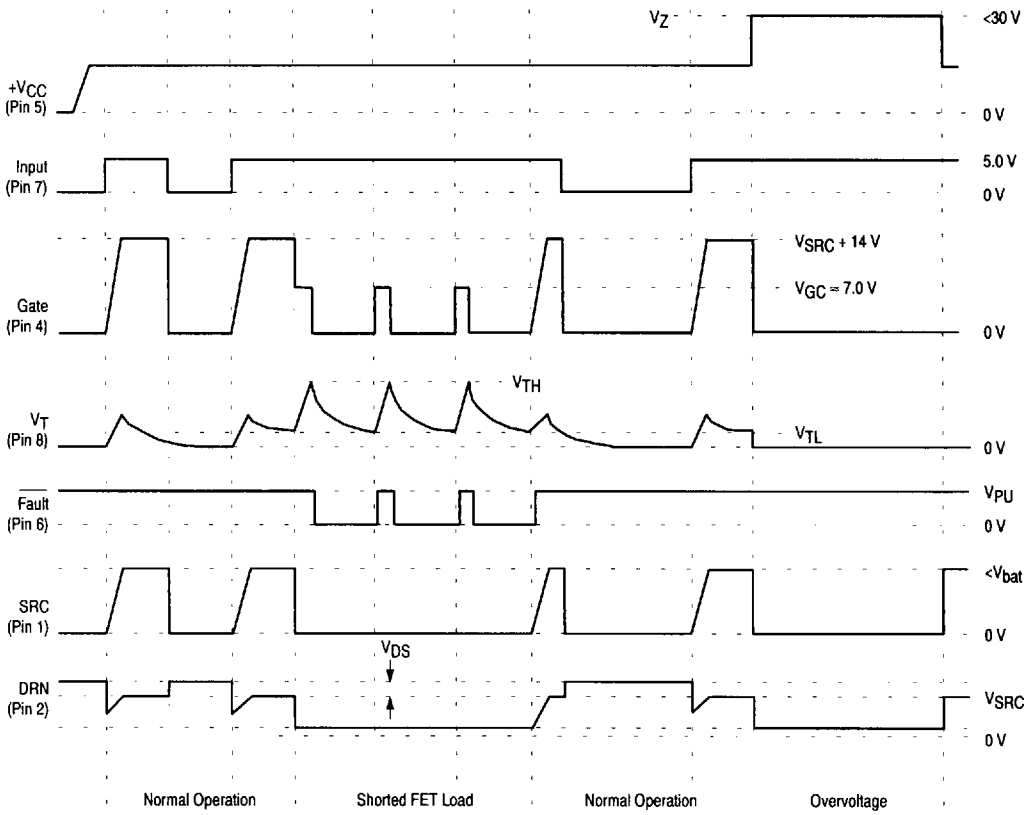


Figure 24. Descriptive Waveform Diagram



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MC33091

FUNCTIONAL DESCRIPTION

Introduction

The MC33091 is designed to drive a wide variety of N-channel TMOS transistors in high side configured, low frequency switching applications. The MC33091 has an internal charge pump to fully enhance the on-state of the TMOS device. The MC33091 protects the TMOS device from shorts to ground and provides a $\overline{\text{Fault}}$ output to report the presence of an over current condition. The few additional external components required allow tailoring of the application's protection level. The protection scheme of the MC33091 uses an externally programmable, nonlinear timer that disables the TMOS device in the event the drain to source voltage exceeds a specified value for a specified duration. Both the value and duration are externally programmable allowing for flexibility in applications.

Pin Description

Figure 1 shows a typical application as well as the internal functional blocks of the MC33091. The discussion to follow references this figure.

Input (Pin 7): The logic levels of the Input are compatible with CMOS logic families. The Input enables the protection and charge pump circuitry. With the Input in a logic low state the MC33091 draws only leakage current of less than 3.0 µA and in this condition the associated TMOS device will be in the off state. When the Input is in a logic high state, the Gate voltage (Pin 4) rise is limited to a maximum of 14 V above SRC (Pin 1), due to an internal clamp diode being used. Under this condition the TMOS device is enhanced full on.

$\overline{\text{Fault}}$ (Pin 6): The $\overline{\text{Fault}}$ output is comprised of an open collector NPN transistor capable of sinking at least 500 µA when the TMOS gate is disabled due to an over current condition. When the TMOS device experiences an over current condition the $\overline{\text{Fault}}$ pin is pulled low.

SRC (Pin 1): The SRC pin senses the TMOS source voltage and is the input to the V_{DS} buffer used in conjunction with the DRN pin in monitoring the drain to source voltage developed across the TMOS device. The purpose of the 1.0 k resistor connected to this pin is to protect the SRC input from over voltage as a result of flyback voltage produced when the TMOS device is used to switch large inductive loads. This resistor can be eliminated when switching noninductive loads.

DRN (Pin 2): The DRN is used in conjunction with the SRC pin and together constitute a V_{DS} monitor of the TMOS drain to source voltage. Feedback from the SRC pin will maintain a voltage across the resistor, (R_X), equal to the V_{DS} voltage developed across the TMOS device. The series resistor, (R_X), connected between the drain of the TMOS device and DRN of the MC33091 is used in conjunction with the feedback buffer and associated PNP transistor to establish a current proportional to the drain to source voltage, (V_{DS}), of the TMOS device. This proportional current, acted upon by the current squaring circuit of the MC33091, is an important part of the TMOS protection scheme.

V_{CC} (Pin 5): The V_{CC} pin supplies operational power to the MC33091. An internal 30 V zener clamp connects to this pin provide over voltage protection of the MC33091. When the zener is activated, the MC33091 disables the TMOS device only for the duration of the overvoltage but the $\overline{\text{Fault}}$ output (Pin 6) does not change logic states. The $\overline{\text{Fault}}$ pin does not go to a logic low state during the over voltage duration since this is not an MC33091 device fault, but an external system fault.

Gate (Pin 4): The Gate pin of the MC33091 is the output of the internal charge pump which controls the TMOS device. The charge pump is a voltage tripler and requires no additional external components for operation. With the Input in a logic low state the charge pump will be turned off. When the Input is pulled to a logic high state, with no load fault existing, the charge pump turns on and pumps the TMOS gate voltage to at least 8.0 V, typically 10 V to 14 V, above V_{CC} over the supply voltage range. An internal zener clamp is incorporated so as to limit the Gate to approximately 14 V above the source so as to prevent rupture of the TMOS gate.

VT (Pin 8): The Timer Pin (V_T) is both an input to the timer window comparators and an output of the current squaring circuit. An external resistor (R_T) and capacitor (C_T) are tied to this node so as to afford programing the characteristics necessary for protection of the TMOS device.

Over Current Protection Timer

The MC33091 protection scheme is based on the ability of the MC33091 to constantly sense the voltage drop developed across the TMOS device. A low voltage drop is indicative of normal TMOS "on" operation while a large voltage drop represents the existence of an over current condition. By monitoring the TMOS drain to source voltage (V_{DS}) the MC33091 is able to detect a shorted load and react to disable the TMOS device. The circuit protection scheme is essentially based on a timer whose rate is dependent on the magnitude of V_{DS}. If the drain to source voltage is large (i.e. $V_{DS} = V_{CC}$), the timer will disable the gate drive very quickly. If V_{DS} is only slightly above the normal operating level, the timer will take much longer to disable the gate drive.

Since the power dissipated in the TMOS device is proportional to V_{DS}^2, low V_{DS} conditions can be tolerated for a longer time than high V_{DS} conditions. To enhance the system application the timer time-out of the MC33091 is inversely proportional to V_{DS}^2. This approach maximizes the TMOS operating range. The timer parameters are completely user programmable through the use of external components affording application usage of a wide variety of TMOS devices. This is intended to model the generation and dissipation of heat within the TMOS device.

The external components R_X, R_T, and C_T determine the timer characteristics. Once enabled, the MC33091 will source a current, (I_{SQ}), from the timer pin that is proportional to V_{DS}^2 such that:

$$I_{SQ} = KV_{DS}^2 \quad (1)$$

where: $K = 1/(R_X^2 I_Q)$

I_Q is an internal current source parameter of the MC33091 that has a nominal value of 100 μA and R_X is the external resistor in series with the drain of the TMOS device that establishes the value of the voltage to current proportionality constant. Since the parallel combination of R_T and C_T appear at the timer pin (V_T), the timer pin voltage, V_T, can be written as:

$$V_T(t) = I_{SQ}R_T[1-e^{-t/(R_TC_T)}] \quad (2)$$

With the Input (Pin 7) in a logic high state and no over current condition existing, the TMOS device will be in the "on" state. If the TMOS device experiences an over current condition, I_{SQ} flowing through R_T will increase causing C_T to charge up, in turn causing the timer voltage, (V_T), to exceed the threshold, (V_{TH}), of the upper comparator. This sets the latch causing the Q output of the latch to go high (and the $\overline{Q}$ output to go low), in turn causing the TMOS gate and $\overline{Fault}$ output (Pin 6) to be pulled low, disabling the TMOS device. Both the current squaring circuit (I_{SQ}) and the charge pump are disabled whenever the Q output of the latch goes low. Using Equation 2, the fault time response for an over current condition can be written as:

$$t = -R_TC_T \ln(1-V_{TH}/I_{SQ}R_T) \quad (3)$$

Using Equation 1 and substituting for ISQ in Equation 3:

$$t = -R_TC_T \ln[1-(V_{TH}R_X^2I_Q)/(V_{DS}^2R_T)] \quad (4)$$

When the timer current (I_{SQ}) is disabled, the attained V_{TH} voltage at Pin 8 decays according to the R_TC_T time constant until the V_{TL} threshold of the lower comparator is reached. At this point the latch is reset and the TMOS gate, charge pump and the current squaring circuit are again enabled, again turning on the TMOS device. The MC33091 will repeatedly duty cycle the TMOS gate in this manner so long as the over current condition exists and the input control signal remains in a high logic state. The $\overline{Fault}$ output (Pin 6) will likewise duty cycle.

Consider the case where in Equation 4 the term $(V_{TH}R_X^2I_Q) / (V_{DS}^2R_T) = 1$ such that the time period is undefined. Solving for V_{DS} for this case yields the *minimum* drain to source voltage necessary which will *not* allow V_T to charge to the V_{TH} threshold of the upper comparator. In other words, the TMOS on-time period is infinite which indicative of *no* TMOS over current condition existing. This minimum drain to source voltage for uninterrupted continuous TMOS operation is:

$$V_{DS(min)} = [(V_{TH}R_X^2I_Q)/R_T]^{1/2} = (V_{TH}/KR_T)^{1/2} \quad (5)$$

Under *normal* operating steady state TMOS "on" conditions, R_X and R_T should be chosen such that the upper comparator threshold voltage is *never* reached. This insures the TMOS device will always be in operation so long as the $V_{DS(min)}$ is not exceeded.

The minimum time required for the capacitor C_T to charge up to upper comparator threshold voltage occurs when the TMOS device experiences maximum current (I_{max}). This will occur when the load, and in turn the source, are shorted to ground resulting in the full battery voltage (V_{bat}) to appear directly across the TMOS device. This condition causes maximum I_{SQ} current to be produced by the current squaring circuit. Under this condition the maximum I_{SQ} current experienced is:

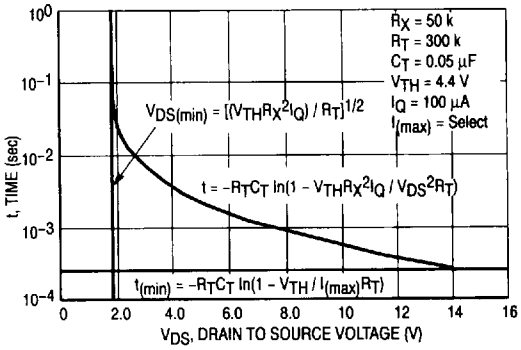
$$I_{SQ(max)} = KV_{bat}^2 = (V_{bat}/R_X)^2/I_Q \quad (6)$$

An expression for the minimum time-out is obtained by substituting I_Q of Equation 6 into Equation 3:

$$t_{(min)} = -R_TC_T \ln[1-V_{TH}/(I_{SQ(max)}R_T)] \quad (7)$$

Equation 4 is shown graphically along with the asymptotic limits imposed by Equations 5 and 7 in Figure 25.

Figure 25. Theoretical Fault Time versus V_{DS}



When driving incandescent lamp loads the minimum timer time-out (the time required for the V_T voltage to reach V_{TH} threshold of the upper comparator) should be set long enough so as to *not* allow the inrush current of incandescent lamp to cause a false trigger, yet short enough to afford the TMOS device survival protection against direct shorts under worst case supply and temperature conditions.

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TMOS Driver Power Dissipation

Under load short conditions, the MC33091 will duty cycle the TMOS gate. The power dissipation in this mode can be significant. For this reason proper heatsinking of the TMOS device is essential as is the selection of compatible external components so as to protect the TMOS device from destruction. In most cases, the heatsink required to handle the TMOS power dissipation under normal operating conditions will be adequate to insure the device survives a short circuit for an indefinite time under worst case conditions.

The MC33091 can protect the TMOS device under a direct load short condition. If the source voltage is less than about 1.5 V above ground, which will normally be the case in the event of a dead short, the MC33091 will clamp the gate to source voltage at 7.0 V. This action will limit the TMOS current and power dissipated under a direct load short condition.

The data sheet for the particular TMOS device being used will normally reveal the current value, $I_{DS(max)}$, to be expected under a dead short condition. TMOS data sheets normally depict graphs of drain current versus drain to source voltage for various gate to source voltages from which the drain current at 7.0 V V_{GS}, $I_{DS(max)}$, can reasonably be approximated. Using this information, the peak TMOS power dissipation under a dead short condition is approximated to be:

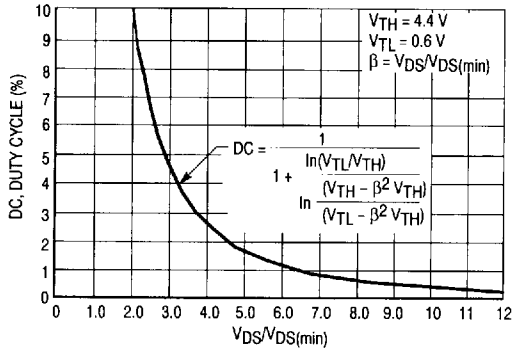
$$P_{D(peak)} = V_{bat(max)} I_{DS(max)} \quad (8)$$

The average power is equal to the peak power dissipation multiplied by the duty cycle (DC):

$$P_{D(avg)} = P_{D(peak)} DC \quad (9)$$

As long as the average power, in Equation 9, is less than the maximum power dissipation of the TMOS device under normal conditions, the short circuit protection scheme of the MC33091 will adequately protect the TMOS device. The duty cycle at which the MC33091 controls the gate can be determined by using Figure 26.

Figure 26. MC33091 Duty Cycle versus V_{DS} / $V_{DS(min)}$



As previously discussed, I_{SQ} is externally dependant on the sensed V_{DS} voltage developed across the TMOS device and R_X in accordance with Equations 1 and 2. At the onset of an overload condition, the voltage across C_T will be less than the V_{TH} threshold voltage of the upper comparator with the TMOS device in an "on" state. I_{SQ} current will increase dramatically and the timing capacitor C_T charges toward V_{TH}. When the voltage on C_T reaches the V_{TH} threshold voltage of the upper comparator, the upper comparator output goes high setting the latch output (Q) high, turning on the open collector NPN transistor and pulling the $\overline{\text{Fault}}$ output low. At the same time, I_{SQ} is switched off allowing C_T to discharge through resistor R_T to V_{TL}, at which time the TMOS device is again switched on. This action is repeated so long as the overload condition exists. The V_{TL} and V_{TH} thresholds are internally set to approximately 0.6 V and 4.4 V respectively. The charge time (t_c) of C_T can be shown as:

$$t_c = -R_T C_T \ln[1-(V_{TH}-V_{TL})/(I_{SQ}R_T-V_{TL})] \quad (10)$$

The discharge time (t_d) of C_T can be shown as:

$$t_d = -R_T C_T \ln(V_{TL}/V_{TH}) \quad (11)$$

The duty cycle is defined as charge time divided by the charge plus discharge time and represented by:

$$DC = t_c/(t_c+t_d) \quad (12)$$

Substituting Equations 10 and 11 into 12: (13)

$$DC = 1/1+\ln(V_{TL}/V_{TH})/\ln\{(V_{TH}-\beta^2 V_{TH})/(V_{TL}-\beta^2 V_{TH})\}$$

where: $\beta = V_{DS}/V_{DS(min)}$

Notice the duty cycle is dependent *only* on the ratio of the drain to source voltage, (V_{DS}), of the TMOS device to the minimum drain to source voltage ($V_{DS(min)}$), allowing uninterrupted continuous TMOS operation as calculated in Equation 5. A graph of Equation 13 is shown in Figure 26 and is valid for any ratio of V_{DS} to $V_{DS(min)}$. Knowing this ratio, the duty cycle can be determined by using Figure 26 or Equation 13 and knowing the duty cycle, the average power dissipation can be calculated by using Equation 9.

If the TMOS device experiences a hard load short to ground a minimum duty cycle will be experienced which can be calculated. When this condition exists, the TMOS device experiences a V_{DS} voltage of V_{bat} which is sensed by the MC33091. The MC33091 very rapidly charges the timing capacitor C_T to V_{TH} shutting down the TMOS device. This condition produces the minimum duty cycle for the specific system conditions. The minimum duty cycle can be calculated for any valid V_{bat} voltage by substituting the value of V_{bat} used for V_{DS} in Equation 13 and solving for the duty cycle.

Knowing the duty cycle and peak power allows determination of the average power as was pointed out in Equation 9. TMOS data sheets specify the maximum allowable junction temperature and thermal resistance, junction to case, at which the device may be operated. Knowing the average power and the device thermal information, proper heatsinking of the TMOS device can be determined.

The duty cycle graph (Figure 26) reveals lower values of $V_{DS(min)}$ produce shorter duty cycles, for a given V_{DS} voltages. The minimum duty cycle, being limited to the case where $V_{DS} = V_{bat}$, increases as higher values of V_{bat} are used.

APPLICATION

The following design approach will simplify application of the MC33091 and will insure the components chosen to be optimal for a specific application.

1. Characterize the load impedance and determine the maximum load current possible for the load supply voltage used.

2. Select a TMOS device capable of handling the maximum load current. Though the MC33091 will equally drive our competitors products, it is hoped you will select one of the many TMOS devices listed in Motorola's *TMOS Power MOSFET Selector Guide/Cross Reference*, (SG56/D).

3. Determine the maximum steady state V_{DS} voltage the TMOS device will experience under *normal* operating conditions. Typically, this is the maximum load current multiplied by the specified $r_{DS(on)}$ of the TMOS device. Junction temperature considerations should be taken into account for the $r_{DS(on)}$ value since it is significantly temperature dependent. Normally, TMOS data sheets depict the affect of junction temperature on $r_{DS(on)}$ and an $r_{DS(on)}$ value at some considered maximum junction temperature should be used. Various graphs relating to $r_{DS(on)}$ are depicted in Motorola TMOS data sheets. Though Motorola TMOS devices typically specify a maximum allowable junction temperature of 150°C, in a practical sense, the user should strive to keep junction temperature as low as possible so as to enhance the applications long term reliability. The maximum steady state V_{DS} voltage the TMOS device will experience under *normal* operating conditions is thus:

$$V_{DS(norm)} = I_{L(max)} r_{DS(on)} \quad (14)$$

4. Calculate the maximum power dissipation of the TMOS device under *normal* operating conditions:

$$P_{D(max)} = V_{DS(on)} I_{L(max)} \quad (15)$$

5. The calculated maximum power dissipation of the TMOS device dictates the required thermal impedance for the application. Knowing this, the selection of an appropriate heatsink to maintain the junction temperature below the maximum specified by the TMOS manufacture for operation can be made. The required overall thermal impedance is:

$$TR_{JA} = (T_{J(max)} - T_{A(max)})/P_{D(max)} \quad (16)$$

Where $T_{J(max)}$, the maximum allowable junction temperature, is found on the TMOS data sheet and $T_{A(max)}$, the maximum ambient temperature, is dictated by the application itself.

6. The thermal resistance (TR_{JA}), represents the maximum overall or total thermal resistance, from junction to the surrounding ambient, allowable to insure the TMOS manufactures maximum junction temperature will not be exceeded. In general, this overall thermal resistance can be considered as being made up of several separate minor thermal resistance interfaces comprised of TR_{JC}, TR_{CS}, and TR_{SA} such that:

$$TR_{JA} = TR_{JC} + TR_{CS} + TR_{SA} \quad (17)$$

Where TR_{JC}, TR_{CS}, and TR_{SA} represent the junction-to-case, case-to-heatsink, and heatsink-to-ambient thermal resistances respectively. TR_{CS} and TR_{SA} are the only parameters the device user can influence.

The case-to-heatsink thermal resistance (TR_{CS}) is material dependent and can be expressed as:

$$TR_{CS} = \rho \bullet t/A \quad (18)$$

Where "ρ" is the thermal resistivity of the heatsink material (expressed in °C/W unit thickness), "t" is the thickness of heatsink material, and "A" is the contact area of the case to heatsink. Heatsink manufactures specify the value of TR_{CS} for standard heatsinks. For nonstandard heatsinks, the user is required to calculate TR_{CS} using some form of the basic Equation 18.

The required heatsink-to-ambient thermal resistance (TR_{SA}) can easily be calculated once the terms of Equation 17 are known. Substituting TR_{JA} of Equation 16 into Equation 17 and solving for TR_{SA} produces:

$$TR_{SA} = (T_{J(max)} - T_{A(max)})/P_{D(max)} - (TR_{JC} + TR_{CS}) \quad (19)$$

Consulting the heatsink manufactures catalog will provide TR_{CS} information for various heatsinks under various mounting conditions so as to allow easy calculation of TR_{SA} in units of °C/W (or when multiplied by the power dissipation produces the heatsink mounting surface temperature rise). Furthermore, heatsink manufactures typically specify for various heatsinks, heatsink efficiency in the form of mounting surface temperature rise above the ambient conditions for various power dissipation levels. The user should insure that the heatsink selected will provide a surface temperature rise somewhat less than the maximum capability of the heatsink so as to insure the device junction temperature will not be exceeded. The user should consult the heatsink manufacturers catalog for this information.

7. Set the value of $V_{DS(min)}$ to something greater than the *normal operating* drain to source voltage, $V_{DS(norm)}$, the TMOS device will experience as calculated in Step 3 above (Equation 14). From a practical standpoint, a value twice the $V_{DS(norm)}$ expected under normal operation will prove to be a good starting point for $V_{DS(min)}$.

8. Select a value of R_T less than 1.0 MΩ for minimal timing error whose value is compatible with R_X, (R_X will be selected in Step 9 below). A recommended starting value to use for R_T would be 470 k. The consideration here is that the input impedance of the threshold comparators are approximately 10 MΩ and if R_T values greater than 1.0 MΩ are used, significant timing errors may be experienced as a result of input bias current variations of the threshold comparators.

9. Select a value of R_X which is compatible with R_T. The value of R_X should be between 50 k and 100 k. Recall in Equation 5 that $V_{DS(min)}$ was determined by the combined selection of R_X and R_T. Low values of R_X will give large values for K ($K = 4.0\ \mu A/V^2$ for R_X = 50 k) causing I_{SQ} to be very sensitive to V_{DS} variations (see Equation 1). This is desirable if a minimum V_{DS} trip point is needed in the 1.0 V range since small V_{DS} values will generate measurable currents. However, at high V_{DS} values, TMOS device currents become excessively large and the current squaring function begins to deviate slightly from the predicted value due to high level injection effects occurring in the output PNP of the current squaring circuit. These effects can be seen when I_{SQ} exceeds several hundred microamps.

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10. Calculate the shorted load average power dissipation for the application using Equations 8 and 9. This involves determining the peak shorted load power dissipation of the TMOS device and gate duty cycle. The duty cycle is based on $V_{DS(min)}$, the value of V_{DS} under shorted conditions (i.e. $V_{bat(max)}$).

11. The calculated shorted load average power dissipation of Step 10 should be less than the maximum power dissipation under *normal* operating conditions calculated in Step 4. If this is not the case, there are two options.

Option one is to reduce the thermal resistance of the TMOS device heatsink, in other words, use a larger or better heatsink. This though, is not always practical to do particularly if restricted by size.

Option two is to set $V_{DS(min)}$ to the lowest practical value. If for instance $V_{DS(min)}$ is set to 4.0 V when only 2.0 V are needed, the short circuit duty cycle will be over twice as large, resulting in double the TMOS device power dissipated. Keeping $V_{DS(min)}$ to a minimum, reduces the shorted load average power.

12. Choose a value of C_T. The value of C_T can be determined either by trial and error or by characterizing the V_{DS} waveform for the load and selecting a capacitor value that generates a minimum fault time curve (see Equation 4) that encompasses the V_{DS} versus time waveform. The value of C_T has *no* effect on the duty cycle itself as was pointed out earlier. See Figure 23 for a graphical selection of C_T.

Inductive Loads

The TMOS device is turned off by pulling the gate to near ground potential. Turning off an inductive load will cause the source of the TMOS device to go below ground due to flyback voltage to the point where the TMOS device may become biased on again allowing the inductive energy to be dissipated through the load. There is an internal 14 V zener diode clamp from the gate to source pin which will limit how far the source pin can be pulled below ground. For high inductive loads, it may be necessary to have an external 10 k current limiting resistor in series with the source pin to limit the clamp current in the event the source pin is pulled more than 14 V below ground.

Transient Faults

The MC33091 is not able to withstand automotive voltage transients directly. However, by correctly sizing resistor R_S and capacitor C_S, the MC33091 can withstand load dump and other automotive type transients. The V_{CC} voltage is clamped at approximately 30 V through the use of an internal zener diode.

Under reverse battery conditions, the load will be energized in reverse due to the parasitic body diode inherent in the TMOS device. Under this condition, the drain is grounded and the MC33091 clamps the gate at 0.7 V below the battery potential. This turns the TMOS device on in reverse and minimizes the voltage across the TMOS device resulting in minimal power dissipation. Neither the MC33091 nor the TMOS device will be damaged under such a condition. In addition, if the load can tolerate a reverse polarity, the load will not be damaged. Some sensitive applications may not tolerate a reverse polarity load condition with reverse battery polarity.

There is no protection of the TMOS device during a reverse battery condition if the load itself is already shorted to ground. The MC33091 will not incur damage under this specialized reverse battery condition but the TMOS device may be damaged since there could be significant energy available from the battery to be dissipated in the TMOS device.

The MC33091 will withstand a maximum V_{CC} voltage of 28 V and with the proper TMOS device used, the system can withstand a double battery condition.

Figure 32 depicts a method of protecting the FET from positive transient voltages in excess of the rated FET breakdown voltage. The zener voltage, in this case, should be less than the FET breakdown voltage. The diode D is necessary where reverse battery protection is required to protect the gate of the FET.

EMI Concern

The gate capacitance and thus the size of the TMOS device used will determine the turn-on and turn-off times experienced. In a practical sense, smaller TMOS devices have smaller gate capacitances and give rise to higher slew rates. By way of example, the slew rate of an MPT50N06 TMOS device might be of the order of 7.5 µs while that of an MPT8N10 is 23 µs (see Figure 13). The slew rate, or speed of turn-on or turn-off can be calculated by assuming the charge pump to supply approximately 100 µA over the time the gate capacitance will transition a V_{GS} voltage of 0 V to 10 V. In reality, the V_{GS} voltage will be greater than 10 V but the additional increase in TMOS drain current will be minimal for V_{GS} voltages greater than 10 V.

Sizing of the charge pump current is such that slew rate need not be of concern in all but the most critical of applications. Where limiting of EMI is of concern, the charge pump of the MC33091 may be slew rate limited by adding an external feedback capacitor from the gate to source of the TMOS device for slow down adjustment of both turn-on and turn-off times (see Figure 29). Figures 27 through 31 depict various methods of modifying the turn-on or turn-off times.

Figure 31 depicts a method of using only six external components to decrease turn-off time and clamp the flyback voltage associated with inductive loads. $V_{GS(th)}$ used in the critical component selection criteria refers to the gate to source threshold voltage of the FET used in the application.

Caution should be exercised when slowing down the switching transition time since doing so can greatly increase the average power dissipation of the TMOS device. The resulting increase in power dissipation should be taken into account when selecting the R_TC_T time constant values in order to protect the TMOS device from any over current condition.

Figure 27. Slow Down FET Turn-On

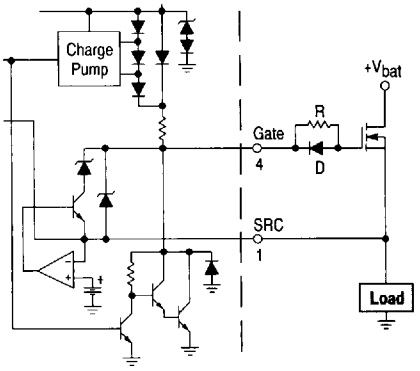


Figure 28. Slow Down FET Turn-Off

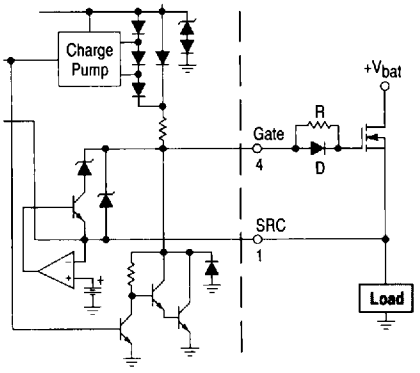


Figure 29. Slow Down Turn-On and Turn-Off of FET

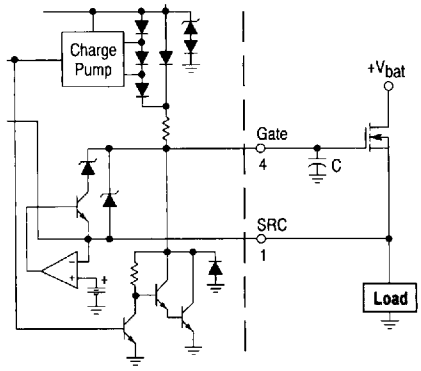


Figure 30. Independent Slow Down Adjustment of FET Turn-On and Turn-Off

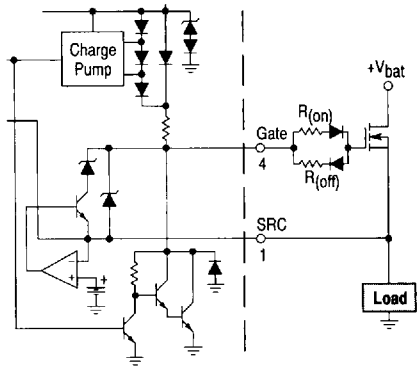


Figure 31. Decreased FET Turn-Off Time With Inductive Flyback Voltage Clamp

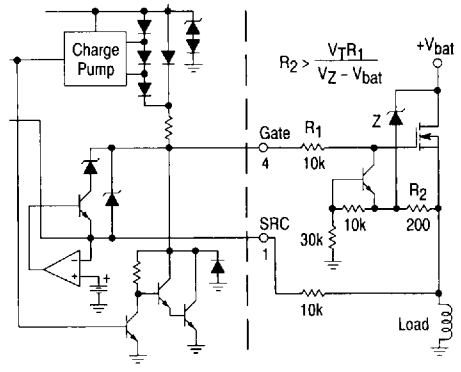
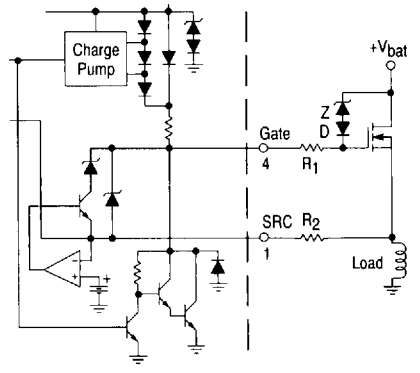


Figure 32. Overvoltage Protection of FET



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