TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

16,777,216-WORD BY 72-BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM72V1615BTG is a 16,777,216-word by 72-bit dynamic RAM module consisting of 18 TC5165405BFT DRAMs on a printed circuit board. This module is optimized for applications which require high density and high capacity, such as computer main memory and image memory, and also for applications which require compactness.

FEATURES

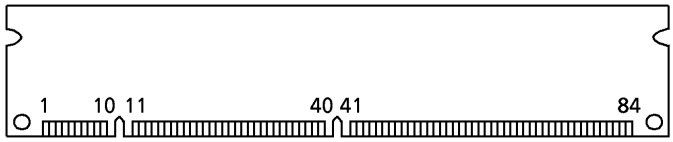
- 16,777,216-word by 72-bit organization
- Fast access and cycle times

	-4	-5
t_{RAC} $\overline{RAS}$ Access Time	40 ns	50 ns
t_{AA} Column Address Access Time	25 ns	30 ns
t_{CAC} $\overline{CAS}$ Access Time	16 ns	18 ns
t_{RC} Cycle Time	69 ns	84 ns
t_{HPC} Hyper Page Mode Cycle Time	16 ns	20 ns

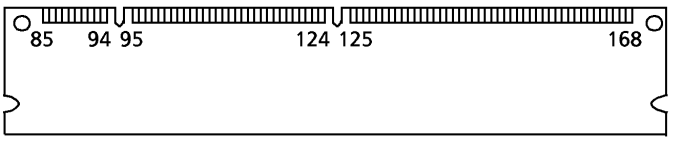
- Single power supply of 3.3 V ± 5%
- Low power dissipation (max)
  - Operating 7530 mW (40-ns type)
    6281 mW (50-ns type)
  - Standby 66.0 mW (both devices)
- Read-Modify-Write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-Only refresh, Hidden refresh, EDO (Hyper Page mode) and Test mode capability
- All inputs and outputs LVTTL-compatible
- 4096 refresh cycles per 64 ms
- Package: 168-pin TSOP Gold contacts

PIN ASSIGNMENT

FRONT



BACK



PIN NAMES

B0,A0 to 11	Address Inputs
DQ0 to 71	Data Inputs/Outputs
$\overline{RAS}$0,2	Row Address Strobe
$\overline{CAS}$0,4	Column Address Strobe
$\overline{WE}$0,2	Read / Write Input
$\overline{OE}$0,2	Output Enable
V_{CC}	Power (+3.3 V)
V_{SS}	Ground
PD0 to 7	Presence Detect Pin
ID0,1	ID bit
NC	No Connection

	-4	-5
PD0	H	H
PD1	H	H
PD2	H	H
PD3	H	H
PD4	H	H
PD5	H	L
PD6	L	L
PD7	L	L
ID0	V_{SS}	V_{SS}
ID1	V_{SS}	V_{SS}

Note: H: High Level (buffered)
L : Low Level (buffered)

1	V_{SS}	85	V_{SS}	18	V_{CC}	102	V_{CC}	35	A4	119	A5	52	DQ18	136	DQ54	69	DQ28	153	DQ64
2	DQ0	86	DQ36	19	DQ14	103	DQ50	36	A6	120	A7	53	DQ19	137	DQ55	70	DQ29	154	DQ65
3	DQ1	87	DQ37	20	DQ15	104	DQ51	37	A8	121	A9	54	V_{SS}	138	V_{SS}	71	DQ30	155	DQ66
4	DQ2	88	DQ38	21	DQ16	105	DQ52	38	A10	122	A11	55	DQ20	139	DQ56	72	DQ31	156	DQ67
5	DQ3	89	DQ39	22	DQ17	106	DQ53	39	NC	123	NC	56	DQ21	140	DQ57	73	V_{CC}	157	V_{CC}
6	V_{CC}	90	V_{CC}	23	V_{SS}	107	V_{SS}	40	V_{CC}	124	V_{CC}	57	DQ22	141	DQ58	74	DQ32	158	DQ68
7	DQ4	91	DQ40	24	NC	108	NC	41	NC	125	NC	58	DQ23	142	DQ59	75	DQ33	159	DQ69
8	DQ5	92	DQ41	25	NC	109	NC	42	NC	126	B0	59	V_{CC}	143	V_{CC}	76	DQ34	160	DQ70
9	DQ6	93	DQ42	26	V_{CC}	110	V_{CC}	43	V_{SS}	127	V_{SS}	60	DQ24	144	DQ60	77	DQ35	161	DQ71
10	DQ7	94	DQ43	27	$\overline{WE}$0	111	NC	44	$\overline{OE}$2	128	NC	61	NC	145	NC	78	V_{SS}	162	V_{SS}
11	DQ8	95	DQ44	28	$\overline{CAS}$0	112	NC	45	$\overline{RAS}$2	129	NC	62	NC	146	NC	79	PD0	163	PD1
12	V_{SS}	96	V_{SS}	29	NC	113	NC	46	$\overline{CAS}$4	130	NC	63	NC	147	NC	80	PD2	164	PD3
13	DQ9	97	DQ45	30	$\overline{RAS}$0	114	NC	47	NC	131	NC	64	NC	148	NC	81	PD4	165	PD5
14	DQ10	98	DQ46	31	$\overline{OE}$0	115	NC	48	$\overline{WE}$2	132	$\overline{PDE}$	65	DQ25	149	DQ61	82	PD6	166	PD7
15	DQ11	99	DQ47	32	V_{SS}	116	V_{SS}	49	V_{CC}	133	V_{CC}	66	DQ26	150	DQ62	83	ID0	167	ID1
16	DQ12	100	DQ48	33	A0	117	A1	50	NC	134	NC	67	DQ27	151	DQ63	84	V_{CC}	168	V_{CC}
17	DQ13	101	DQ49	34	A2	118	A3	51	NC	135	NC	68	V_{SS}	152	V_{SS}				

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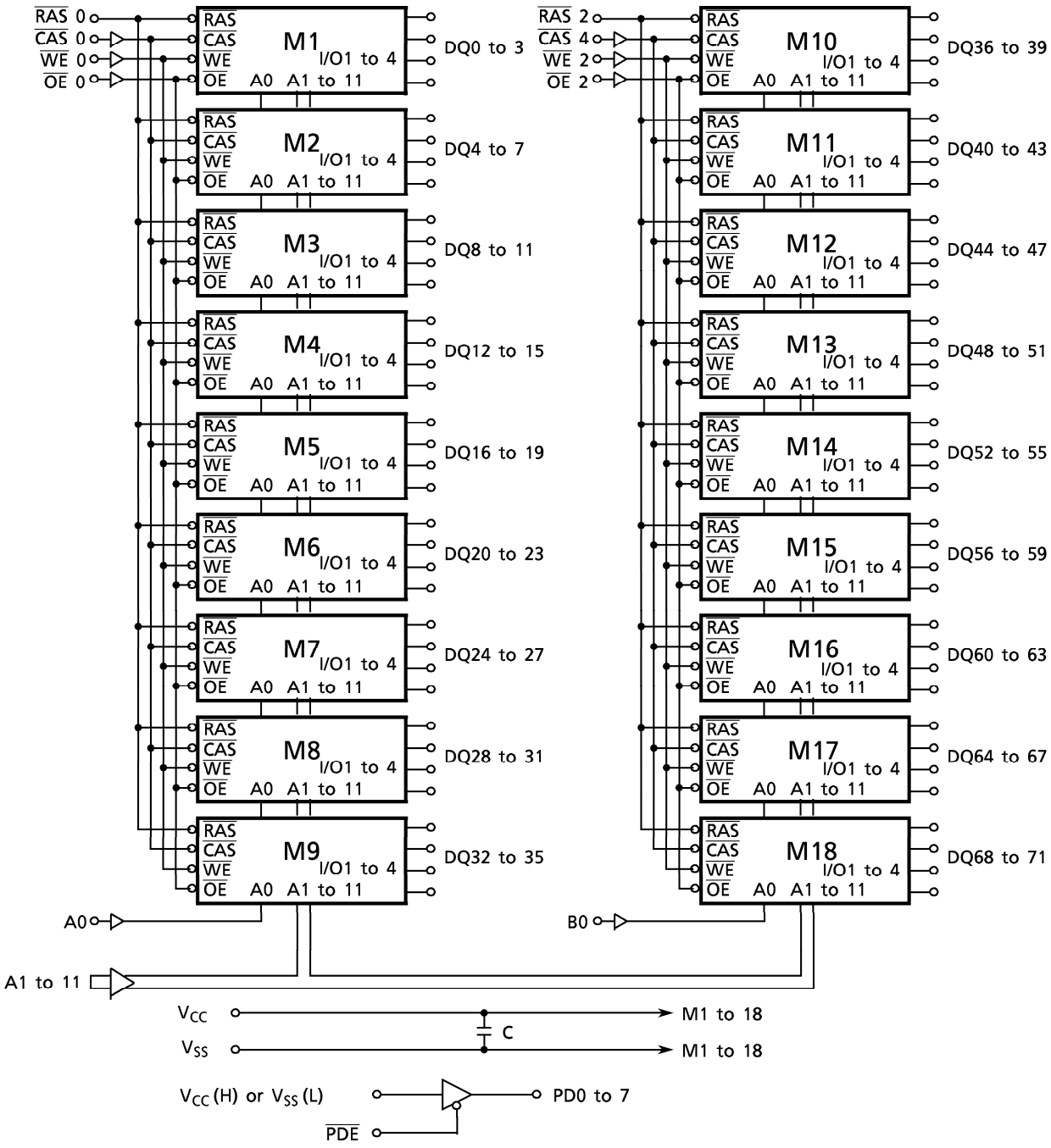
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	– 0.3 to V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	– 0.3 to V_{CC} + 0.3	V	1
V_{CC}	Power Supply Voltage	– 0.3 to 4.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1
T_{STG}	Storage Temperature	– 55 to 125	°C	1
P_D	Power Dissipation	8.3	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	3.13	3.3	3.47	V	2
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 0.3*	V	2
V_{IL}	Input Low Voltage	– 0.3**	–	0.8	V	2

* V_{CC} + 1.2 V at pulse width ≦ 20 ns (pulse width is measured at V_{CC})

** –1.2 V at pulse width ≦ 20 ns (pulse width is measured at V_{SS})

CAPACITANCE (V_{CC} = 3.3 V ± 5%, f = 1 MHz, Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (B0, A0 to 11)	–	T.B.D.	pF
C_{I2}	Input Capacitance ($\overline{WE}$0,2)	–	T.B.D.	pF
C_{I3}	Input Capacitance ($\overline{RAS}$0,2)	–	T.B.D.	pF
C_{I4}	Input Capacitance ($\overline{CAS}$0,4)	–	T.B.D.	pF
C_{I5}	Input Capacitance ($\overline{OE}$0,2)	–	T.B.D.	pF
C_{I6}	Input Capacitance ($\overline{PDE}$)	–	T.B.D.	pF
C_{DQ}	I/O Capacitance (DQ0 to 71)	–	T.B.D.	pF

DC CHARACTERISTICS (V_{CC} = 3.3 V ± 5%, Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	THMxxxxxx-4	–	2170	mA	3, 4
		THMxxxxxx-5	–	1810		5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	28	mA	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	THMxxxxxx-4	–	2170	mA	3, 5
		THMxxxxxx-5	–	1810		
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, Address Cycling: t_{HPC} = t_{HPC} min)	THMxxxxxx-4	–	1630	mA	3, 4
		THMxxxxxx-5	–	1360		5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		–	19	mA	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min)	THMxxxxxx-4	–	2170	mA	3, 5
		THMxxxxxx-5	–	1810		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, Any Input (0 V ≦ V_{IN} ≦ V_{CC}, All Other Pins Not under Test = 0 V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, 0 V ≦ V_{OUT} ≦ V_{CC})		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output H Level Voltage (I_{OUT} = – 2 mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output L Level Voltage (I_{OUT} = 2 mA)		–	0.4	V	

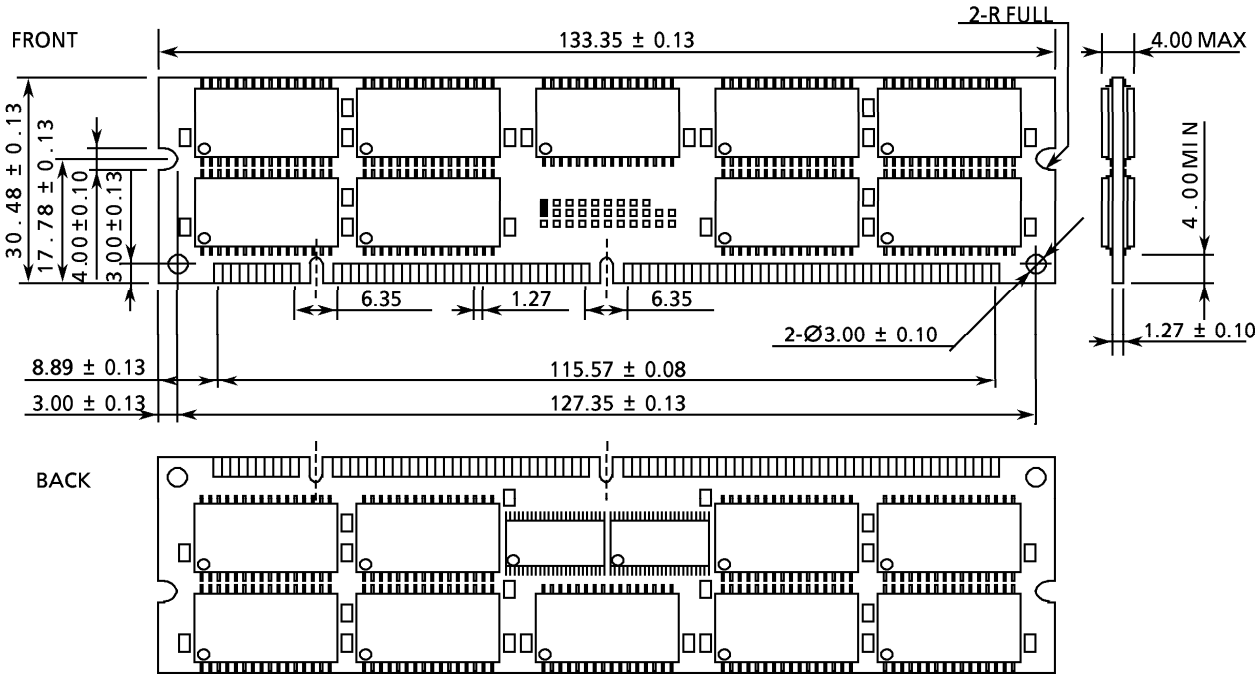
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 5%, Ta = 0° to 70°C)

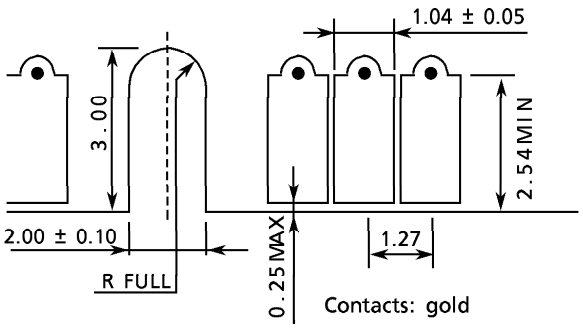
Please refer to DRAM MODULE AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No. 45

PACKAGE DIMENSIONS (THM72 V1615BTG)

Unit: mm



CONTACT DIMENSIONS



Weight: 23.8g (typ.)

DRAM MODULE
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.45

TC5164405BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5165405BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5164805BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5165805BJ/BFT/BJS/BFTS (BUFFER) USING MODULE
TC5164165BFT/BFTS (BUFFER) USING MODULE
TC5165165BFT/BFTS (BUFFER) USING MODULE

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	-40		-50		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	69	–	84	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	102	–	121	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	40	–	50	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	16	–	18	ns	9, 14
t_{AA}	Access Time from Column Address	–	25	–	30	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	27	–	33	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	16	0	18	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	25	–	30	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	40	10,000	50	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	11	–	13	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Hyper Page Mode)	27	–	33	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	30	–	35	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	6	10,000	8	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	24	12	32	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	8	15	10	20	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	6	–	8	–	ns	
t_{ASR}	Row Address Set-Up Time	5	–	5	–	ns	
t_{RAH}	Row Address Hold Time	6	–	8	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	6	–	8	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	–	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	6	–	8	–	ns	
t_{WP}	Write Command Pulse Width	6	–	8	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	11	–	13	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	6	–	8	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	11	–	13	–	ns	12

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	-40		-50		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{REF}	Refresh Period	–	64	–	64	ms	
t_{REF}	Refresh Period (Self Refresh)	–	128	–	128	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	36	–	40	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	–	72	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	40	–	50	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	47	–	55	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	11	–	13	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	16	–	18	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	16	–	18	–	ns	
t_{OLZ}	$\overline{OE}$ to output in Low-Z	0	–	0	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	16	0	18	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	6	–	8	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RNCD}	$\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode)	40	–	50	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	16	–	20	–	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	47	–	57	–	ns	
t_{COH}	Output Data Hold Time	5	–	5	–	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	11	0	13	ns	10, 16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	16	0	18	ns	10
t_{WED}	$\overline{WE}$ to Data Delay	16	–	18	–	ns	
t_{OE}	$\overline{OE}$ Pulse Width	11	–	13	–	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	6	–	8	–	ns	
t_{CPO}	$\overline{CAS}$ to $\overline{OE}$ Precharge Time	5	–	5	–	ns	
t_{OCH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$	6	–	8	–	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	100	–	100	–	μs	
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self refresh)	69	–	84	–	ns	
t_{CHS}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self refresh)	-50	–	-50	–	ns	
t_{PD}	$\overline{PDE}$ to Presence Detect Data in Low-Z	–	10	–	10	ns	
t_{PDOFF}	Presence Detect Data turn off Delay Time from $\overline{PDE}$	1	–	1	–	ns	

NOTES:

1. Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on the cycle rate.
4. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while $\overline{RAS}=V_{IL}$. In the case of I_{CC4}, it can be changed once at most during a Hyper Page Mode cycle (t_{HPC}).
6. An initial pause of 200μs is required after power-up followed by a minimum of eight $\overline{RAS}$-Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles instead of eight $\overline{RAS}$-Only refresh cycles is required.
7. AC measurements assume $t_T=2$ns.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the V_{IH} and V_{IL} levels.
9. This is measured with a load equivalent to 100pF at V_{OH} = 2.0V (I_{OUT} = −2mA), V_{OL} = 0.8V (I_{OUT} = 2mA).
10. t_{OFF} (max), t_{OEZ} (max), t_{REZ} (max) and t_{WEZ} (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of $\overline{CAS}$ in Early Write cycles and to the leading edge of $\overline{WE}$ in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then the access time is determined by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then the access time is determined by t_{AA}.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the output goes open circuit when $\overline{CAS}$ goes high (t_{OFF}).
    If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the output goes open circuit when $\overline{RAS}$ goes high (t_{REZ}).

DATA-OUT HI-Z CONTROL LOGIC

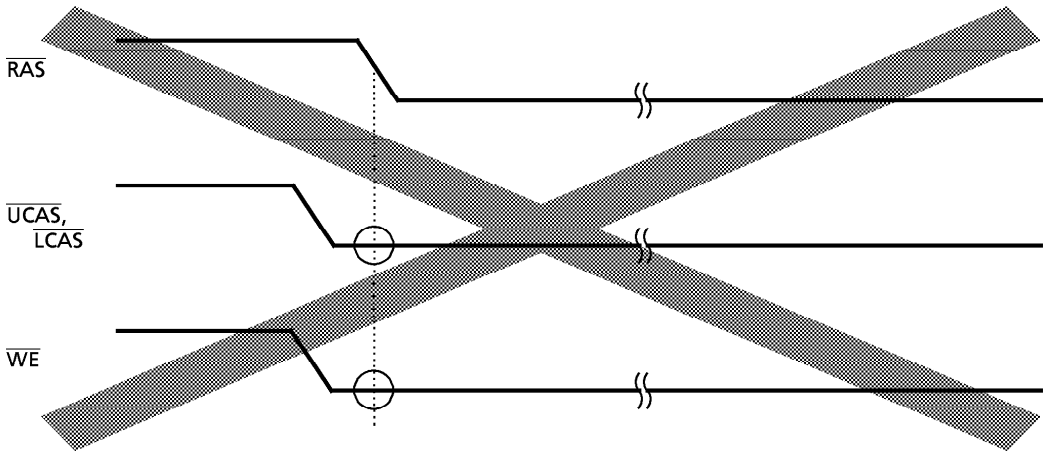
$\overline{RAS}$	$\overline{UCAS}$, $\overline{LCAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
H	↗	L	H	t_{OFF}
↗	H	L	H	t_{REZ}
L	L	↗	H	t_{OEZ}
L	H	L	↘	t_{WEZ}

DATA-OUT LO-Z CONTROL LOGIC

$\overline{RAS}$	$\overline{UCAS}$, $\overline{LCAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
L	↘	L	H	t_{CLZ}
L	L	↘	H	t_{OLZ}
L	L	↗↘	H	t_{OLZ}

CAUTION

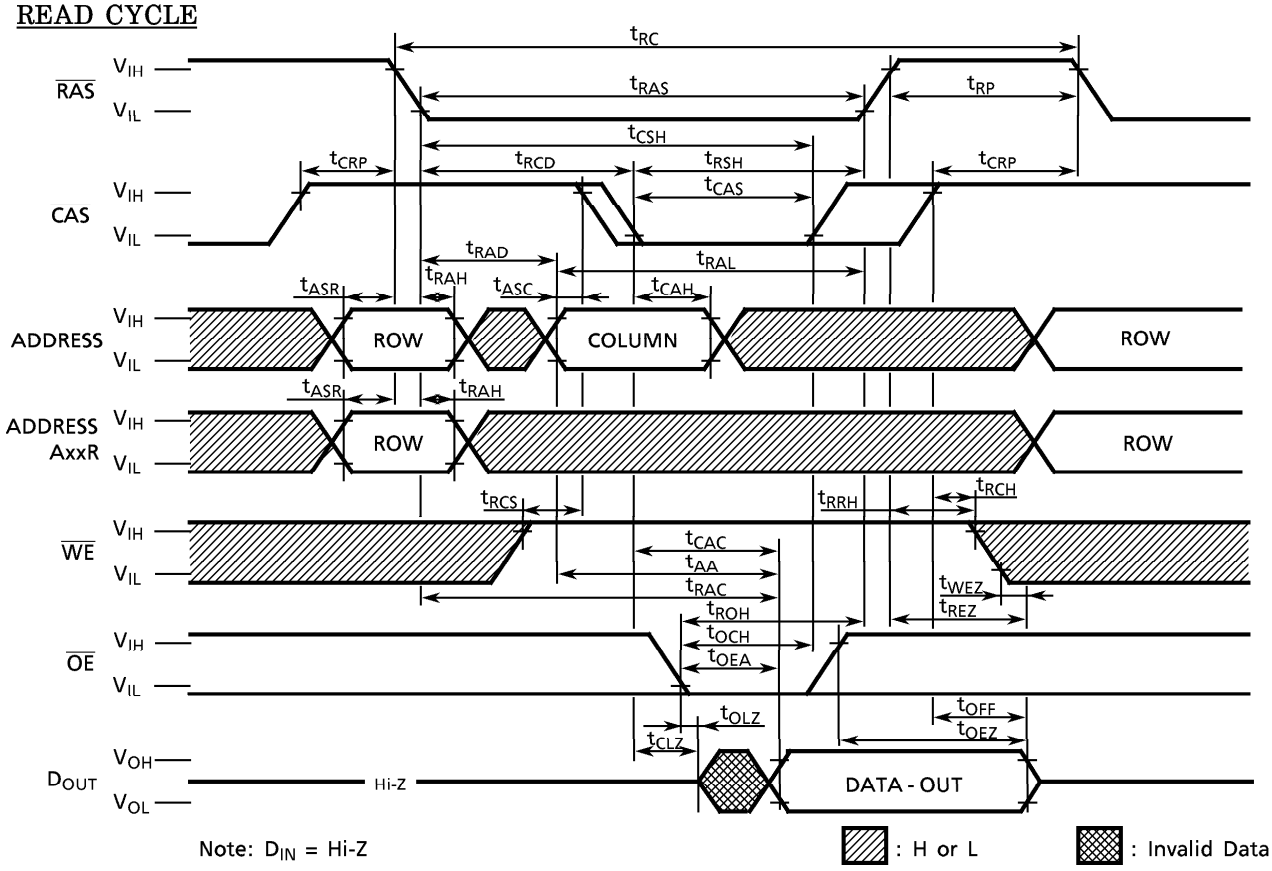
The WCBR ($\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.



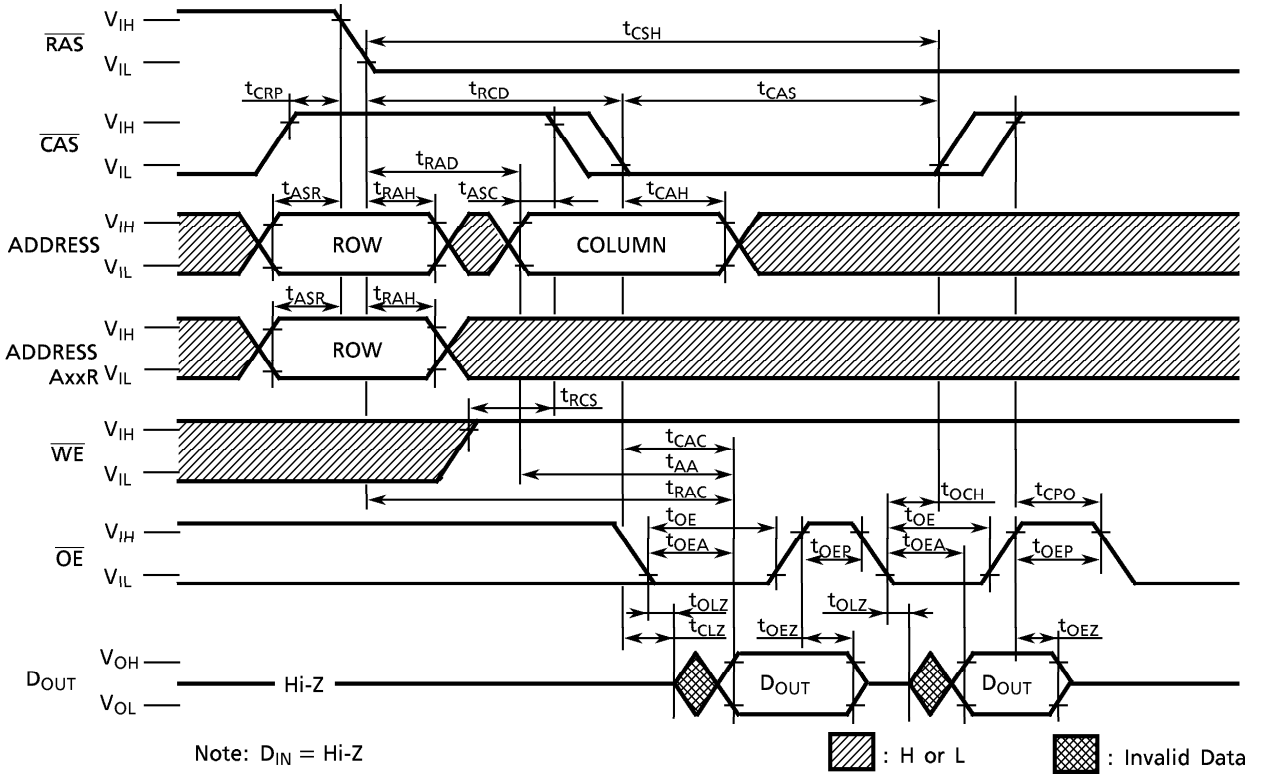
WCBR timing

TIMING DIAGRAMS

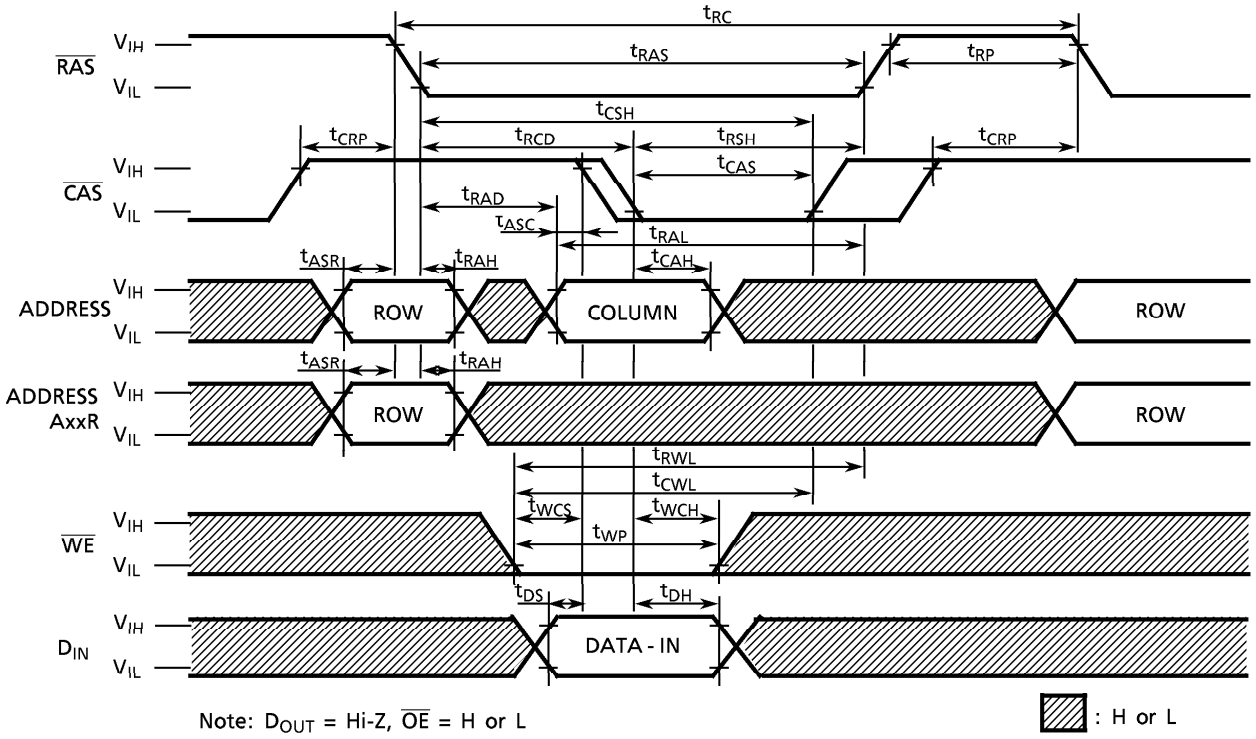
READ CYCLE



OE-CONTROLLED READ CYCLE



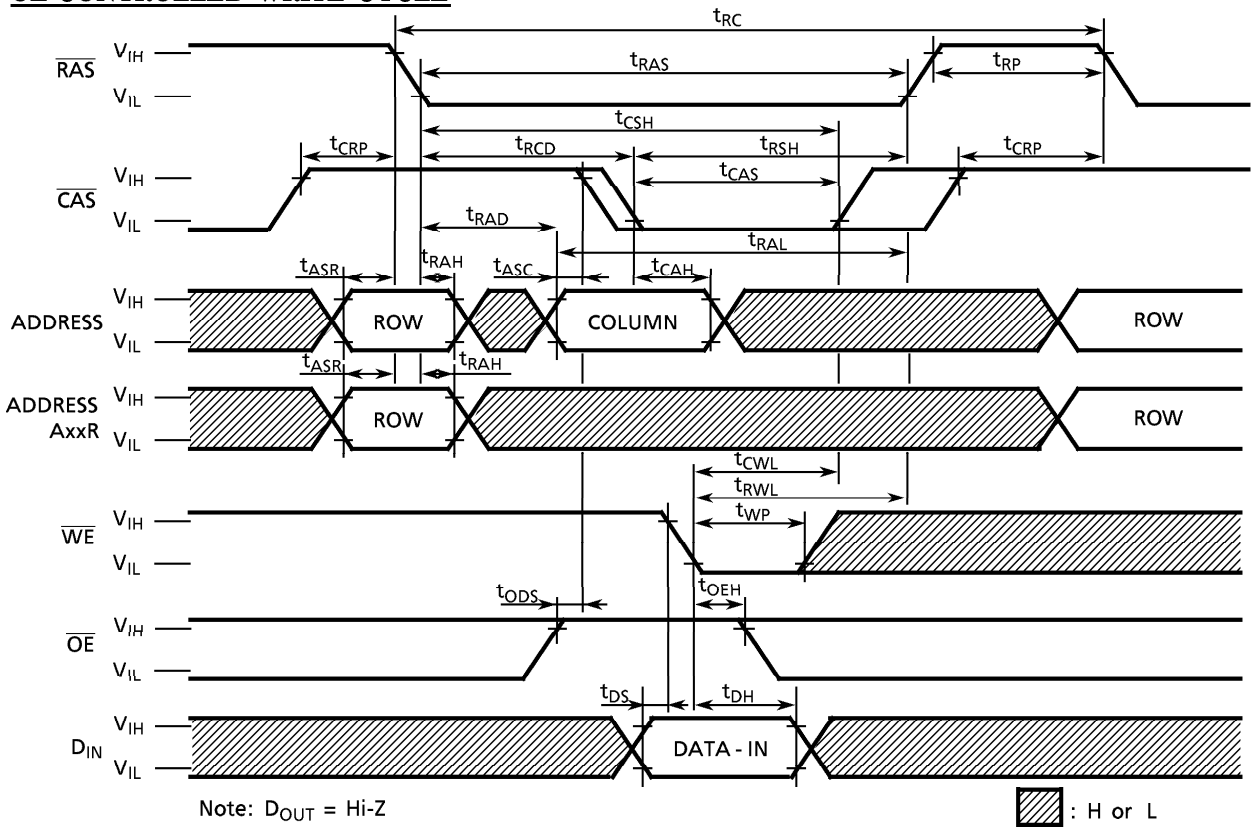
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z, $\overline{OE}$ = H or L

: H or L

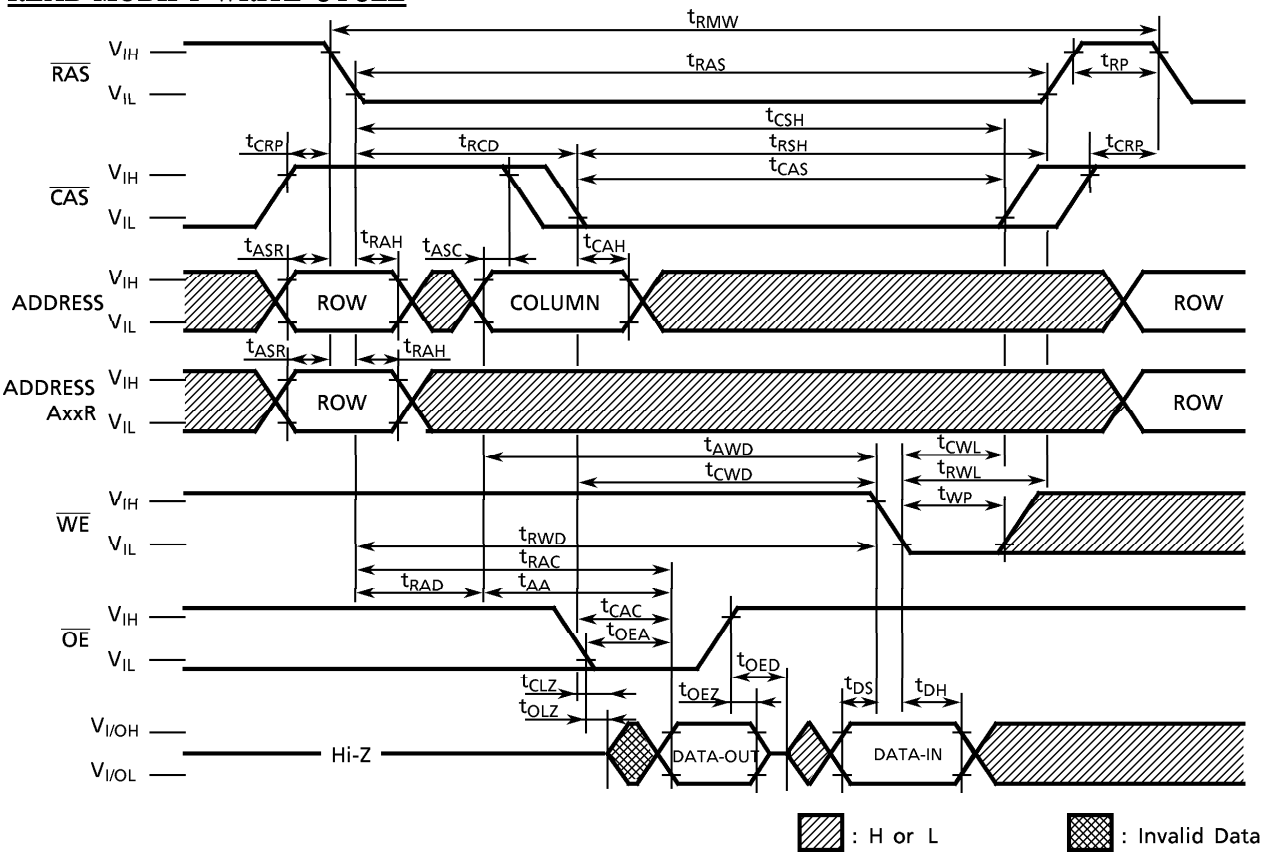
$\overline{OE}$-CONTROLLED WRITE CYCLE



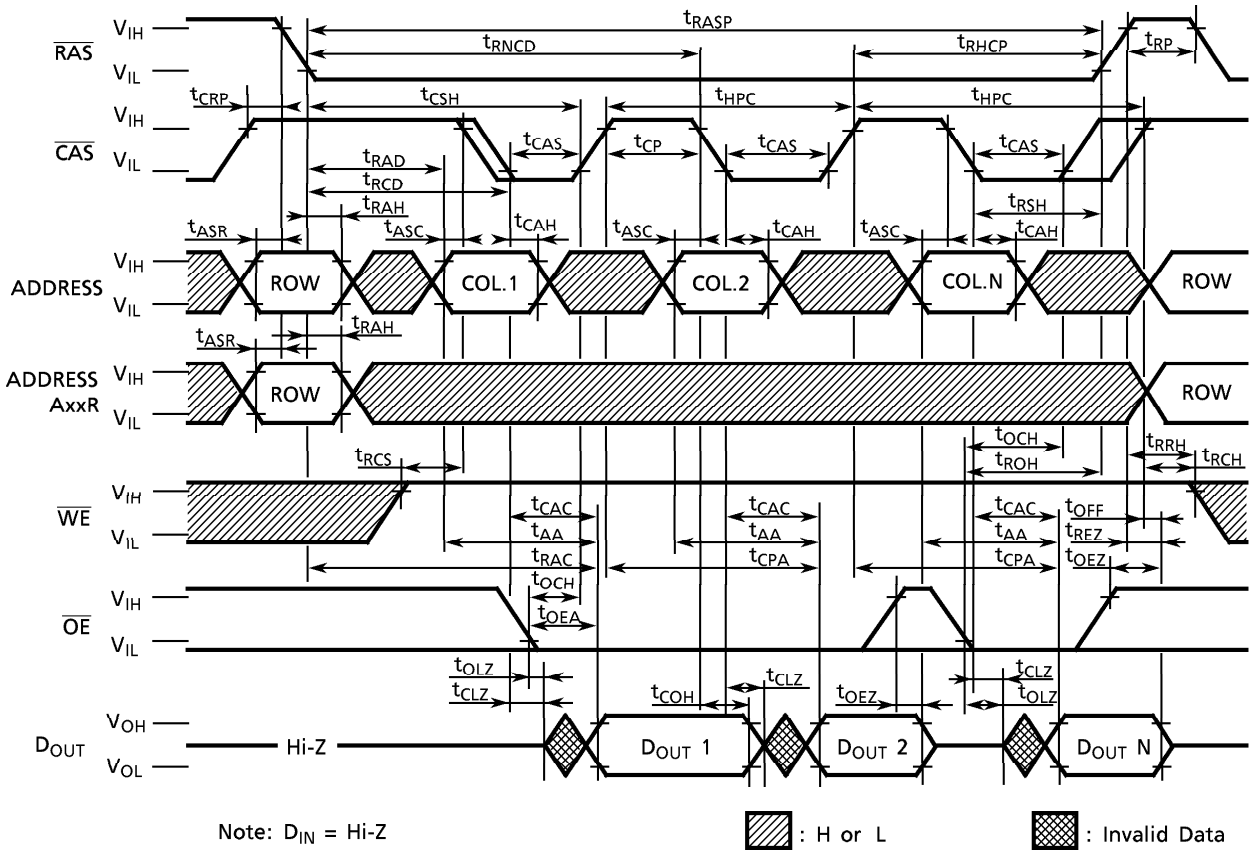
Note: D_{OUT} = Hi-Z

: H or L

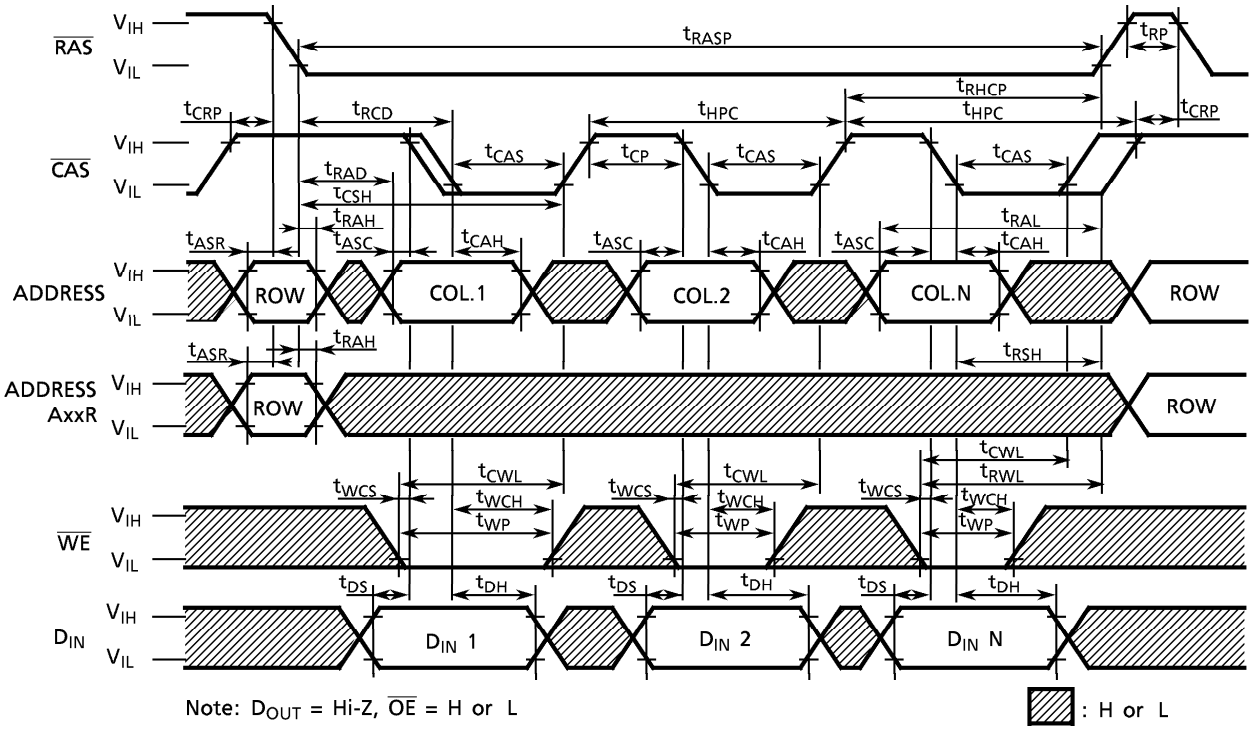
READ-MODIFY-WRITE CYCLE



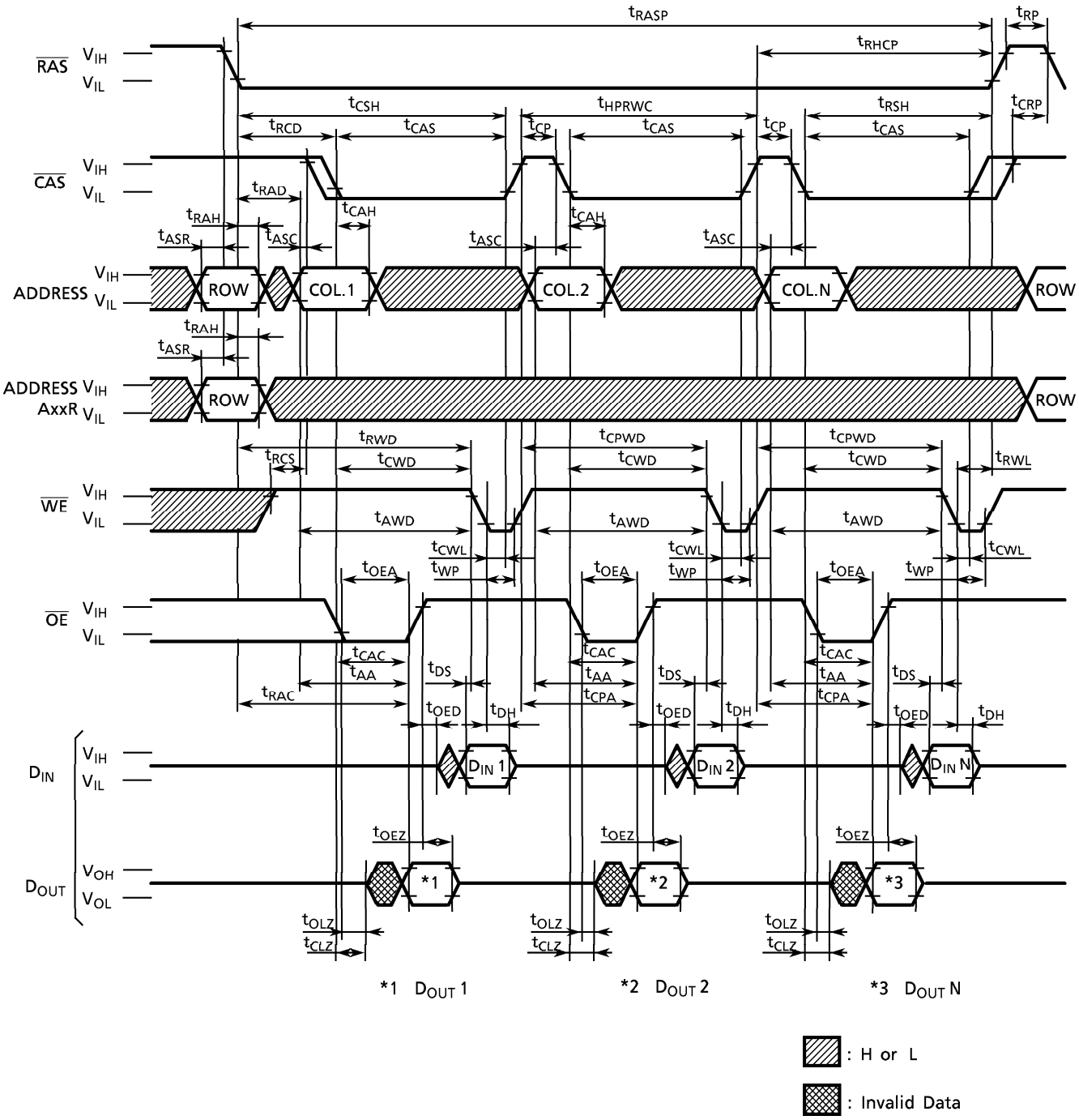
HYPER PAGE MODE READ CYCLE



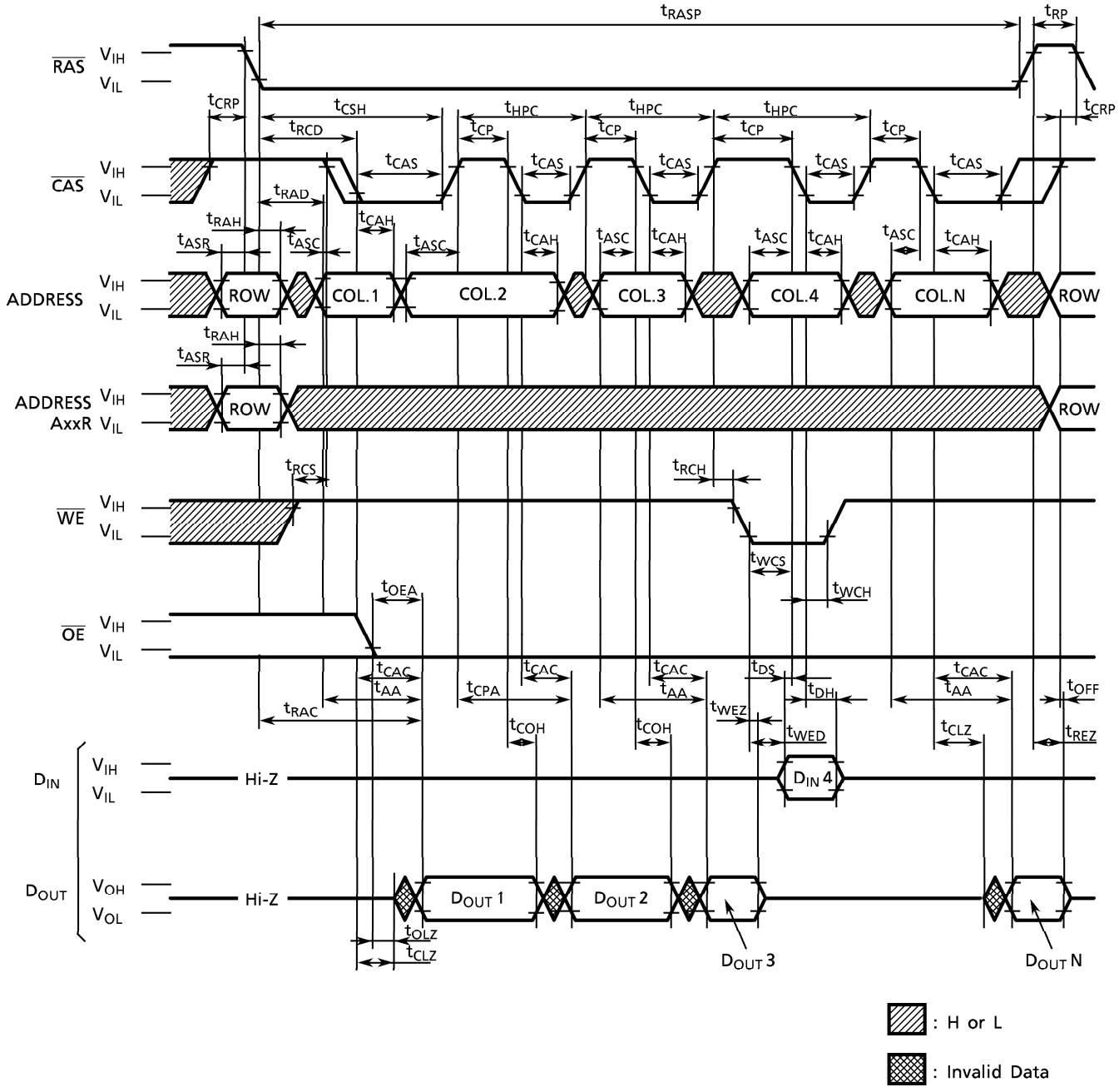
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



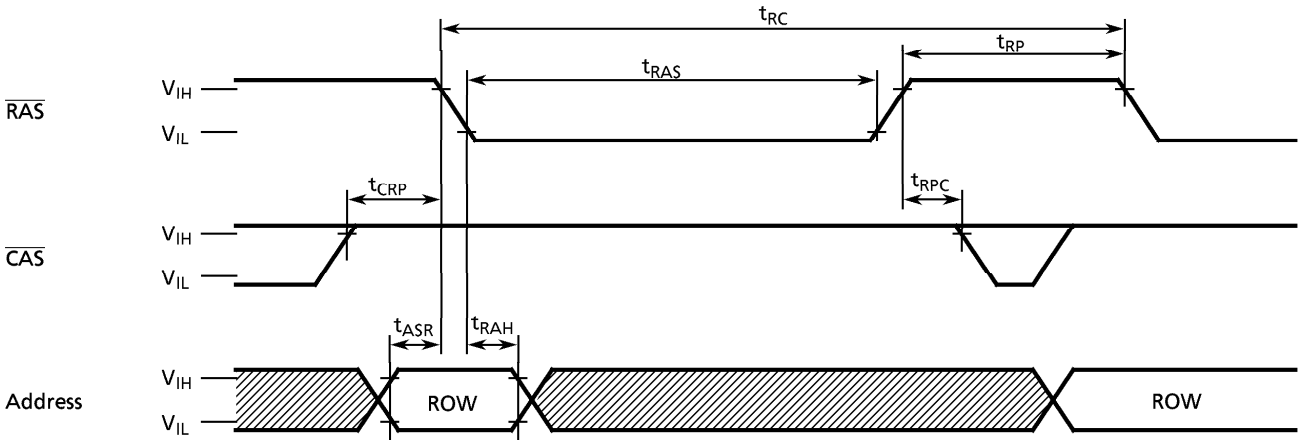
HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE READ WRITE MIXED CYCLE



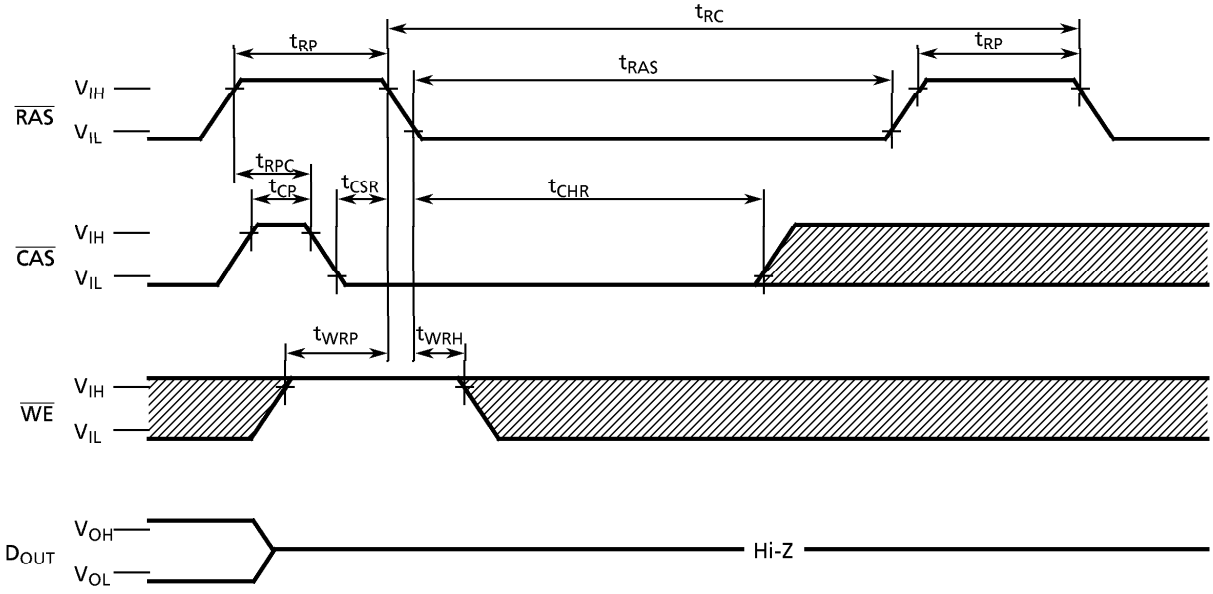
$\overline{RAS}$-ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ and D_{IN} = H or L

▨ : H or L

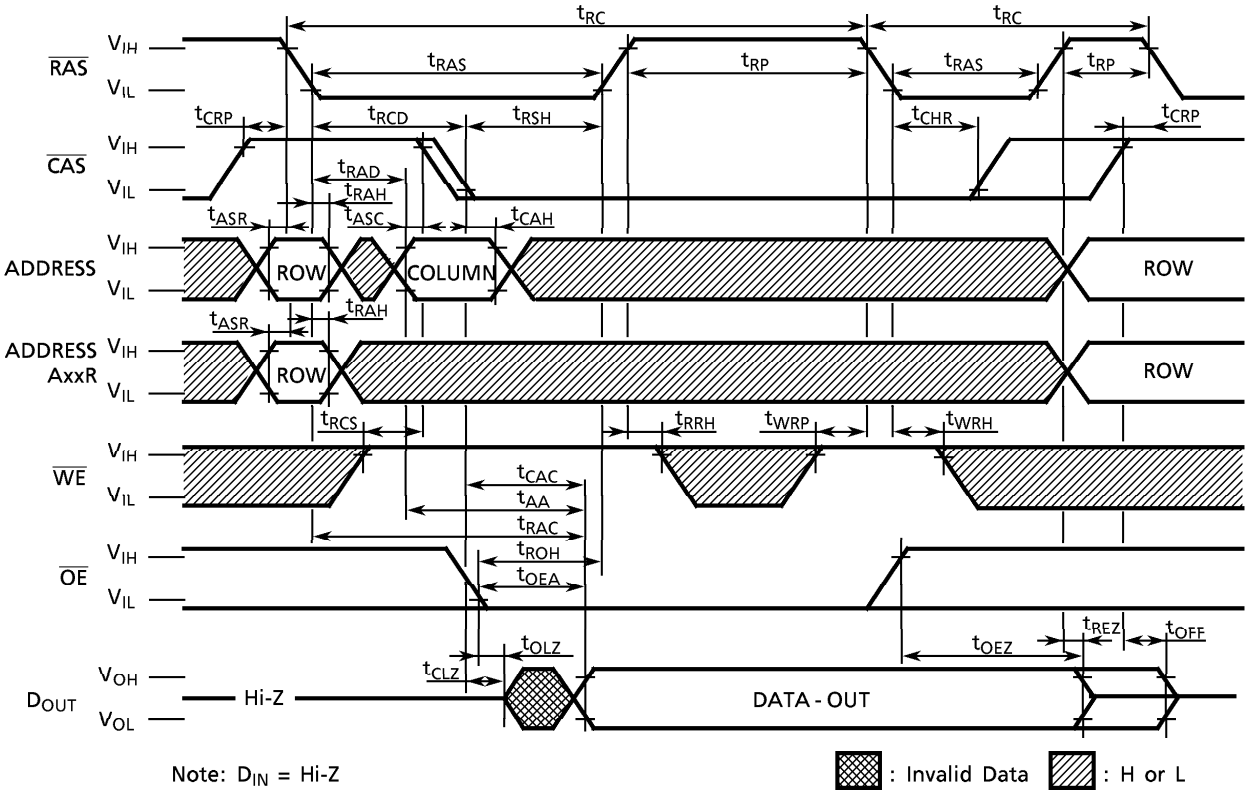
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



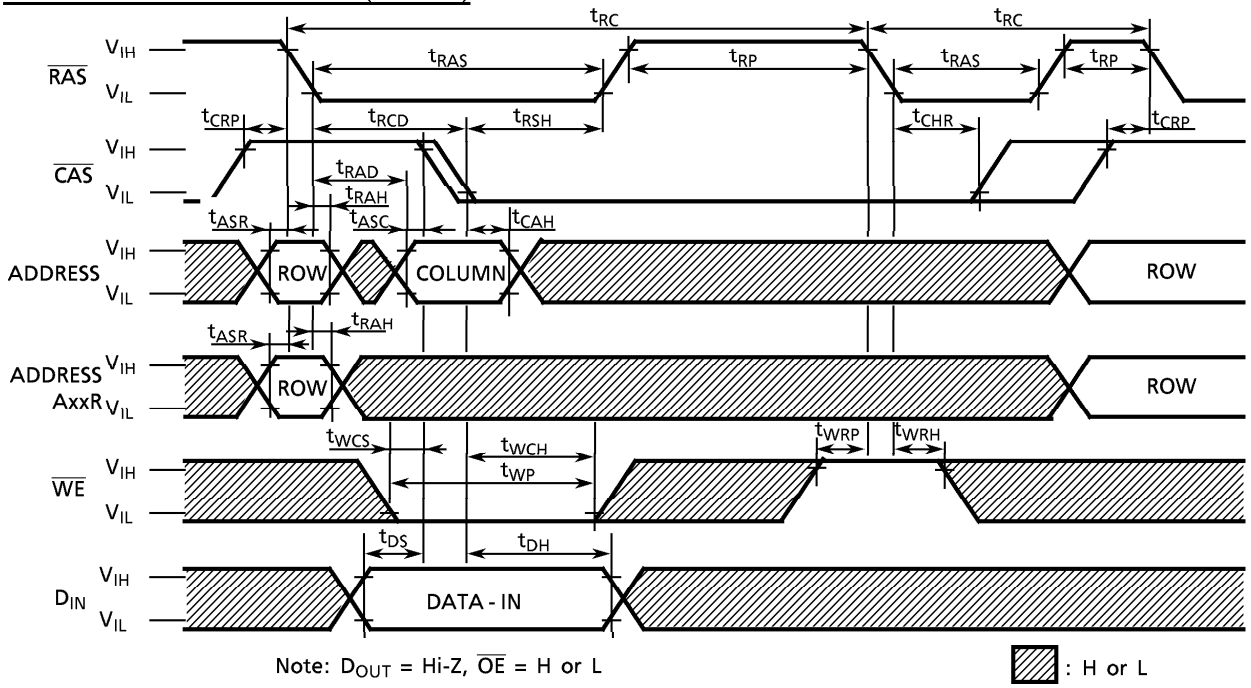
Note: D_{IN}, $\overline{OE}$, ADDRESS = H or L

▨ : H or L

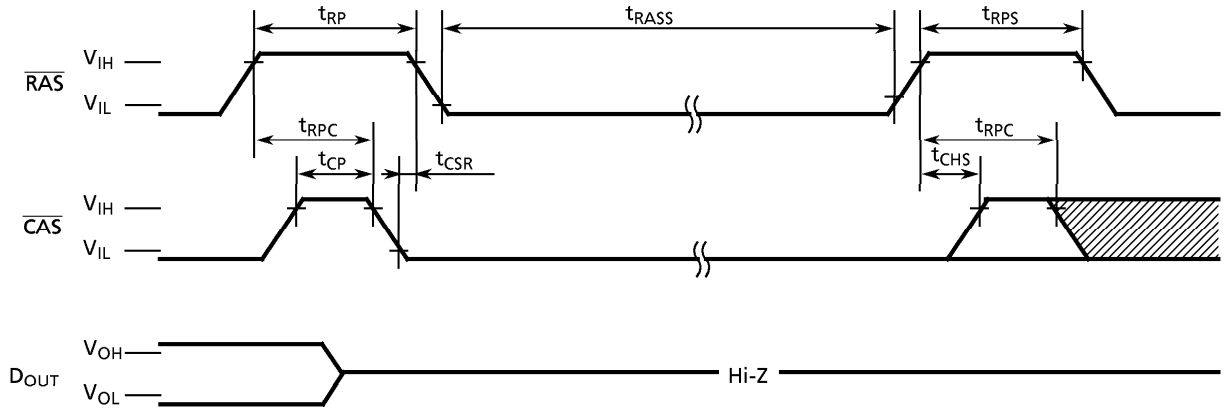
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



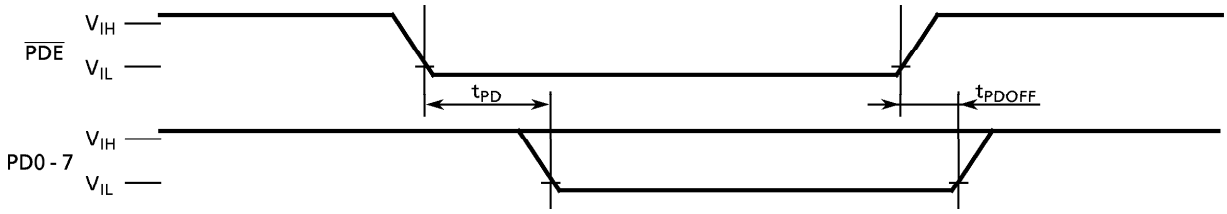
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF-REFRESH CYCLE (THL64VxxxxBTG-xS only)



Note: D_{IN}, $\overline{WE}$, $\overline{OE}$, ADDRESS = H or L

▨ : H or L

PRESENCE DETECT DATA READ CYCLE



Note: t_{PDOFF} is measured with PD pin pulled V_{CC}.