SILICON STACKED GATE CMOS

262,144 WORD x 16 BIT/524,288 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

Description

The TC544200P/F is a 4,194,304 word x 16 bit CMOS one time programmable read only memory. It is organized as either 256K words by 16 bits or 512K words by 8 bits.

The TC544200P/F is compatible with the 40-pin 4M bit Mask ROM and is available in a 40-pin standard plastic package. The TC544200P/F is fabricated using CMOS technology. Advanced circuit techniques result in both high speed and low power features with access times of 120ns/150ns and a maximum operating current of 60mA/8.3MHz.

The electrical characteristics and programming method are the same as for the TC574200D UV EPROM. Once programmed, the TC544200P/F cannot be erased because of the use of a plastic package without a transparent window.

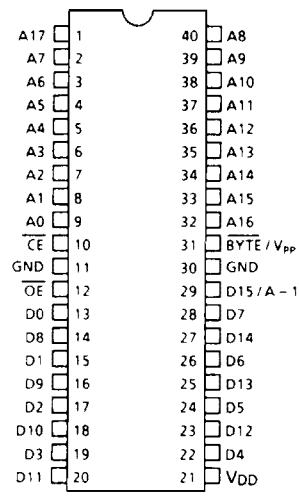
Features

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Fast access time
  - TC544200P/F-120 : 120ns
  - TC544200P/F-150 : 150ns
- Single 5V power supply
- Low power dissipation
  - Active : 60mA/8.3MHz
  - Standby : 100μA
- Fully static operation
- Inputs and outputs TTL compatible
- Three state outputs
- High speed programming mode : t_{PW} = 50μs
- 4M MROM compatible pinout : TC534200P
- Package
  - TC544200P : DIP40-P-600
  - TC544200F : SOP40-P-525

Pin Names

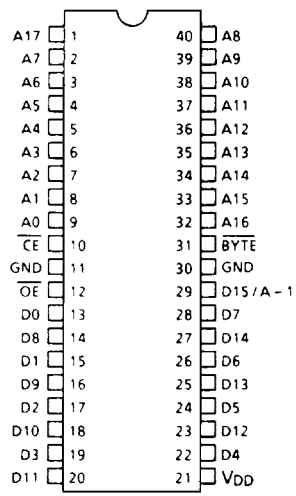
A0 ~ A17	Address Inputs
D0 ~ D14	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A - 1	Output (Input)/Address Input
$\overline{BYTE}$/ V_{PP}	Word, Byte Select Input/ Program Supply Voltage
V_{DD}	Power Supply Voltage (+5V)
GND	Ground

Pin Connection (Top View)



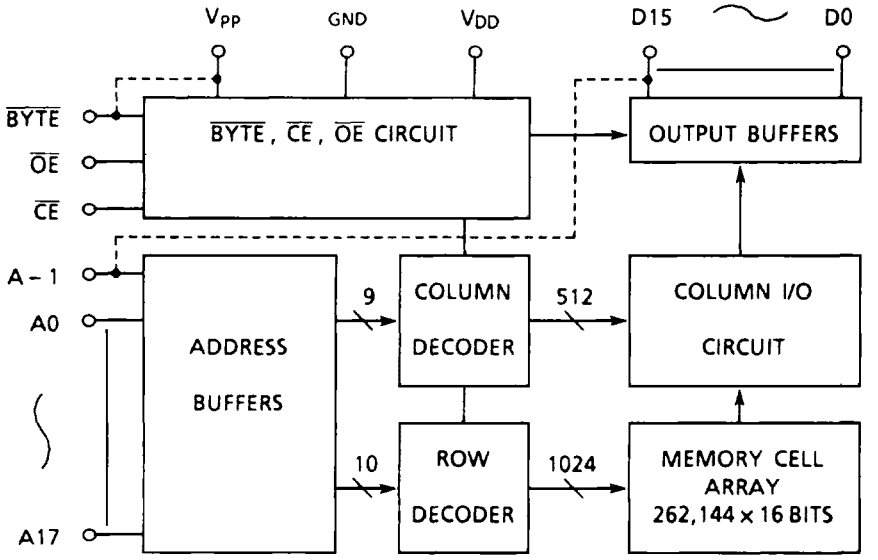
TC544200P / F

(Reference)



4M Mask ROM
TC534200P

Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$/V_{PP}	V_{DD}	D0 ~ D7	D8 ~ D14	D15/A - 1	POWER
Read (16 Bits)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bits)	L	L	L		Data Out (Lower 8 Bits)	High Impedance	L	
Read (Upper 8 Bits)	L	L	L		Data Out (Upper 8 Bits)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			Standby
			L		High Impedance		*	
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note : H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	
V_{IN}	Input Voltage	-0.6 ~ 7.0	
V_{IN}(A9)	Input Voltage (A9)	-0.6 ~ 13.5	
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{DD} + 0.5	
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	

Read Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	4.50	5.00	5.50	
V_{PP}	Program Supply Voltage	0	–	V_{DD} + 0.6	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0V ~ V_{DD}	–	–	±10	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA, f = 8.3MHz	–	–	60	mA
I_{DDO2}		$\overline{CE}$ = 0V, I_{OUT} = 0mA, f = 1MHz	–	–	30	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	–	1	
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V	–	–	100	μA
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	
I_{PP1}	V_{PP} Current	V_{PP} = 0V ~ V_{DD} + 0.6V	–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{DD}	–	–	±10	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	-120		-150		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	120	–	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	120	–	150	
t_{OE}	$\overline{OE}$ to Output Valid	–	60	–	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	50	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	50	0	60	
t_{OH}	Output Data Hold Time	0	–	0	–	
t_{BT}	$\overline{BYTE}$ to Output Valid	–	120	–	150	
t_{BTD}	$\overline{BYTE}$ to Output in High Impedance	–	60	–	70	

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

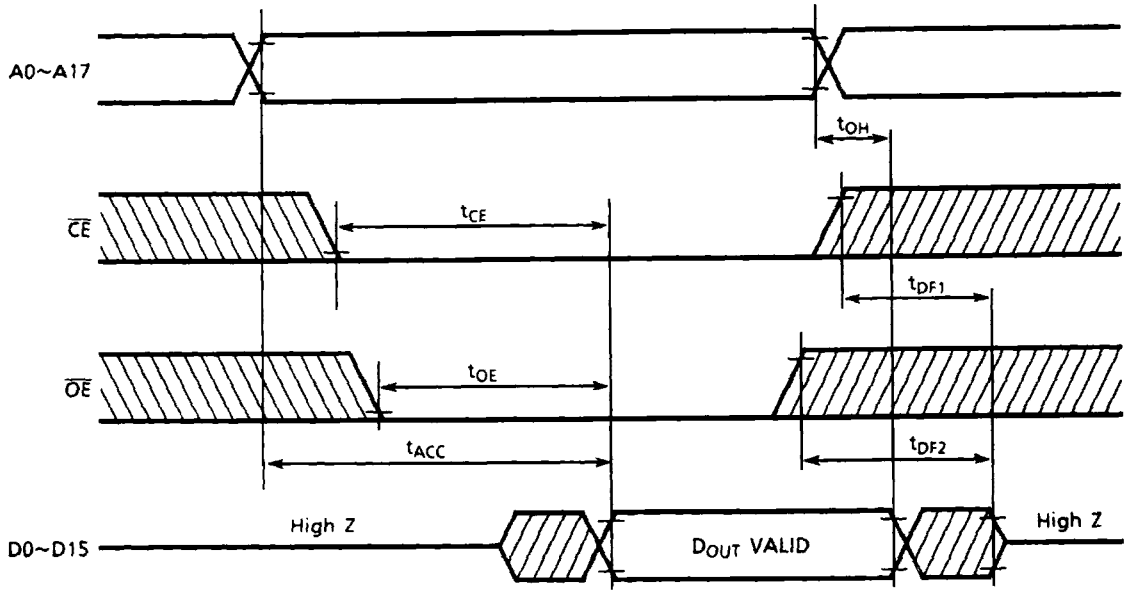
Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	V_{IN} = 0V	–	6	10	pF
C_{IN2}	Input Capacitance ($\overline{BYTE}$/V_{PP})	V_{IN} = 0V	–	110	120	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	10	12	

*This parameter is periodically sampled and is not 100% tested.

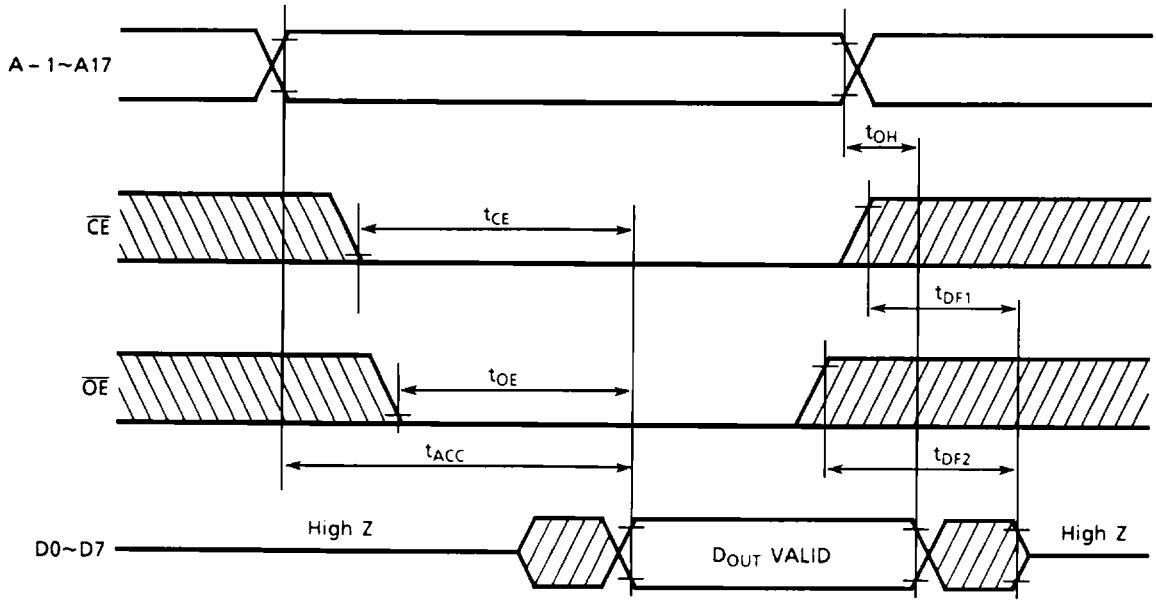
Timing Waveforms (Read)

Word-Wide (16 Bit) Read Mode



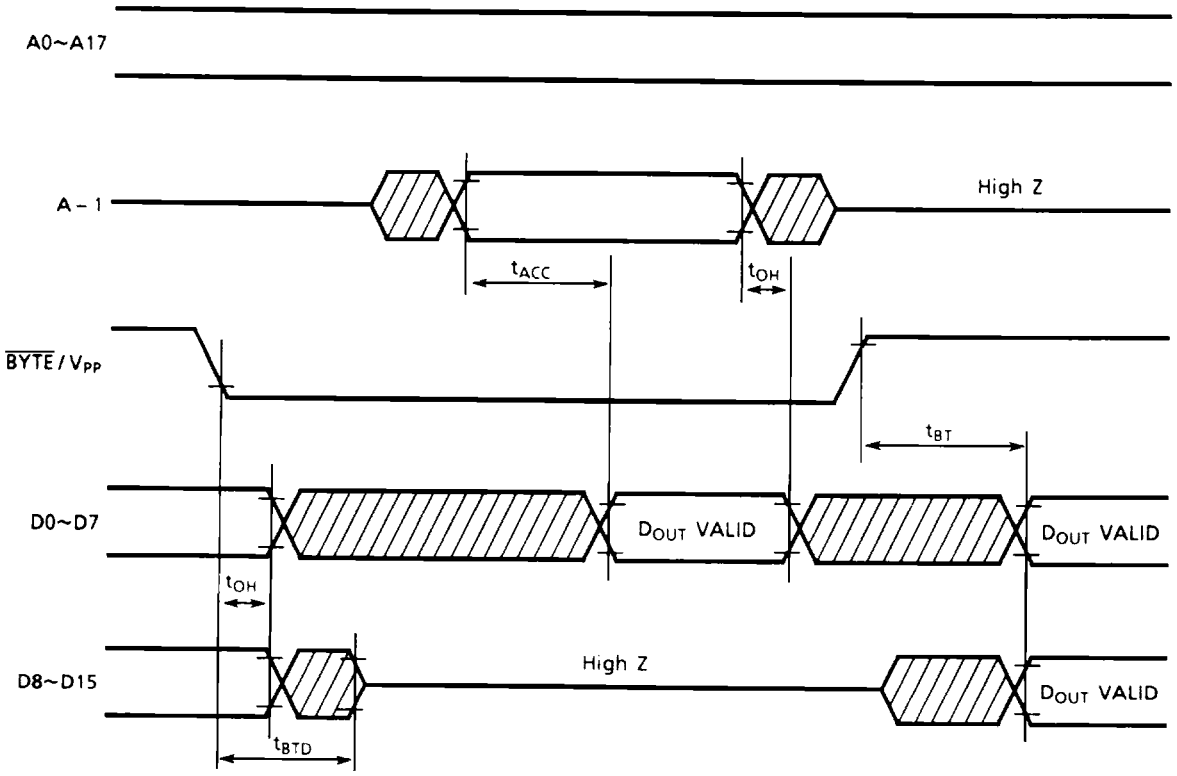
Note : $\overline{BYTE}$ / $V_{PP} = V_{IH}$

Byte-Wide (8 Bit) Read Mode



Note : $\overline{BYTE}$ / $V_{PP} = V_{IL}$

BYTE Transition



Note : $\overline{CE}$, $\overline{OE} = V_{IL}$

High Speed Programming Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 1.0	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	Program Supply Voltage	12.20	12.50	12.80	

DC Characteristics (Ta = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.50V±0.30V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0V ~ V_{DD}	–	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	
I_{DD}	V_{DD} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 12.8V	–	–	50	

AC Programming Characteristics (Ta = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.50V±0.30V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	2	–	–	
t_{VPS}	V_{PP} Setup Time	–	2	–	–	
t_{VDS}	V_{DD} Setup Time	–	2	–	–	
t_{PW}	Program Pulse Width	–	45	50	55	
t_{OPW}	Overprogram Pulse Width	Note 1	45	50	55	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IH}	–	–	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IH}	–	–	90	

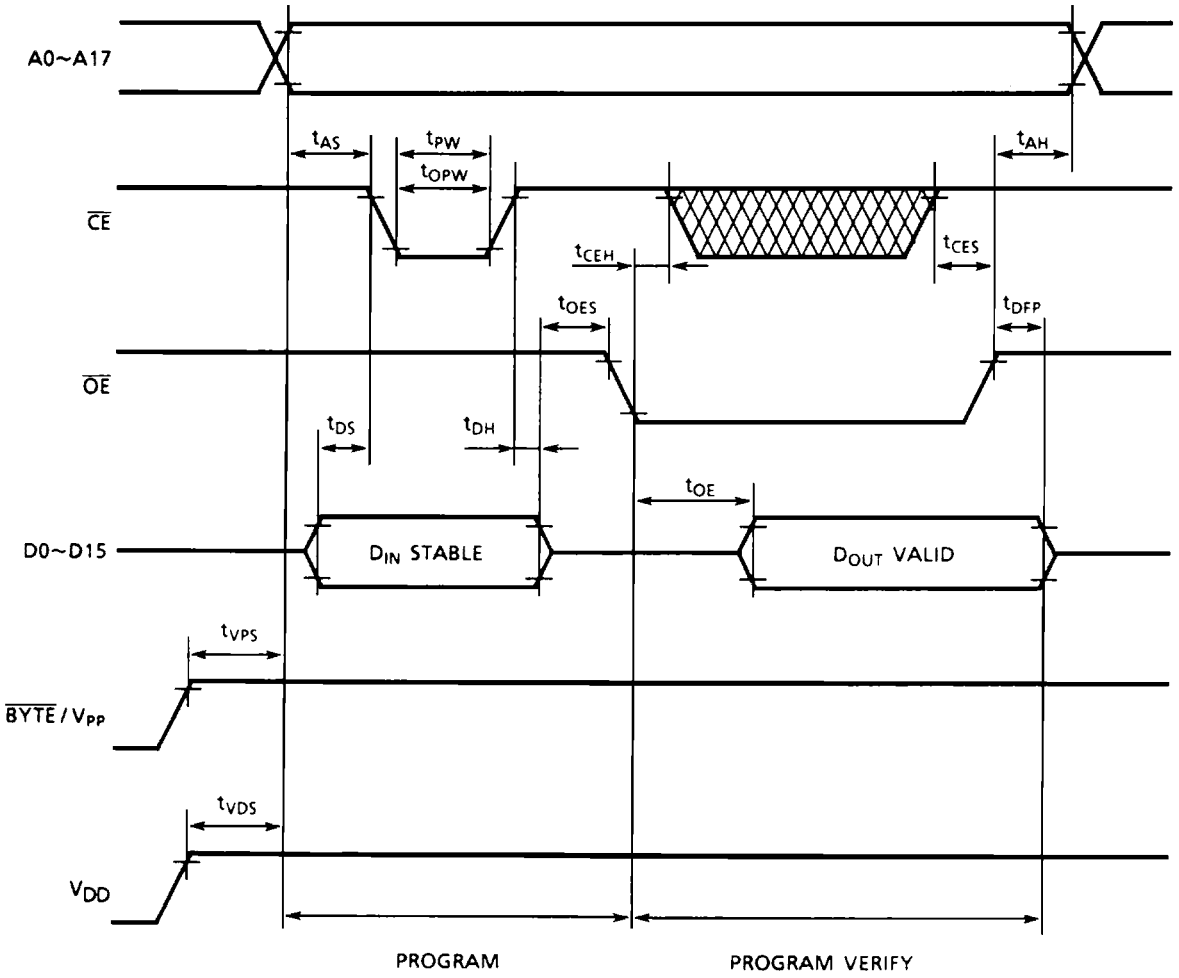
Note: 1. t_{OPW} depends on the program pulse width which is required in the initial programming.

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Timing Waveforms (Program)

High Speed Programming Mode



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from a programming socket and replacing the device in the socket while V_{PP} = 12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Operation Information

The TC544200P/F's eight operating modes are listed in the following table.
Mode selection is achieved by applying TTL level signals to appropriate inputs.

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$/V_{PP}	V_{DD}	D0 ~ D7	D8 ~ D14	D15/A - 1	POWER
Read (16 Bits)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bits)	L	L	L		Data Out (Lower 8 Bits)	High Impedance	L	
Read (Upper 8 Bits)	L	L	L		Data Out (Upper 8 Bits)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			Standby
			L		High Impedance		*	
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Notes: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Read Mode

The TC544200P/F has a $\overline{BYTE}$/V_{PP} terminal that selects word-wide (16 bit) output or byte-wide (8 bit) output. When $\overline{BYTE}$/V_{PP} is set to V_{IH}, word-wide input is selected, and the D15/A - 1 pin is used for D15 data output. When $\overline{BYTE}$/V_{PP} is set to V_{IL}, byte-wide output is selected, and the D15/A - 1 pin is used for A - 1 address input. When A - 1 is set to V_{IL} in this condition, The data that is output is the lower 8 bits of the 16 bits which had been programmed. When A - 1 is set to V_{IH}, the data output is the upper 8 bits.

The TC544200P/F has two control inputs. The chip enable ($\overline{CE}$) input controls the operating power and should be used for device selection while the output enable ($\overline{OE}$) input controls the output buffers. Assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL}, once the address has stabilized, output data will be valid after the address access time has elapsed. The $\overline{CE}$ to output valid time (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}$ = V_{IL}, and that the address has been stable for at least t_{ACC}, then output data will be valid after t_{OE} from the falling edge of $\overline{OE}$.

Output Deselect Mode

If $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, the outputs will be in a high impedance state.

Therefore, two or more devices can be connected together on a common bus if the output of only one device is enabled. When $\overline{CE}$ is used for device selection, all deselected devices are in the low power standby mode.

Standby Mode

The TC544200P/F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a MOS high level voltage (V_{DD}) to the $\overline{CE}$ input, the TC544200P/F is placed in the standby mode which reduces the operating current to 100μA and puts the outputs in a high impedance state, independent of the $\overline{OE}$ input.

Program Mode

When the TC544200P/F is initially received by customers, all bits of the device are in the "1" state, which is the erased state. Therefore, the object of the program operation is to introduce "0" data into the desired bit locations. The TC544200P/F is in the programming mode when V_{PP} = 12.5V, $\overline{CE}$ = V_{IL}, and $\overline{OE}$ = V_{IH}. Data to be programmed must be applied 16 bits in parallel to the data pins.

The TC544200P/F can be programmed at any address location at any time - either individually, sequentially, or at random.

Program Verify Mode

The verify mode is used to check that the desired data has been correctly programmed. The verify mode is activated when $\overline{OE}$ = V_{IL}. The programmed data should be compared with the original word-wide (16 bit) data.

Program Inhibit Mode

When the programming voltage (12.5V) is applied to the V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC544200P/F from being programmed. The programming of two or more TC544200P/Fs in parallel with different data is easily accomplished. All

inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, then a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only while a TTL high level signal is applied to the $\overline{CE}$ of the other devices.

High Speed Programming Mode

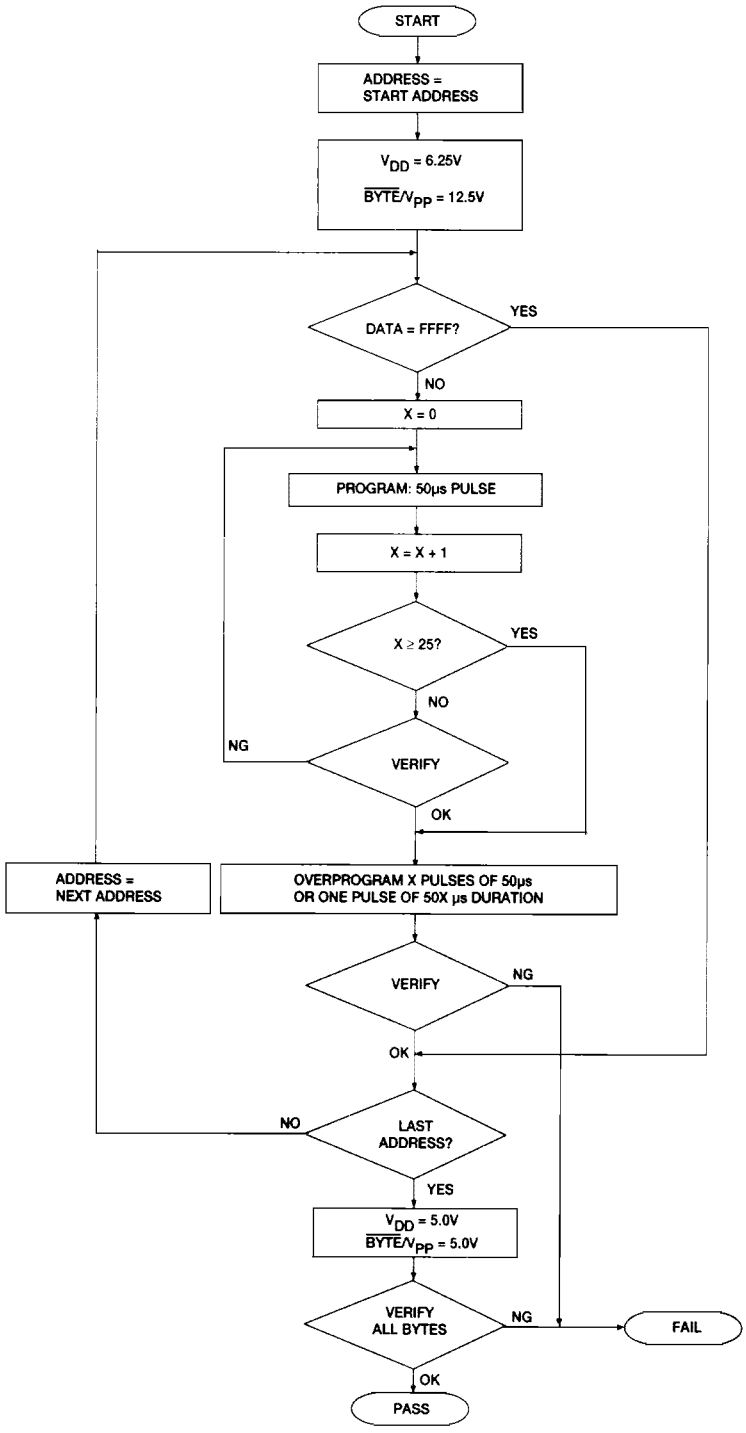
The device is set up in high speed programming mode when the programming voltage (12.5V) is applied to the V_{PP} terminal with V_{DD} = 6.25V.

Programming is achieved by applying a single 50μs TTL low level pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using the program verify mode. If the programmed data is not correct, another program pulse of 50μs is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

After correctly programming the selected address, an overprogram pulse with the same width as that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{DD} = V_{PP} = 5V$.

High Speed Programming Mode

Flow Chart



Electric Signature Mode

The electric signature mode allows one to read out a code from the TC544200P/F which identifies its manufacturer and device type.

The programming equipment may read out the manufacturer code and device code from the TC544200P/F by using this mode before programming and automatically set the programming voltage (V_{PP}) and algorithm.

The electric signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} during a read operation. Data output under these conditions is the manufacturer code. The device code is output when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit being (D7).

The following table shows the electric signature of the TC544200P/F.

PINS / SIGNATURE	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	1	1	1	**8F

Notes: A9 = 12.0V±0.5V
A1 ~ A8, A10 ~ A17, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{BYTE}/V_{PP}$ = V_{IH}

* Don't care