Data Sheet

# T7102A-X.25/X.75 Protocol Controller

## Features

- 24-bit address bus to address a 16-Mbyte address space
- Dual-channel DMA with standard interface, including DMA request, DMA acknowledge, DMA read, and DMA write
- Independently programmable T1 and T4 timers
- Programmable retransmission counter
- Transmit and receive buffers accessed indirectly through a look-up table
- Programmable modulo-8 or modulo-128 frame sequence numbering
- Programmable window size (transmit and receive)
- Selectable 16-bit (CRC-CCITT) or 32-bit polynomial for frame checking sequence (FCS)
- Wait-state generator (on DMA side) for slow memory
- Programmable interframe flag fill
- Error detection and automatic recovery via packet retransmission
- Link initialization and supervision
- Independently programmable transmit and receive window size
- Password exchange mechanism for dial-up operation
- Programmable for X.25 or X.75 operation
- Supports 8-bit or 16-bit data buses
- Intel, Motorola, or *WE*® 32100 Microprocessor DMA interface (data bus)
- Sixteen programmable event counters, with optional interrupt capability
- Daisy-chain DMA structure for priority-controlled CPU interfaces
- Two independent test modes (far-end loopback and near-end loopback) to verify the XPC and its link
- Optional parity generation and checking across data bus interface on all DMA operations
- Six bidirectional address leads for accessing 51 internal XPC registers
- 2-MHz clock
- Single 5 V supply

## Description

The T7102A X.25/X.75 Protocol Controller (XPC) integrated circuit is an X.25/X.75 level 2 protocol controller. It is a single-chip LSI device available in a 70-pin pin-grid-array (PGA) package and is fabricated using N-channel silicon gate MOS technology. The T7102A XPC implements an augmented X.25 level 2 data communications standard for packet switching. The device satisfies the X.25 link level (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. The device also implements X.75 level 2 protocol, which is used in internetwork applications. The protocol controller is bit-oriented, with a maximum transmit and receive speed of 333 kb/s. A set of programmable registers controls and records vital events during data transmission.

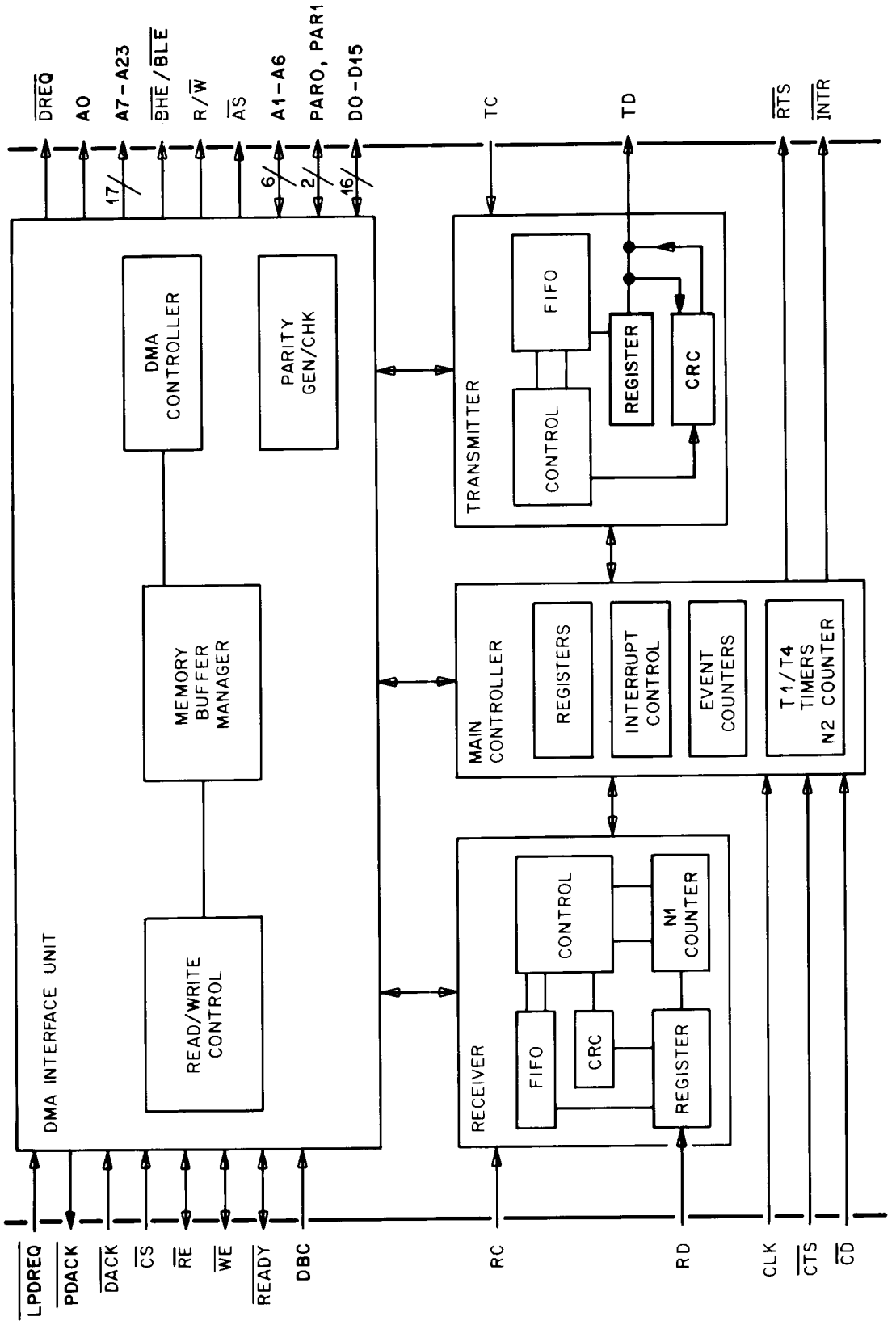
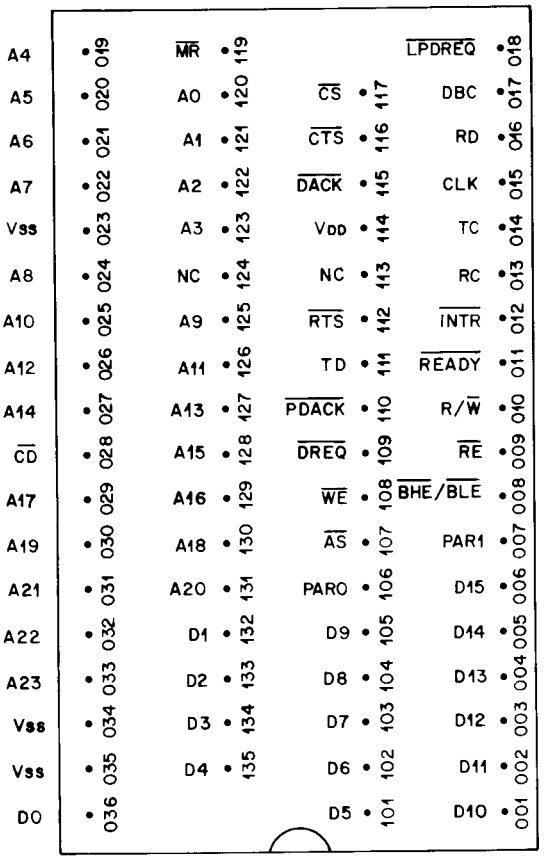



Figure 1. Block Diagram

# User Information

## Pin Descriptions




| Sym | Pin | Sym | Pin | Sym | Pin |
|---|---|---|---|---|---|
| A0 | 120 | A23 | 33 | D15 | 6 |
| A1 | 121 | $\overline{AS}$ | 107 | $\overline{DACK}$ | 115 |
| A2 | 122 | $\overline{BHE}$/ | 8 | DBC | 17 |
| A3 | 123 | $\overline{BLE}$ | | $\overline{DREQ}$ | 109 |
| A4 | 19 | $\overline{CD}$ | 28 | $\overline{INTR}$ | 12 |
| A5 | 20 | CLK | 15 | $\overline{LPDREQ}$ | 18 |
| A6 | 21 | $\overline{CTS}$ | 116 | $\overline{MR}$ | 119 |
| A7 | 22 | $\overline{CS}$ | 117 | PAR0 | 106 |
| A8 | 24 | D0 | 36 | PAR1 | 7 |
| A9 | 125 | D1 | 132 | $\overline{PDACK}$ | 110 |
| A10 | 25 | D2 | 133 | RC | 13 |
| A11 | 126 | D3 | 134 | RD | 16 |
| A12 | 26 | D4 | 135 | $\overline{RE}$ | 9 |
| A13 | 127 | D5 | 101 | $\overline{READY}$ | 11 |
| A14 | 27 | D6 | 102 | $\overline{RTS}$ | 112 |
| A15 | 128 | D7 | 103 | R/$\overline{W}$ | 10 |
| A16 | 129 | D8 | 104 | TC | 14 |
| A17 | 29 | D9 | 105 | TD | 111 |
| A18 | 130 | D10 | 1 | VDD | 114 |
| A19 | 30 | D11 | 2 | VSS | 23,34, |
| A20 | 131 | D12 | 3 | | 35 |
| A21 | 31 | D13 | 4 | $\overline{WE}$ | 108 |
| A22 | 32 | D14 | 5 | | |

**Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols**

**Table 1. Pin Descriptions**

| Pin | Symbol | Type | Name/Function |
|---|---|---|---|
| 1<br>2<br>3<br>4<br>5<br>6 | D10<br>D11<br>D12<br>D13<br>D14<br>D15 | I/O* | **Data Bus Bit 10.**<br>**Data Bus Bit 11.** If DBC (pin 17) is high, a 16-bit data bus (pins 1—6,<br>**Data Bus Bit 12.** 36, 101—105, and 132—135) is used; if DBC is low,<br>**Data Bus Bit 13.** an 8-bit data bus (pins 36, 101—103, and 132—135)<br>**Data Bus Bit 14.** is used.<br>**Data Bus Bit 15.** |
| 7 | PAR1 | I/O* | **Parity on High Data Byte.** Parity generation and checking of high byte of data bus. Valid only during DMA operations. |
| 8 | $\overline{BHE}$/$\overline{BLE}$ | O* | **Byte High Enable (Active Low).** The XPC uses this line to control access to the high data byte when it has a 16-bit data bus. Access is to the low data byte in the Motorola configuration (see Table 18). |
| 9 | $\overline{RE}$ | I/O* | **Read Enable (Active Low).** An input during CPU access of XPC registers; an output during DMA read cycles. |

* Indicates 3-state condition.

**Table 1. Pin Descriptions (Continued)**

| Pin | Symbol | Type | Name/Function |
|---|---|---|---|
| 10 | R/$\overline{W}$ | O* | **Read or Write (Active Low).** If low, the XPC wants to write to main memory; if high, the XPC wants to read from main memory. Not used during internal XPC register read/write operations. |
| 11 | $\overline{READY}$ | I/O* | **Ready (Active Low).** This signal is used as an input during DMA read and write cycles to allow slow memory to be accessed. During DMA operations, $\overline{RE}$ and $\overline{WE}$ (pins 9 and 108) remain low as long as $\overline{READY}$ is held high. During CPU read/write operations of internal XPC registers, $\overline{READY}$ is an output. It goes low to signal the CPU that the read/write operation is complete. |
| 12 | $\overline{INTR}$ | O | **Interrupt Request (Active Low).** This signal indicates that the XPC is requesting service. It returns high when the CPU reads the interrupt register. |
| 13 | RC | I | **Receive Clock.** Data is received at this frequency. |
| 14 | TC | I | **Transmit Clock.** Data is transmitted at this frequency. |
| 15 | CLK | I | **Clock.** This pin controls the internal sequencing of the chip. The clock must be a square wave with a minimum frequency of 250 kHz and a maximum frequency of 2 MHz ($f_{CLK} \geq 6f_{RC}$ and $f_{CLK} \geq 6f_{TC}$). |
| 16 | RD | I | **Receive Data.** Serial data input line. |
| 17 | DBC | I | **Data Bus Configuration.** This pin must be wired to $V_{SS}$ or $V_{DD}$ to configure the XPC data bus for 8-bit or 16-bit operation, respectively. |
| 18 | $\overline{LPDREQ}$ | I | **Low-Priority DMA Request (Active Low).** This pin is used to daisy-chain DMA requests in systems without a bus arbiter that use more than one XPC. Tie high on lowest priority XPC in the daisy chain. |
| 19 | A4 | I/O* | **Address Bus Bit 4.** If $\overline{CS}$ (pin 117) is low, A1—A6 (pins 19—21 and |
| 20 | A5 | I/O* | **Address Bus Bit 5.** 121—123) are inputs used to address the XPC |
| 21 | A6 | I/O* | **Address Bus Bit 6.** internal registers; if $\overline{CS}$ is high, all pins of the |
| 22 | A7 | O* | **Address Bus Bit 7.** 24-bit address bus (pins 19—22, 24—27, 29—33, 120—123, and 125—131) are outputs used to address system memory. |
| 23 | $V_{SS}$ | O | **Ground.** |
| 24 | A8 | O* | **Address Bus Bit 8.** |
| 25 | A10 | | **Address Bus Bit 10.** |
| 26 | A12 | | **Address Bus Bit 12.** See description of pins 19—22. |
| 27 | A14 | | **Address Bus Bit 14.** |
| 28 | $\overline{CD}$ | I | **Carrier Detect (Active Low).** $\overline{CD}$ generates two interrupts to notify the host of level 1 activity. No further processing is done by the XPC. |
| 29 | A17 | O* | **Address Bus Bit 17.** |
| 30 | A19 | | **Address Bus Bit 19.** |
| 31 | A21 | | **Address Bus Bit 21.** See description of pins 19—22. |
| 32 | A22 | | **Address Bus Bit 22.** |
| 33 | A23 | | **Address Bus Bit 23.** |
| 34 | $V_{SS}$ | — | **Ground.** |

* Indicates 3-state condition.

**Table 1. Pin Descriptions (Continued)**

| Pin | Symbol | Type | Name/Function |
|---|---|---|---|
| 35 | VSS | — | **Ground.** |
| 36 | D0 | I/O* | **Data Bus Bit 0.** See description of pins 1—6. |
| 101 | D5 | | **Data Bus Bit 5.** |
| 102 | D6 | | **Data Bus Bit 6.** |
| 103 | D7 | | **Data Bus Bit 7.** |
| 104 | D8 | | **Data Bus Bit 8.** |
| 105 | D9 | | **Data Bus Bit 9.** |
| 106 | PAR0 | I/O* | **Parity on Low Data Byte.** Parity generation and checking of low byte of data bus. Valid only during DMA operations. |
| 107 | $\overline{AS}$ | O* | **Address Strobe (Active Low).** The XPC uses this signal during DMA operations to indicate that it has placed a valid address on the address bus. |
| 108 | $\overline{WE}$ | I/O* | **Write Enable (Active Low).** Used as an input during CPU access of XPC registers. Output during DMA write cycles. |
| 109 | $\overline{DREQ}$ | O | **DMA Request (Active Low).** A low on this pin indicates to the CPU that the XPC needs the address bus and the data bus for DMA cycles. |
| 110 | $\overline{PDACK}$ | O | **Propagated DMA Acknowledge (Active Low).** This pin is used to daisy-chain acknowledgments in systems using more than one XPC. $\overline{PDACK}$ output of one XPC connects to $\overline{DACK}$ input of the next lower priority XPC. |
| 111 | TD | O | **Transmit Data.** XPC serial data output line. |
| 112 | $\overline{RTS}$ | O | **Request to Send (Active Low).** When asserted, this signal indicates to level 1 that the XPC is ready to transmit either data or flags over the link. $\overline{RTS}$ remains low while the link is up. |
| 113 | NC | — | **No Connection.** |
| 114 | VDD | — | **5 V Supply.** |
| 115 | $\overline{DACK}$ | I | **DMA Acknowledge (Active Low).** When this signal is low, the CPU indicates that the XPC has been granted system buses. All floating outputs of the XPC then become TTL drivers. $\overline{DACK}$ must remain low until $\overline{DREQ}$ (pin 19) is removed. |
| 116 | $\overline{CTS}$ | I | **Clear to Send (Active Low).** Level 1 interface notifies the XPC that the data set is ready to send by asserting this signal. The link cannot come up until $\overline{CTS}$ is asserted. $\overline{CTS}$ must remain asserted when the link is up. |
| 117 | $\overline{CS}$ | I | **Chip Select (Active Low).** $\overline{CS}$ must be asserted to allow access to internal registers of the XPC. When $\overline{CS}$ is asserted, $\overline{RE}$, $\overline{WE}$, and A1—A6 become inputs and $\overline{READY}$ becomes an output. |
| 119 | $\overline{MR}$ | I | **Master Reset (Active Low).** When this pin is asserted, all command, status, and parameter register bits are cleared (0) except for the mandatory disconnect (MDISC) and the DISCMODE bits in command register 0, which are set (1). $\overline{MR}$ must be high for at least two clock (CLK) periods after power-on. The minimum low time for reset is 1.5 CLK periods. All outputs are 3-stated when both $\overline{MR}$ and $\overline{CS}$ are low. |

* Indicates 3-state condition.

**Table 1. Pin Descriptions (Continued)**

| Pin | Symbol | Type | Name/Function |
|---|---|---|---|
| 120 | A0 | O* | **Address Bus Bit 0.** |
| 121 | A1 | I/O* | **Address Bus Bit 1.** |
| 122 | A2 | I/O* | **Address Bus Bit 2.** See description of pins 19—22. |
| 123 | A3 | I/O* | **Address Bus Bit 3.** |
| 124 | NC | — | **No Connection.** |
| 125 | A9 | O* | **Address Bus Bit 9.** |
| 126 | A11 | | **Address Bus Bit 11.** |
| 127 | A13 | | **Address Bus Bit 13.** |
| 128 | A15 | | **Address Bus Bit 15.** See description of pins 19—22. |
| 129 | A16 | | **Address Bus Bit 16.** |
| 130 | A18 | | **Address Bus Bit 18.** |
| 131 | A20 | | **Address Bus Bit 20.** |
| 132 | D1 | I/O* | **Data Bus Bit 1.** |
| 133 | D2 | | **Data Bus Bit 2.** |
| 134 | D3 | | **Data Bus Bit 3.** See description of pins 1—6. |
| 135 | D4 | | **Data Bus Bit 4.** |

* Indicates 3-state condition.

## Overview

The T7102A XPC performs complete link level control according to X.25 and X.75 data communications protocols. The device generates supervisory and unnumbered frames automatically, without intervention by the host. The host must supply buffers for the data fields of received and transmitted information frames. It is notified of important events via interrupts. The XPC contains a transmitter, receiver, controller, and an interface unit, as shown in Figure 1.

## Architecture

### Transmitter

The transmitter constructs frames on command from the main controller. The transmitter contains a transmitter controller, 4-byte (first-in first-out) FIFO buffer, holding register, cyclic redundancy check (CRC) encoder, and zero inserter. The transmitter handles the transmission of continuous flags, aborts, or idle channel indications automatically. Bit stuffing is implemented to ensure data transparency.

The transmitter FIFO and the transmitter holding register control the flow of information from main memory to the data link. The transmitter FIFO is used as temporary storage for data delivered from memory to the transmitter by the DMA controller. The DMA controller can read two bytes of data at a time from main memory and place them into the transmitter FIFO. The transmitter holding register is loaded in a parallel fashion from the transmitter FIFO. The various bytes needed to construct a frame are also loaded into the holding register. When the data is ready to be transmitted, it is shifted out serially through the transmit data (TD) lead on the negative edge of the transmit clock (TC).

The CRC encoder calculates the frame check sequence (FCS) and appends it to the data field, or to the control field for frames without data. The FCS is calculated over the address, control, and data fields. The zero inserter performs bit stuffing to ensure data transparency.

### Receiver

The receiver processes incoming data and notifies the controller of received frames and other link conditions. The receiver contains a preprocessor, receiver controller, 4-byte FIFO, receiver register, and CRC decoder. The preprocessor detects flags, aborts, and idle conditions on the data link, and deletes the 0s that were added for data transparency. Receive data (RD) is latched on the positive edge of the receive clock (RC). Frames are identified and checked for proper format by the receiver controller.

The information field of a frame is loaded into the FIFO and is DMAed to memory by the interface unit.

The frame is checked for transmission errors by means of the CRC. The XPC acts on frames received error-free and discards frames received with errors. The XPC maintains the number of link errors in the counter registers.

### Controller

The controller interprets results from the receiver, transmitter, and internal registers, and implements the actions of the protocol. The X.25/X.75 protocol block contains the logic used to implement the entire X.25/X.75 level 2 protocol. Specific tasks of the main controller include configuring the link as specified by the parameter and command registers, maintaining the status registers, analyzing received frames and taking appropriate action, logging certain events in the bank of 16 event counters, directing the transmitter to send specific commands or responses, directing the interface unit to acquire receive and transmit data buffers, managing timing directions, and using a set of interrupts to notify the host of data link conditions.

### DMA Interface Unit

The interface unit provides the interface between main memory and the transmitter and receiver via 2-channel DMA. It consists of a data bus selector, parity generator and checker, address controller, read/write machine, data section, and DMA controller.

The data bus selector controls the width of the external data bus and data byte ordering. The external data bus can be set at either 8-or 16-bits wide by strapping DBC (pin 17) to $V_{SS}$ or $V_{DD}$, respectively. The internal data bus is 8 bits wide. Data byte ordering is accomplished via parameter register 14, bit 0.

Parity is generated and checked for each byte of the data bus during DMA operations if parity is enabled. Parity is not checked or generated when the host accesses the XPC registers.

The address controller calculates and stores the addresses for the elements and buffer pointers for the transmit and receive channels.

The read/write machine generates the control signals to access data from memory, while the data section routes the data from memory to the transmit FIFO and from the receive FIFO to memory.

The DMA controller, on request from the controller, opens data buffers for the transmitter and receiver and controls the sequencing of the other sections.

A DMA priority scheme can be implemented in a daisy-chain fashion with no additional hardware for multiple XPC applications.

### Loopback Test Control

The loopback test control connects the RD and TD pins, as required by the near-end loopback test, far-end loopback test, or echo mode.

## Principles of Operation

### CPU Interface

The CPU interface is used to specify commands to the XPC and to receive status information from the XPC. The XPC is a peripheral device that accepts commands from the CPU and provides interrupts and results to the CPU when necessary. Through the CPU interface, the CPU loads the command, parameter, and counter registers with the characteristics of the serial interface. The XPC provides status information and interrupts via the status and interrupt registers. The CPU accesses these registers via bits A1—A6 of the address bus. When $\overline{CS}$ is asserted, $\overline{RE}$, $\overline{WE}$, and A1—A6 become inputs and $\overline{READY}$ becomes an output. Only the low-order byte of the data bus is used for register read/write operations. The XPC ignores the upper byte during write operations and forces a 3-state condition on the upper data byte during read operations. The registers always appear on D0—D7, regardless of the byte ordering that is selected. Table 2 lists the register addresses for the XPC.

### Master Reset

When the master reset ($\overline{MR}$) is asserted, the parameter registers are cleared, the command register is set to 82H (DISCMODE = 1, MDISC = 1), and the interrupt register is cleared. Status registers 9—13 and the counter registers are not initialized. $\overline{MR}$ must be high for at least two CLK periods after power-up. The minimum low time for reset is 1.5 CLK periods.

When the XPC detects a reset, it performs an internal reset sequence that requires eight CLK periods. After the reset sequence, the XPC enters a set-up state in which the CPU can configure the parameter and counter registers. While in the set-up state, the XPC transmits 1s and ignores any frames that are received. The XPC exits the set-up state and enters the operational state when the CPU clears MDISC in the command register.

In order to change parameter register values, either the XPC must be placed in the set-up state by a reset or the MDISC bit must be set while the XPC is in the operational state. An exception to this is parameter register 0, which can be configured only in the set-up state.

$\overline{MR}$ is also used with $\overline{CS}$ to provide board isolation capabilities. If $\overline{CS}$ is low when $\overline{MR}$ is asserted, $\overline{INTR}$, $\overline{RTS}$, TD, $\overline{DREQ}$, and $\overline{DACK}$ are placed in a high-impedance state; if $\overline{CS}$ is high when $\overline{MR}$ is asserted, these pins are not put in a high-impedance state. All other outputs are placed in a high-impedance state when $\overline{MR}$ is asserted, regardless of the state of $\overline{CS}$.

### Registers

The XPC contains 51 addressable registers for controlling and observing its operational mode. The registers are divided into five types: command, status, interrupt, parameter, and counter.

**Command Register.** This register controls seven XPC functions: send, receive, mandatory disconnect, active or passive link initialization, password exchange, password verification, and disconnect. The command register can be written to at any time.

**Status Registers.** These 14 registers report the state of the XPC, input conditions, and other vital information regarding the XPC to the CPU; e.g., the values of the state variables V(S) and V(R).

**Interrupt Register.** This register's lower six bits present an encoded reason for a particular interrupt issued to the CPU; for example, packet received, parity error, idle link detected, and frame reject. This register is backed up by a 4-word FIFO, which enables several interrupts to occur before the CPU can service the XPC. Bit 7 contains a lost interrupt bit, which is independent of the LSTIN bit in status register 0 and is implicitly cleared after a read of the interrupt register. If no interrupts are pending, the interrupt register contains 00H.

**Parameter Registers.** These 17 registers determine system constants and the mode of operation, for example, the period of the T1 and T4 timers and the address of the TLOOK table. The XPC can also be put into a test mode to test either itself or itself and the link. These registers can be written to only when MDISC is set. An exception to this is parameter register 0, which can be configured only in the set-up state.

**Counter Registers.** These 18 down-counter registers monitor 16 different events on the data link; for example, the number of rejected frames received, the number of times timer T1 expired, and the number of parity errors generated. The counter registers can be written to at any time.

**Table 2. XPC Register Address Offsets**

| Address | | | | Address | | | |
|---|---|---|---|---|---|---|---|
| Hex | Dec | Status* | Name | Hex | Dec | Status* | Name |
| 00 | 0 | R/W | Command register | 34 | 52 | R/W | Parameter register 10 |
| 02 | 2 | R | Status register 0 | 36 | 54 | R/W | Parameter register 11 |
| 04 | 4 | R | Status register 1 | 38 | 56 | R/W | Parameter register 12 |
| 06 | 6 | R | Status register 2 | 3A | 58 | R/W | Parameter register 13 |
| 08 | 8 | R | Status register 3 | 3C | 60 | R/W | Parameter register 14 |
| 0A | 10 | R | Status register 4 | 3E | 62 | R/W | Parameter register 15 |
| 0C | 12 | R | Status register 5 | 40 | 64 | R/W | Counter register 0 |
| 0E | 14 | R | Status register 6 | 42 | 66 | R/W | Counter register 1 |
| 10 | 16 | R | Status register 7 | 44 | 68 | R/W | Counter register 2 |
| 12 | 18 | R | Status register 8 | 46 | 70 | R/W | Counter register 3 |
| 14 | 20 | R | Status register 9 | 48 | 72 | R/W | Counter register 4 |
| 16 | 22 | R | Status register 10 | 4A | 74 | R/W | Counter register 5 |
| 18 | 24 | R | Status register 11 | 4C | 76 | R/W | Counter register 6 |
| 1A | 26 | R | Status register 12 | 4E | 78 | R/W | Counter register 7 |
| 1C | 28 | R | Status register 13 | 50 | 80 | R/W | Counter register 8 |
| 1E | 30 | R | Interrupt register | 52 | 82 | R/W | Counter register 9 |
| 20 | 32 | R | Parameter register 0 | 54 | 84 | R/W | Counter register 10 |
| 22 | 34 | R/W** | Parameter register 1 | 56 | 86 | R/W | Counter register 11 |
| 24 | 36 | R/W | Parameter register 2 | 58 | 88 | R/W | Counter register 12 |
| 26 | 38 | R/W | Parameter register 3 | 5A | 90 | R/W | Counter register 13 |
| 28 | 40 | R/W | Parameter register 4 | 5C | 92 | R/W | Counter register 14 |
| 2A | 42 | R/W | Parameter register 5 | 5E | 94 | R/W | Counter register 15 |
| 2C | 44 | R/W | Parameter register 6 | 60 | 96 | R/W | Counter register 16 |
| 2E | 46 | R/W | Parameter register 7 | 62 | 98 | R/W | Counter register 17 |
| 30 | 48 | R/W | Parameter register 8 | 64 | 100 | R/W | Parameter register 16 |
| 32 | 50 | R/W | Parameter register 9 | | | | |

* Read/write (R/W) or read-only (R) status.
** Parameter registers can be written only when MDISC is set.

**Table 3. Command Register Definitions**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | DISCMODE | PWOK2 | PWOK1 | PWXCH | ACT/PAS | RECR | MDISC | SEND |

| Bit | Symbol | Name/Description |
|---|---|---|
| 0 | SEND | **Send.** Controls transmission of packets. If cleared, inhibits XPC from sending new packets; if set, enables XPC to send new packets. The XPC clears this bit if the link goes down or if the next transmit element is not ready. Retransmissions occur automatically, regardless of the send bit state. |
| 1 | MDISC | **Mandatory Disconnect.** Selects whether the XPC brings the link up or remains disconnected. If cleared, the XPC brings the link up; if set, the XPC transmits all 1s during fill times and remains disconnected. If the XPC is in the information transfer phase when MDISC is set, it transmits a DISC frame and exits the information transfer phase. Interrupt generation is disabled when MDISC is set and NOTDISC (status register 0) is cleared. MDISC is set during a master reset (see Table 4). |
| 2 | RECR | **Receiver Ready.** Indicates availability of receiver buffers. If cleared, no receiver buffers are available. If set, receiver buffers are allocated and available. The XPC clears this bit if the receiver overruns, if the buffer chain segment is not ready, or if the receive element referenced by V(R) is not ready. If cleared while the XPC is in the information transfer phase, the XPC enters the station busy state and ignores all incoming I frames. |
| 3 | ACT/PAS | **Active/Passive.** Specifies XPC action in the disconnected phase. If cleared, the XPC passively awaits link set-up; if set, the XPC actively initiates link set-up (see Table 4). |
| 4 | PWXCH | **Password Exchange.** Determines which end of the link initiates password exchange. If cleared, the other end of link initiates password exchange; if set, the XPC initiates password exchange. |
| 5, 6 | PWOK1, PWOK2 | **Password Verified.** Enables the host to notify the XPC about the correct action to take in response to a received password. Bits 4, 5, and 6 are interpreted as:<br>**Code** (**b6 b5 b4**) — **Condition**<br>0 1 0 — Valid password command received<br>0 1 1 — Valid password response received<br>1 0 0 — Valid password command not received<br>1 0 1 — Valid password response not received |
| 7 | DISCMODE | **Disconnect Mode.** Specifies a disconnected state. DISCMODE is set during a master reset. DISCMODE must be set for passive link initialization and must be cleared for XID operation (see Table 4). |

**Table 4. Disconnected Phase Operation**

| Protocol State | XIDEN[1] | DISCMODE | ACT/PAS[2] | MDISC | Description |
|---|---|---|---|---|---|
| S0 | 0 | x | x | 1[3] | Does not respond to received frames until MDISC is cleared.[4] Responds to P-bit frame with DM final.[5] |
| S0 | 0 | 0 | 0 | 0 | Responds to P-bit frame with DM final.[6] |
| S1 | 0 | 1 | 0 | 0 | Link can be initialized by remote DXE. |
| x | 0 | x | 1 | 0 | Initiates link setup. |
| S0 | 1 | 0 | 0 | 0 | Waits for XID transfer. |
| S0 | 1 | 0 | 1 | 0 | Initiates XID transfer. |
| S0 | 1 | 0 | x | 1 | Does not respond to received frames until MDISC is cleared. |
| x | 1 | 1 | x | x | Do not use. |

Note: x = don't care.
[1] Password enable bit in parameter register 1.
[2] Use PWXCH instead of ACT/PAS if XIDEN is 1.
[3] Interframe fill is idle (all 1s).
[4] MDISC not yet cleared after reset.
[5] MDISC previously cleared after reset.
[6] Interframe fill is flags.

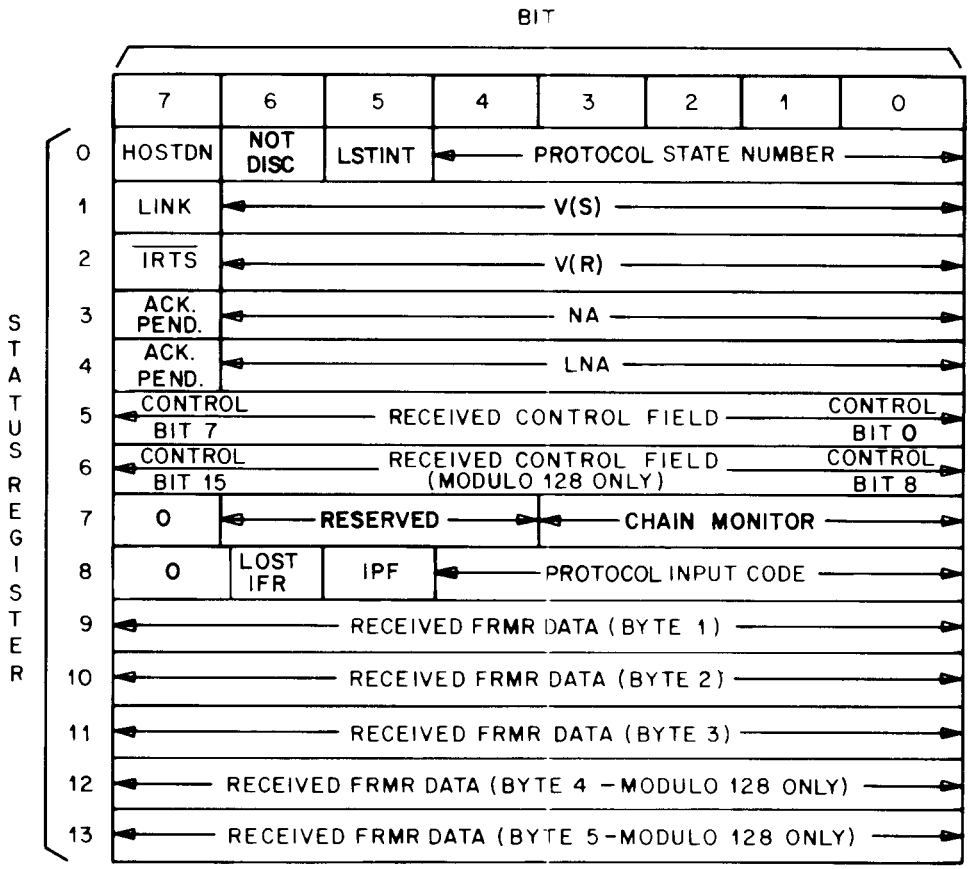



**Figure 3. Status Registers**

**Table 5. Status Registers**

| Reg | Bit | Symbol | Name/Description |
|---|---|---|---|
| 0 | 0—4 | PSN | **Protocol State Number.** Encoding of protocol state (see Table 6). |
| 0 | 5 | LSTINT | **Lost Interrupt.** Indicates if interrupts were lost. If cleared, no interrupts were lost. If set, interrupt register FIFO overflowed and interrupts were lost. This bit is implicitly cleared after a read of status register 0. |
| 0 | 6 | NOTDISC | **Not Disconnected.** This bit is cleared if the XPC is disconnected or in XID phase. It is set when the device is in the link set-up or information transfer phase (protocol state ≥ S3). Interrupt generation is disabled when NOTDISC is cleared and MDISC (command register) is set. |
| 0 | 7 | $\overline{\text{HOSTD}}$ | **Host Done (Active Low).** Allows the internal host done bit to be monitored in the event that the interrupt informing the host of a link-down condition was lost. If set, the host must reassign transmit and receive buffers before link reinitialization is permitted. The XPC sets this bit when an SABM frame is received while the XPC is in the information transfer phase (LINK = 1) or when the XPC exits the information transfer phase (LINK = 0). This bit is cleared by writing to status register 0 or parameter register 1. |
| 1 | 0—6 | V(S) | **Send State Variable.** The sequence number, N(S), of the next I frame to be transmitted and an index into the TLOOK table to access the buffer containing data for that frame. |
| 1 | 7 | LINK | **Link.** Indicates the status of the transmission link. If cleared, information transfer is not possible; if set, the XPC is in the information transfer phase (protocol state ≥ S6). |
| 2 | 0—6 | V(R) | **Receive State Variable.** The expected value of the sequence number, N(S), of the next I frame to be received and an index into the RLOOK table for the receiver buffer associated with that packet. |
| 2 | 7 | $\overline{\text{IRTS}}$ | **Internal Request to Send.** Indicates that the XPC wants to acquire the link. If cleared, XPC wants link; if set, XPC does not want link. |
| 3 | 0—6 | NA | **Next Acknowledgment Expected.** Number of earliest unacknowledged packet. If no outstanding packets, NA = V(S). |
| 3 | 7 | ACKPEND | **Acknowledgments Pending.** This bit is set when the DMA has received acknowledgment processing to do. When all appropriate TLOOK elements have been updated, this bit is cleared. Before the host clears $\overline{\text{HOSTD}}$ or reallocates transmit buffers, it must check that this bit is cleared. |
| 4 | 0—6 | LNA | **Last Next Acknowledgment Expected.** Whenever NA is updated, the old value of NA is saved here. NA and LNA can be used to determine how many transmit data buffers have been acknowledged by the remote DXE and subsequently freed by the XPC. |
| 4 | 7 | ACKPEND | **Acknowledgment Pending.** See ACKPEND description above. |

**Table 5. Status Registers (Continued)**

| Reg | Bit | Symbol | Name/Description |
|---|---|---|---|
| 5 | 0—7 | RCF | **Received Control Field.** Holds the control field of the most recently received error-free frame. |
| 6 | 0—7 | RCF | **Received Control Field.** Holds the second byte of the control field in modulo-128 mode only. If in modulo-8 (normal sequencing), this register is always cleared. |
| 7 | 0—3 | CHMON | **Chain Monitor.** Indicates which chain segment of the receiver buffer is currently being used. |
| 7 | 4—6 | — | **Reserved.** These bits are for internal use and should be masked when reading status register 7. |
| 7 | 7 | — | **Zero.** This bit is always 0. |
| 8 | 0—4 | PIC | **Protocol Input Code.** Contains an encoding of what the protocol considers to be its most recent input stimulus (see Table 7). |
| 8 | 5 | IPF | **Internal Poll/Final Bit.** Last poll/final bit upon which the XPC has acted. This bit is used in conjunction with the protocol input code. |
| 8 | 6 | LSTIFR | **Lost I-Frame.** Cleared for normal operation; set if an I frame is received but no receive buffers are available or if a receiver overrun occurs. This bit is cleared when the XPC exits the station busy condition. |
| 8 | 7 | — | **Zero.** This bit is always 0. |
| 9—11 | 0—7 | RFDF | **Received Frame Project (FRMR) Data Field.** Holds the first, second, and third bytes of data field contained in a received FRMR frame. These registers contain random data until the first FRMR is received. |
| 12, 13 | 0—7 | RFDF | **Received Frame Project (FRMR) Data Field.** Holds the fourth and fifth byte of data field in FRMR frame (modulo-128 only). If in modulo-8 (normal sequencing), these registers always contain random data. |

**Table 6. Status Register 0 — Protocol State Number Encoding**

| State Number | | | | | | State | Description |
|---|---|---|---|---|---|---|---|
| Hex | b4 | b3 | b2 | b1 | b0 | | |
| 00 | 0 | 0 | 0 | 0 | 0 | S0 | Logically disconnected |
| 01 | 0 | 0 | 0 | 0 | 1 | S1 | Logically disconnected |
| 02 | 0 | 0 | 0 | 1 | 0 | S2a | Awaiting XID command |
| 03 | 0 | 0 | 0 | 1 | 1 | S2b | Awaiting XID response |
| 04 | 0 | 0 | 1 | 0 | 0 | S3 | Link set-up initiated |
| 07 | 0 | 0 | 1 | 1 | 1 | S4 | Frame rejected |
| 05 | 0 | 0 | 1 | 0 | 1 | S5 | Disconnect request |
| 06 | 0 | 0 | 1 | 1 | 0 | S6 | Information transfer |

**Table 6. Status Register 0 — Protocol State Number Encoding (Continued)**

| State Number | | | | | | State | Description |
|---|---|---|---|---|---|---|---|
| Hex | b4 | b3 | b2 | b1 | b0 | | |
| 08 | 0 | 1 | 0 | 0 | 0 | S7 | REJ frame sent |
| 09 | 0 | 1 | 0 | 0 | 1 | S8 | Waiting acknowledgment |
| 11 | 1 | 0 | 0 | 0 | 1 | S9 | Station busy |
| 0A | 0 | 1 | 0 | 1 | 0 | S10 | Remote station busy |
| 0F | 0 | 1 | 1 | 1 | 1 | S11 | S9 and S10 |
| 10 | 1 | 0 | 0 | 0 | 0 | S12 | S8 and S9 |
| 0B | 0 | 1 | 0 | 1 | 1 | S13 | S8 and S10 |
| 1A | 1 | 1 | 0 | 1 | 0 | S14 | S8, S9, and S10 |
| 1B | 1 | 1 | 0 | 1 | 1 | S15 | S7 and S9 |
| 0C | 0 | 1 | 1 | 0 | 0 | S16 | S7 and S10 |
| 0D | 0 | 1 | 1 | 0 | 1 | S17 | S7, S9, and S10 |

**Table 7. Status Register 8 — Input Code**

| Input Code* | Description |
|---|---|
| 0 | Local stop – disconnect link |
| 1 | Local start – initiate link set-up |
| 2 | Busy condition clears |
| 3 | Valid XID command received |
| 4 | T1 expired |
| 5 | T3/T4 expired |
| 6 | Station has become busy |
| 7 | I frame available (reset condition also) |
| 8 | Invalid N(S) in last received I frame (X.75) |
| 9 | Unrecognized frame received |
| 10 | I frame received |
| 11 | RNR command received |
| 12 | REJ command received |
| 13 | RR command received |
| 14 | SABM received |
| 15 | DISC received |
| 16 | UA received |
| 17 | FRMR received |
| 18 | DM received |
| 19 | Valid XID response received |
| 20 | Idle link detected for T3 |
| 21 | Incorrect N(S) in last received I frame |
| 23 | N2 exceeded |
| 24 | Invalid N(R) in last received I frame |
| 26 | Initiate password exchange |
| 27 | RNR response received |
| 28 | REJ response received |
| 29 | RR response received |
| 30 | Wait for password exchange |

* This code is represented as a binary number in the 5-bit protocol input code field in the status register.

**Table 8. Interrupt Vector Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | LOST INTERRUPT | 0 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 |

| Code* | Interrupt | Name/Description |
|---|---|---|
| 1 | SABM | **Link Reset Received.** An SABM or SABME command frame was received while the XPC was in the information transfer phase. The link is reinitialized when $\overline{\text{HOSTD}}$ is cleared. |
| 2 | UA | **UA Received While Link is Up.** The XPC initializes the link because an unnumbered response frame was received acknowledging an unnumbered command never sent. The link is reinitialized when $\overline{\text{HOSTD}}$ has been cleared. If in the X.75 mode, a FRMR frame is sent. |
| 3 | DM | **DM Received.** The XPC attempts to initialize the link if it is in active mode because it received an unsolicited, unnumbered response frame indicating that the far end of the link is in a disconnected state. If in the X.75 mode, a FRMR frame is sent. |
| 4 | FRMRR | **Frame Reject (FRMR) Received.** The interrupt is issued after data is stored in status registers 9—13. |
| 5 | DISC | **Received DISC While Link is Up.** This interrupt occurs when a disconnect command is received while the XPC is in the information transfer phase, causing the link to go down. |
| 6 | IDLINK | **Idle Link Detected.** If the XPC detects 15 or more contiguous 1s, it starts timer T3 if T1 is not running. If a flag is not detected before timer T3 expires, an idle link is reported and this interrupt is issued. If timer T1 is running, the XPC waits for T1 to finish before starting T3. |
| 7 | N2EXC | **N2/C2 Counter was Exceeded.** If in the active mode, the XPC attempts to initialize the link because the maximum number of retransmissions (N2) was exceeded. If the XPC is in the password exchange mode, this counter is interpreted as the C2 counter. |
| 8 | RF1P | **F = 1 Received Without Sending P = 1.** This interrupt occurs when a response frame with its final bit set was received but the XPC did not send a command frame with poll bit set. In the X.25 mode, the frame is discarded; in the X.75 mode, the XPC sends a FRMR frame to begin link reset procedures. |
| 9 | LK01 | **Link Is Up.** The XPC goes from the disconnected or link set-up state to the information transfer phase (the logical link has come up). |
| 10 | XIDRCVD | **XID Frame Received.** An XID frame was received and its data field was placed in main memory. |
| 11 | NOXIDR | **No XID Response.** An XID command was transmitted and no response was received in time T4. |

* The code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit and is implicitly cleared after the interrupt register is read. Bit 6 is always 0.

**Table 8. Interrupt Vector Register (Continued)**

| Code* | Interrupt | Name/Description |
|---|---|---|
| 12 | FRMRX–W | **Frame Reject Transmitted – W = 1.**** Receipt of command or response that is invalid or not implemented and cannot be corrected by retransmission. |
| 13 | FRMRX–X | **Frame Reject Transmitted – X = 1.**** Receipt of S or U frame with an information field that is not permitted. |
| 14 | FRMRX–Y | **Frame Reject Transmitted – Y = 1.**** Receipt of an I frame with an information field that exceeds the maximum established length, N1. |
| 15 | FRMRX–Z | **Frame Reject Transmitted – Z = 1.**** Receipt of an invalid N(R). |
| 16 | PKR | **Packet Received.** This interrupt is issued after the XPC has received an I frame and stored its data field in main memory. V(R) points to the next element in the RLOOK table after this interrupt is issued. |
| 17 | XBA | **Transmitted Block Acknowledged.** Issued when the XPC receives acknowledgment for one or more previously transmitted I frames. |
| 18 | RCVOVR | **Receiver Overrun.** The receiver FIFO buffer overflowed because new characters were being brought in faster than DMA could save them in main memory. The receiver FIFO is 4-bytes deep. The XPC clears the RECR bit in the command register when issuing this interrupt. |
| 19 | XUNDR | **Transmitter Underrun.** The transmitter FIFO buffer became empty during transmission and frame was aborted. If the send bit is set, the XPC attempts to retransmit the I frame. The transmit FIFO is 4-bytes deep. |
| 20 | PPROB | **Parity Error.** If the DMA reads a main memory location and an error is detected, the DMA reads that location again. This interrupt is issued if the error is repeated. If an I frame is in transmission, it is aborted. |
| 21 | RLKNRDY | **Receiver Look-Up (RLOOK) Table Not Ready.** The XPC read the RLOOK element referenced by V(R) and found that the RECRDY bit is cleared. It clears the RECR bit in the command register when issuing this interrupt. |
| 22 | LDCHM | **Going to Next Chain Segment.** The DMA has filled a buffer segment and automatically transfers (chains) to the next segment. |
| 23 | BFOVF | **Buffer Overflow (Next Chain Segment Not Ready).** The DMA has read the transfer address before transferring to the next buffer and it was 0. This interrupt occurs only for the receive buffers. XPC clears the RECR bit in the command register when issuing this interrupt. |
| 24 | BADIFLD | **Received I Field is Not an Integral Number of Bytes.** The length of the data field of a received I frame is not an integral number of bytes and the XPC is in byte mode. Bit 5 of byte 0 of the RLOOK element is set. |
| 25 | CTSLST | **Clear-to-Send-Lost.** Clear-to-send ($\overline{CTS}$) input on the XPC went high. The XPC goes into inactive state until $\overline{CTS}$ goes low. |
| 26 | ODAD | **Odd Address.** The TLOOK starting address is odd and the data bus is set for 16-bit operation. The XPC sets MDISC and goes into the set-up state. |

* The code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit and is implicitly cleared after the interrupt register is read.

** W, X, Y, and Z are bits in the information field of a frame reject response that indicates the reason that a frame is being frame rejected. The XPC automatically generates this response.

**Table 8. Interrupt Vector Register (Continued)**

| Code* | Interrupt | Name/Description |
|---|---|---|
| 27 | NOAD | **No Address.** The TLOOK starting address is 0. The XPC sets MDISC and goes into the set-up state. |
| 28 | RCOVF | **Receiver Counter Overflowed.** A data field longer than the maximum 4096 bytes permitted by DMA was received. |
| 29 | LK10 | **Link Is Down.** The XPC goes to a link set-up or disconnected state. $\overline{\text{HOSTD}}$ must be cleared to resume normal operation. |
| 30 | CTSACQ | **Clear-to-Send Acquired.** $\overline{\text{CTS}}$ input went low. |
| 31 | RCLST | **Receive Carrier Lost.** $\overline{\text{CD}}$ input went high. The XPC takes no further action. |
| 32 | CO** | **Countout in Counters 0 and 1.** Register addresses 64 and 66. |
| 33 | CO | **Countout in Counter 17.** Register address 98. |
| 34 | CO | **Countout in Counters 2 and 3.** Register addresses 68 and 70. |
| 35 | CO | **Countout in Counter 16.** Register address 96. |
| 36 | CO | **Countout in Counter 4.** Register address 72. |
| 37 | CO | **Countout in Counter 5.** Register address 74. |
| 38 | CO | **Countout in Counter 6.** Register address 76. |
| 39 | CO | **Countout in Counter 7.** Register address 78. |
| 40 | CO | **Countout in Counter 8.** Register address 80. |
| 41 | CO | **Countout in Counter 9.** Register address 82. |
| 42 | CO | **Countout in Counter 10.** Register address 84. |
| 43 | CO | **Countout in Counter 11.** Register address 86. |
| 44 | CO | **Countout in Counter 12.** Register address 88. |
| 45 | CO | **Countout in Counter 13.** Register address 90. |
| 46 | CO | **Countout in Counter 14.** Register address 92. |
| 47 | CO | **Countout in Counter 15.** Register address 94. |
| 48 | RCACQ | **Receive Carrier Acquired.** $\overline{\text{CD}}$ input went low. The XPC takes no further action. |

* The code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit and is implicitly cleared after the interrupt register is read.

** Interrupt on count-out bit in parameter register 1 must be set for the CO interrupts to occur.

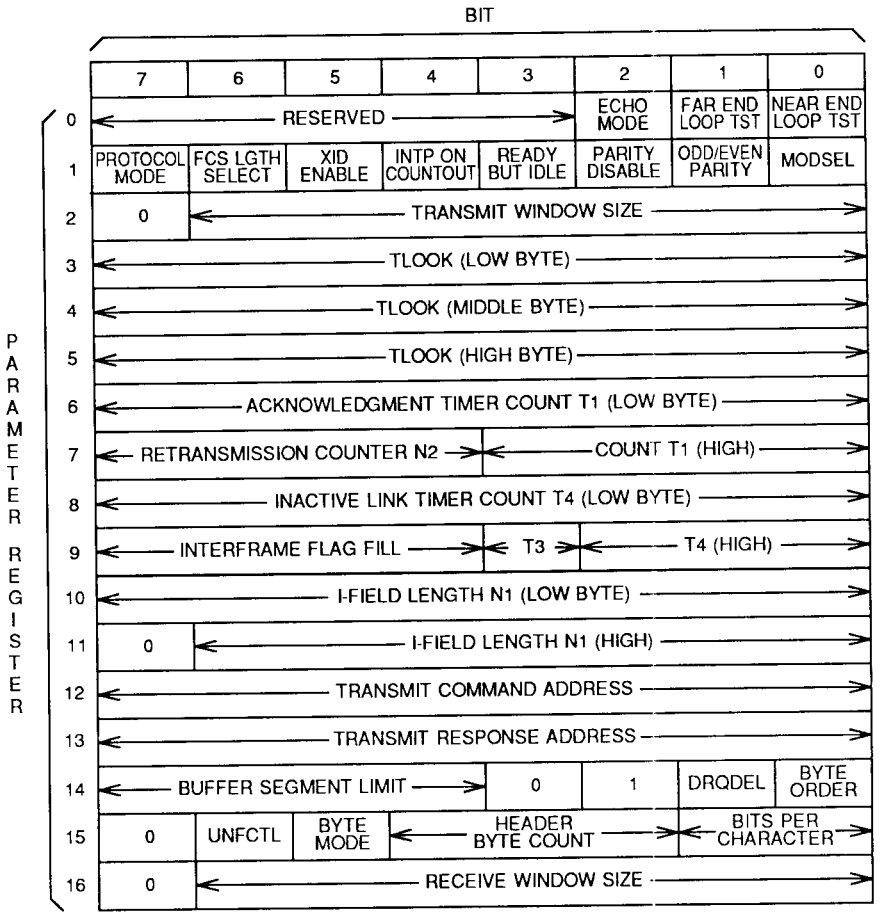



**Figure 4. Parameter Registers**

**Table 9. Parameter Registers**

| Reg | Bit | Symbol | Name/Description |
|---|---|---|---|
| 0 | 0 | NELT* | **Near-End Loop Test.** Setting this bit causes the XPC to enter the near-end loopback test mode. TD and RD are internally tied together; the XPC transmits 1s on TD. Both RC and TC must be applied and must be synchronized with each other. $\overline{CTS}$ must be low. |
| 0 | 1 | FELT* | **Far-End Loop Test.** Setting this bit causes the XPC, in conjunction with link controller at far-end of loop, to enter the far-end loopback test. The remote station must be in echo mode. Both RC and TC must be applied. $\overline{CTS}$ must be low. |
| 0 | 2 | ECHMOD* | **Echo Mode.** Setting this bit causes data coming into receive data (RD) input to appear at transmitter data (TD) output. The XPC takes no action on received frames. Neither RC nor TC need be applied. |
| 0 | 3—7 | — | **Reserved.** These bits are for internal use and are not writable. They should be masked when reading parameter 0. |
| 1 | 0 | MODSEL | **Modulus Select.** If cleared, selects modulo-8, normal sequence numbering; if set, selects modulo-128, extended sequence numbering. |

* These bits cause the specified action only if set after a chip reset and before MDISC is cleared. Only one of these bits can be set for the specified action to occur.

Table 9. Parameter Registers (Continued)

| Reg | Bit | Symbol | Name/Description |
|---|---|---|---|
| 1 | 1 | PARITY | **XPC Parity.** If cleared, even parity; if set, odd parity. |
| 1 | 2 | PARDSB | **Parity Disable.** Setting this bit disables the parity generation and checking capability. The parity pins should not be connected if parity is disabled. |
| 1 | 3 | RDYIDL | **Ready But Idle.** If cleared, the XPC transmits a continuous stream of flags when logically disconnected and not sending frames; if set, the XPC transmits a continuous stream of 1s as interframe fill when logically disconnected. |
| 1 | 4 | INTCO | **Interrupt On Count-Out.** If this bit is set, the XPC issues an interrupt if any of the counter registers are decremented to 0. |
| 1 | 5 | PWDENBL | **Password Enable.** Setting this bit causes the XPC to require a password exchange with far end of link before the link set up is allowed. |
| 1 | 6 | FCSLEN | **FCS Length Select.** If cleared, XPC uses standard 16-bit CRC generator polynomial; if set, XPC uses 32-bit CRC generator polynomial. |
| 1 | 7 | PROTMOD | **Protocol Mode.** If this bit is set, the XPC is in the X.75 mode; if this bit is cleared, the device is in the X.25 mode. |
| 2 | 0—6 | k | **Transmit Window Size.** Maximum allowable number of outstanding I frames (must not equal 0). An outstanding I frame is considered to be any I frame acknowledged by the remote DXE. Valid values are 1—7 for modulo-8 and 1—127 for modulo-128. |
| 2 | 7 | — | **Zero.** This bit is always 0. |
| 3—5 | 0—7 | TLOOK | **Transmit Look-Up Table Pointer.** Starting address in main memory of the first element of the transmit look-up table. |
| 6 | 0—7 | T1 (low byte) | **T1 Timer Period.** This number is proportional to period of the T1 timer: $\text{T1 Count}_{(\text{decimal})} = \frac{\text{fCLK(Hz)}}{16384} \times \text{T1 PERIOD}_{(\text{seconds})}$. It is the maximum time the XPC waits for an acknowledgment. |
| 7 | 0—3 | T1 (high bits) | |
| 7 | 4—7 | N2 | **X.25 Retransmission Counter.** Valid values are 1—15, which determine the maximum number of transmissions and retransmissions of a frame allowed without receiving an acceptable response. |
| 8 | 0—7 | T4 (low byte) | **T4 Timer Period.** A number proportional to period of the T4 timer: $\text{T4 Count}_{(\text{decimal})} = \frac{\text{fCLK(Hz)}}{16384} \times \text{T4 PERIOD}_{(\text{seconds})}$. Maximum time a station allows without frames being exchanged on data link. This parameter is also used as a part of the pseudo-T3 timer. |
| 9 | 0—2 | T4 (high bits) | |

Table 9. Parameter Registers (Continued)

| Reg | Bit | Symbol | Name/Description |
|---|---|---|---|
| 9 | 3 | T3 | **Maximum Idle Time.** Maximum time a station receives an idle condition before resetting the link:<br>If T3 = 0, the period of T3 = the period of T4.<br>If T3 = 1, the period of T3 = T4 period + $\frac{2^{25}}{fCLK(Hz)}$. |
| 9 | 4—7 | FLGFIL | **Interframe Flag Fill.** A weighted code specifying the minimum number of flags to be inserted between frames (see Table 10). |
| 1 | 0—7 | N1 (low byte) | **Maximum I Field Length.** The XPC rejects any I frame whose I Field length exceeds N1 bits. |
| 11 | 0—6 | N1 (high bits) | |
| 11 | 7 | — | **Zero.** This bit is always 0. |
| 12 | 0—7 | TCA | **Transmit Command Address.** Address field of command frames transmitted by the XPC. Address of local station. |
| 13 | 0—7 | TRA | **Transmit Response Address.** Address field of response frames transmitted by the XPC. Address of far-end station. |
| 14 | 0 | BYTORD | **Byte Order.** If cleared, the Intel data bus convention is used for DMA: D7—D0 is even byte; D15—D8 is odd byte. If set, the Motorola data bus convention is used for DMA: D7—D0 is odd byte; D15—D8 is even byte. $\overline{BHE}$ becomes $\overline{BLE}$ when this bit is set (see Figure 9 and Table 18). |
| 14 | 1 | DRQDEC | **DMA Request Delay.** If this bit is set, the DMA logic waits for $\overline{DACK}$ to go high before reasserting $\overline{DREQ}$; if this bit is clear, the DMA logic does not wait for $\overline{DACK}$ to go high before reasserting $\overline{DREQ}$. |
| 14 | 2 | — | **One.** This bit is always 1. |
| 14 | 3 | — | **Zero.** This bit is always 0. |
| 14 | 4—7 | LIMIT | **Limit.** Size of buffer segments for both receiver and transmitter. Buffer segments must be sized in 64-byte multiples:<br>$\text{Limit} = \frac{\text{BUFFER SEGMENT}}{64} - 1.$<br>Maximum buffer segment = 64(1+15) = 1024 bytes. |
| 15 | 0,1 | BPC | **Bits Per Character.** Characters are 5—8 bits in length and are right-justified, with 0s in the most significant bits (see Table 11). |
| 15 | 2—4 | HBC | **Header Byte Count.** Data field of an I frame may consist of a number of characters proceeded by some 8-bit header bytes. This field specifies number of 8-bit bytes in header (see Table 12). |
| 15 | 5 | BYTMOD | **Byte Mode.** If 0, a received fractional byte length data field is permitted; if 1, received I frames must be an integral number of 8-bit bytes. |

**Table 9. Parameter Registers (Continued)**

| Reg | Bit | Symbol | Name/Description |
|---|---|---|---|
| 15 | 6 | UNFCTL | **Unnumbered Control Field Length.** Used in modulo-128 operation only. If cleared, the unnumbered control field is two bytes; if set, the unnumbered control field is one byte. |
| 15 | 7 | — | **Zero.** This bit is always 0. |
| 16 | 0—6 | rk | **Receive Window Size.** Used in X.75 mode only. The maximum allowable number of packets that can be received before an acknowledgment must be sent. Valid values are 1—7 for modulo-8 and 1—127 for modulo-128. |
| 16 | 7 | — | **Zero.** This bit is always 0. |

### Main Memory

Main memory contains data buffers that store transmit and receive data. The pointers used to access these buffers are stored in look-up tables in main memory. The location of data to be transmitted is referenced by pointers in the transmitter look-up table (TLOOK) elements, and the location of data to be received is referenced by pointers in the receiver look-up table (RLOOK) elements.

**Table 10. Interframe Flag Fill**

| Flag Fill Parameter | Minimum Number of Flags |
|---|---|
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 6 |
| 4 | 16 |
| 5 | 18 |
| 6 | 2 |
| 7 | 22 |
| 8 | 64 |
| 9 | 66 |
| 10 | 68 |
| 11 | 70 |
| 12 | 80 |
| 13 | 82 |
| 14 | 84 |
| 15 | 86 |

**Table 11. Bits Per Character Encoding**

| Parameter Register 15 | | Number of Bits per Character |
|---|---|---|
| b1 | b0 | |
| 0 | 0 | 8 |
| 0 | 1 | 7 |
| 1 | 0 | 6 |
| 1 | 1 | 5 |

**Table 12. Header Byte Count**

| Parameter Register 15 | | | Number of Header Bytes |
|---|---|---|---|
| b4 | b3 | b2 | |
| 0 | 0 | 0 | 7 |
| 0 | 0 | 1 | 6 |
| 0 | 1 | 0 | 5 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 3 |
| 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Table 13. Counter Registers**

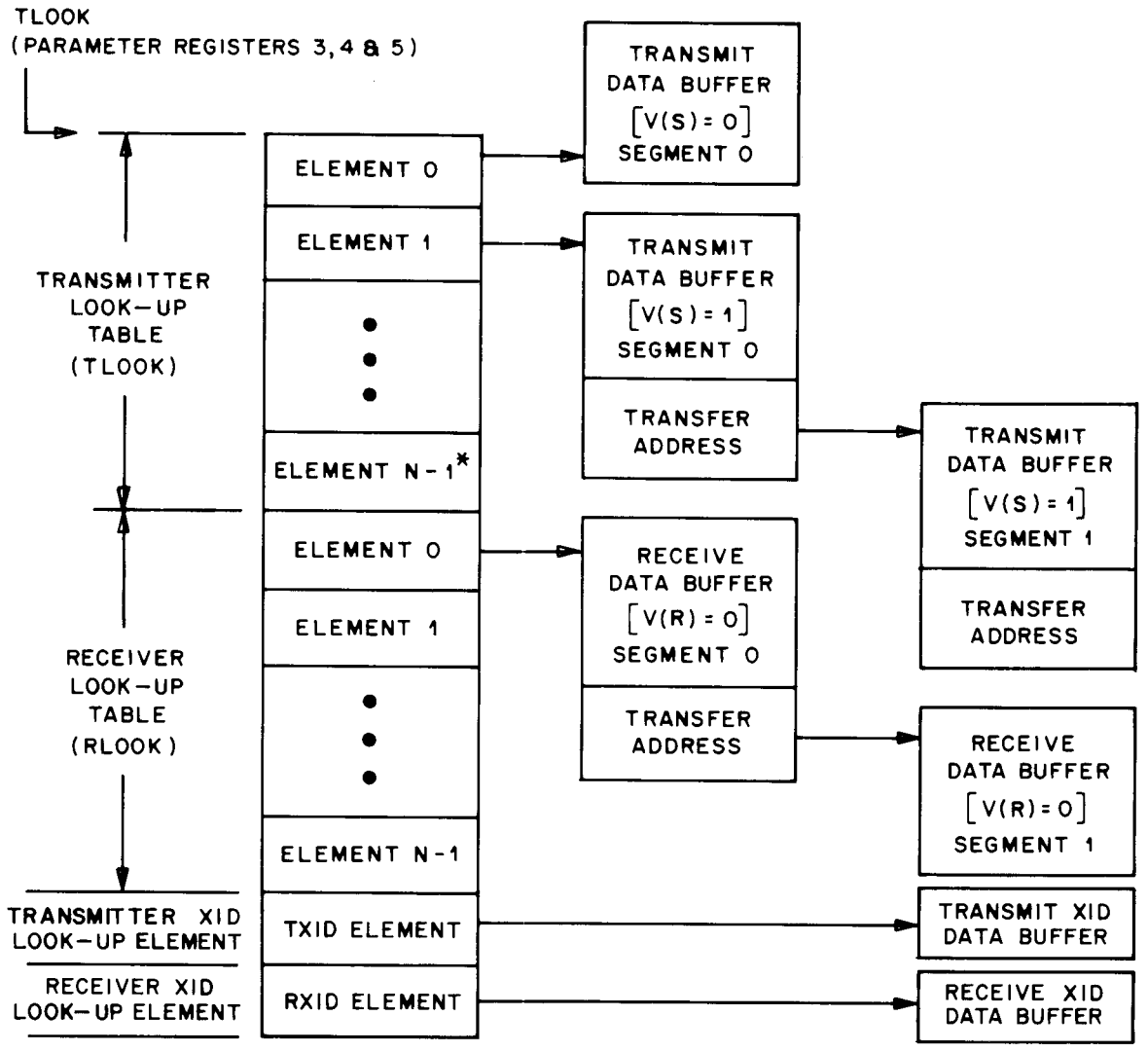
| Counter | Register Number | Description of Event Counted |
|---|---|---|
| | 64 | Supervisory and unnumbered frames received (low byte) |
| 1 | 66 | Supervisory and unnumbered frames received (high byte) |
| 2 | 68 | Supervisory and unnumbered frames sent (low byte) |
| 3 | 70 | Supervisory and unnumbered frames sent (high byte) |
| 4 | 72 | REJ frames received |
| 5 | 74 | REJ frames sent |
| 6 | 76 | RNR frames received |
| 7 | 78 | RNR frames sent |
| 8 | 80 | I frames retransmitted |
| 9 | 82 | Number of times T1 expired |
| 1 | 84 | Null packets received |
| 11 | 86 | Short frames received |
| 12 | 88 | I fields greater than N1 received |
| 13 | 90 | Bad frame check sequences received |
| 14 | 92 | Invalid addresses received |
| 15 | 94 | Invalid control fields received |
| 16 | 96 | Number of aborts received |
| 17 | 98 | Number of parity errors |

The TLOOK table is a list of N 8-byte elements in main memory starting at address TLOOK (stored in parameter registers 3, 4, and 5). N is either 8 or 128 and is determined by the modulus select bit in parameter register 1. Each element in the TLOOK table describes the buffers corresponding to one packet of data to be transmitted by the XPC. The TLOOK list of elements is a circular queue, with element number V(S) at the head.

The RLOOK table is a list of N 8-byte elements in main memory immediately following the TLOOK table. Each element in the RLOOK table describes the buffers corresponding to one packet of data to be received by the XPC. The RLOOK list of elements is a circular queue also, with the element number V(R) at the head.

The XID table is a list of two 8-byte elements in main memory immediately following the RLOOK table. Element 0 is the transmit look-up element (TXID) and element 1 is the receive look-up (RXID) element. These elements are identical to the TLOOK and RLOOK elements, respectively.

When buffer chaining is used and a transfer address of 0 is encountered, the buffer is considered to have ended. Transfer addresses immediately follow the buffers in main memory and are three bytes long (low, middle, and high bytes). Buffer segments must be sized in multiples of 64 bytes. The maximum buffer segment is 1024 bytes. The XPC determines the size of the buffer segment from the limit field in parameter register 14.




Note: Each element consists of 8 bytes. Each transfer address consists of 3 bytes.
* N is either 8 or 128, depending on the sequence numbering modulo select.

**Figure 5. Main Memory Configuration**

### DMA Operation

The XPC uses a dual-channel DMA to read and write the data fields of the I and XID frames and the TLOOK and RLOOK tables. The full 16-bit data bus is used for this operation when the DBC pin is connected to $V_{DD}$. An 8-bit data bus (lower byte of data bus) is used when DBC is connected to $V_{SS}$.

When the XPC is configured for an 8-bit data bus, DMA can begin on even- or odd-byte boundaries for the RLOOK and TLOOK tables and buffers. The XPC reads and writes one byte at a time; the upper data byte (D15—D8) is not used.

When the XPC is configured for a 16-bit data bus, DMA must begin on even-word address boundaries for the RLOOK and TLOOK tables and buffers. $\overline{BHE}/\overline{BLE}$ from the DMA controller is used to access the odd byte of a 16-bit word. $\overline{BHE}/\overline{BLE}$ allows individual selection of even bytes (A0 = 0, $\overline{BHE}/\overline{BLE}$ = 1) or both odd and even bytes as words (A0 = 0, $\overline{BHE}/\overline{BLE}$ = 0).

When BYTORD is high, the data bus is configured in the Motorola mode. $\overline{BHE}$ is then considered to be $\overline{BLE}$. The odd byte appears on D7—D0 (see Figure 9 and Table 18).

To initiate a DMA bus cycle, the XPC requests the use of the bus by forcing $\overline{DREQ}$ low. The host CPU indicates that the bus is available by forcing $\overline{DACK}$ low. This allows $\overline{RE}$, $\overline{WE}$, R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$, A0—A23, and $\overline{AS}$ to become outputs and $\overline{READY}$ to become an input. Once the DMA has control of the bus, it expects to have use of the bus until it has finished its DMA operation. For some operations, the DMA can request the use of the bus within two CLK periods after it has relinquished bus control. For those applications where $\overline{DACK}$ is quick enough to respond within two CLK periods, DRQDEL in parameter register 14 can be cleared. If $\overline{DACK}$ is slow to respond, DRQDEL must be set high.

Slow memory handshaking is provided through the $\overline{READY}$ input. The DMA holds a read or write until it samples $\overline{READY}$ low.

When instructed to open a transmit element, the DMA calculates the address of the particular TLOOK element from the TLOOK base address and the value of V(S), and proceeds to read the bytes of the element. If the BRDY bit in the first byte is 0, the DMA aborts the TLOOK read. The XPC clears the SEND bit in the command register and information transmission is suspended. If BRDY is high, the DMA continues to read the TLOOK element, placing the transmit count in a byte counter and the transmit buffer pointer in an address counter register. The DMA then fetches the data to be transmitted from memory and routes it to the transmitter FIFO. The transmitter signals the DMA for more data when the transmit FIFO contains two bytes or less. The loading process ends when the number of bytes specified by the transmit count has been loaded into the transmit FIFO. The DMA then places this TLOOK element in the not-acknowledged state by setting the NACK bit and clearing the BRDY bit in the element. The TLOOK element is available for retransmission when in this configuration.

When an acknowledgment is received, the DMA clears the NACK bit and sets the ACK bit of all the TLOOK elements whose information buffers have been acknowledged. The DMA then issues an XBA interrupt to indicate that the data associated with one or more TLOOK elements has been acknowledged. The host can then reallocate the TLOOK elements to send more information frames.

When instructed to open a receive element, the DMA calculates the address of the particular RLOOK element from the TLOOK base address and the value of V(R) and proceeds to read the bytes of the element. If the RECRDY bit in the first byte is 0, the DMA aborts the RLOOK read. The XPC clears the RECR bit in the command register and any information frames that are received are discarded. If RECRDY is high, the DMA continues to read the RLOOK element, placing the receive buffer pointer in an address counter register.

When the receive FIFO contains two or more bytes of data, the DMA routes the data from the FIFO and writes it out to memory. The DMA continues to write data to memory until it is notified by the receiver of an end-of-frame condition. At this time, the DMA flushes out the receive FIFO and updates the RLOOK element with the number of bytes received and places the element in the frame-complete state. The DMA then issues a PKR interrupt, notifying the host that an information frame was received and that the data was placed in memory. The host can then reinitialize the RLOOK element in anticipation of receiving more information frames.

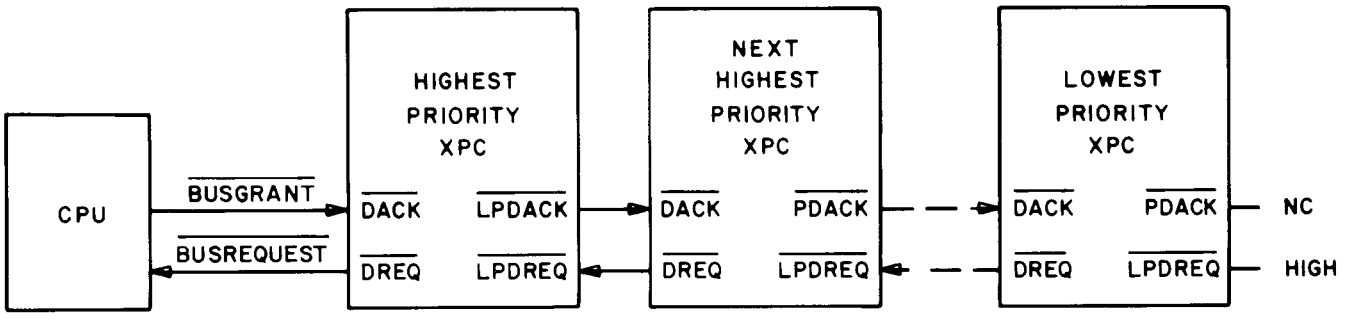



**Figure 6. DMA Priority Scheme Interconnection**

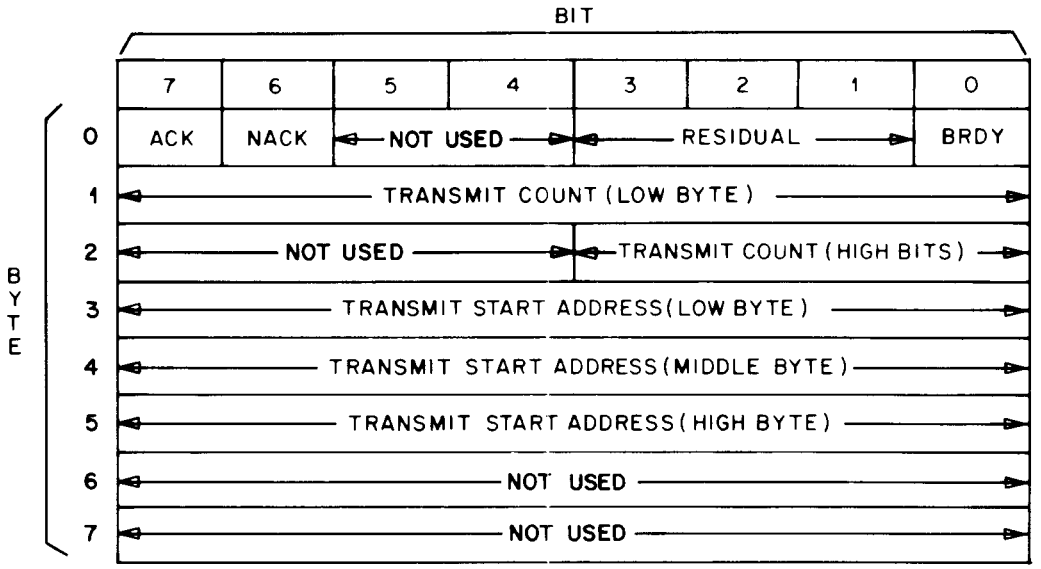



**Figure 7. TLOOK Element Layout**

The DMA accesses the transmit and receive buffers two bytes at a time when configured for 8-bit data buses and one word at a time when configured for 16-bit data buses. If the number of bytes in the buffer is odd, the last access is a single byte access.

A priority DMA bus arbitration scheme can be implemented with no additional hardware by using a daisy chain for multiple XPC applications. The $\overline{\text{DREQ}}$ pin of the lowest priority XPC is tied to the $\overline{\text{LPDREQ}}$ input of the next highest priority XPC. $\overline{\text{DREQ}}$ for the highest priority XPC is tied to the HOLD input of the CPU. The hold acknowledge output of the CPU is tied to the $\overline{\text{DACK}}$ of the highest priority XPC. The $\overline{\text{PDACK}}$ of the highest priority XPC is tied to $\overline{\text{DACK}}$ of the next highest priority XPC and this continues until the lowest priority XPC is reached. The $\overline{\text{LPDREQ}}$ input of the lowest priority XPC must be tied high.

**CAUTION:** When resetting an XPC in a chain, $\overline{\text{CS}}$ must be held high for that XPC. If $\overline{\text{CS}}$ is low when the XPC is reset, the outputs are 3-stated and the propagated request and acknowledge signals are disrupted.

**Table 14. TLOOK Elements**

| Byte | Bit | Symbol | Name/Description |
|---|---|---|---|
| 0 | 0 | BRDY | **Buffer Ready.** Setting this bit tells the XPC that data associated with this element is ready to be transmitted. BRDY is the last bit to be set by CPU. After all the data of a frame has been accessed, the XPC clears the BRDY bit and sets the NACK bit of the associated element. If the NACK bit is set, BRDY also indicates that the buffer is available to the XPC for retransmission. |
| 0 | 1—3 | TRRES | **Residual.** The XPC allows the CPU to select the number of bits that should be transmitted from the last byte of data (see Table 15.) When in byte mode, there should be no residual bits. |
| 0 | 4, 5 | — | **Spare.** Not used. |
| 0 | 6 | NACK | **Not Acknowledged.** The XPC sets this bit after all the data has been accessed; the XPC clears this bit when the packet associated with this element is acknowledged. |

**Table 14. TLOOK Elements (Continued)**

| Byte | Bit | Symbol | Name/Description |
|---|---|---|---|
| 0 | 7 | ACK | **Acknowledged.** The XPC sets this bit when a packet associated with this element becomes acknowledged and generates an XBA interrupt to the CPU. Only then may the CPU reuse this buffer. |
| 1<br>2 | 0—7<br>0—3 | TRCNT | **Transmit Count.** The number of bytes in a data packet associated with this element is acknowledged and generates an XBA interrupt to the CPU. |
| 2 | 4—7 | — | **Spare.** Not used. |
| 3—5 | 0—7 | TRSA | **Transmit Start Address.** This 24-bit number is the location in main memory of the first byte of data in the packet associated with this element. |
| 6, 7 | 0—7 | — | **Spare.** Not used. |

**Table 15. TLOOK Residual Field**

| TLOOK Element Byte 0 | | | Bits Transmitted From Last Memory Byte |
|---|---|---|---|
| 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 7 |
| 0 | 1 | 0 | 6 |
| 0 | 1 | 1 | 5 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 3 |
| 1 | 1 | 0 | 2 |
| 1 | 1 | 1 | 1 |

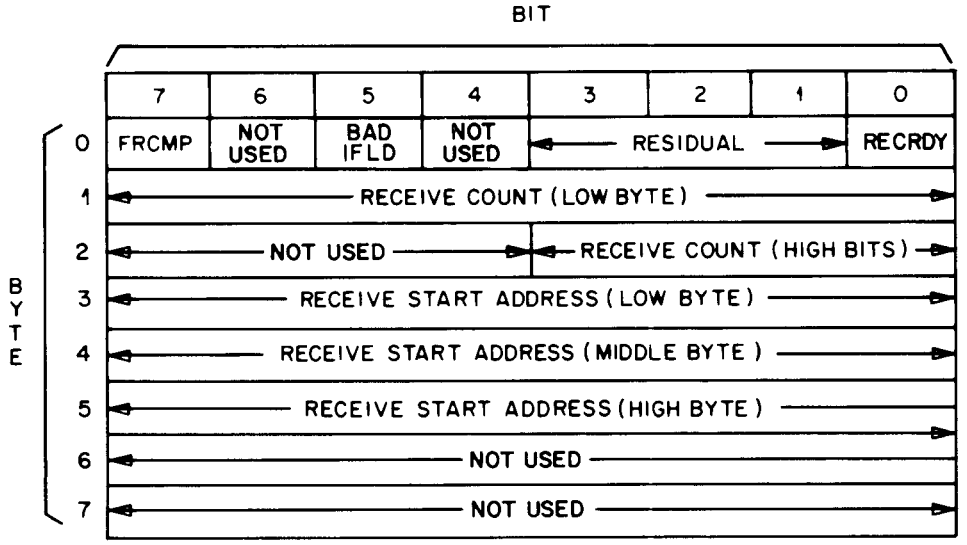



**Figure 8. RLOOK Element Layout**

**Table 16. RLOOK Elements**

| Byte | Bit | Symbol | Name/Description |
|---|---|---|---|
| 0 | 0 | RECRDY | **Receiver Ready.** Setting this bit tells the XPC that the data buffer associated with this element is ready to receive data. All fields of the RLOOK element should be initialized before the CPU sets the RECRDY bit. After the XPC receives a valid packet and stores it in memory, it clears the RECRDY bit of the associated element. |
| 0 | 1—3 | RCVRES | **Residual Bits.** After the XPC receives a frame, it writes the number of bits stored in the last byte into the residual bits field (see Table 17). |
| 0 | 4 | — | **Spare.** Not used. |
| 0 | 5 | BADIFLD | **Bad Information Field.** A fractional byte length frame was received and stored in the buffer pointed to by this element. The XPC also generates a BADIFLD interrupt. This bit is set only if the XPC is in byte mode. |
| 0 | 6 | — | **Spare.** Not used. |
| 0 | 7 | FRCMP | **Frame Complete.** When a valid I frame is received, the XPC writes the receive count, clears RECRDY, and sets FRCMP. A PKR interrupt is generated to notify the CPU of the received packet. |
| 1 | 0—7 | RCVCNT | **Receiver Count.** This 12-bit number specifies how many bytes of memory have been filled by the packet. The XPC writes this after the I frame has been received. |
| 2 | 4—7 | — | **Spare.** Not used. |
| 3—5 | 0—7 | RCVSA | **Receive Start Address.** This 24-bit address is the location in main memory of the first byte of received data for the packet. |
| 6, 7 | 0—7 | — | **Spare.** Not used. |

**Table 17. RLOOK Residual Field**

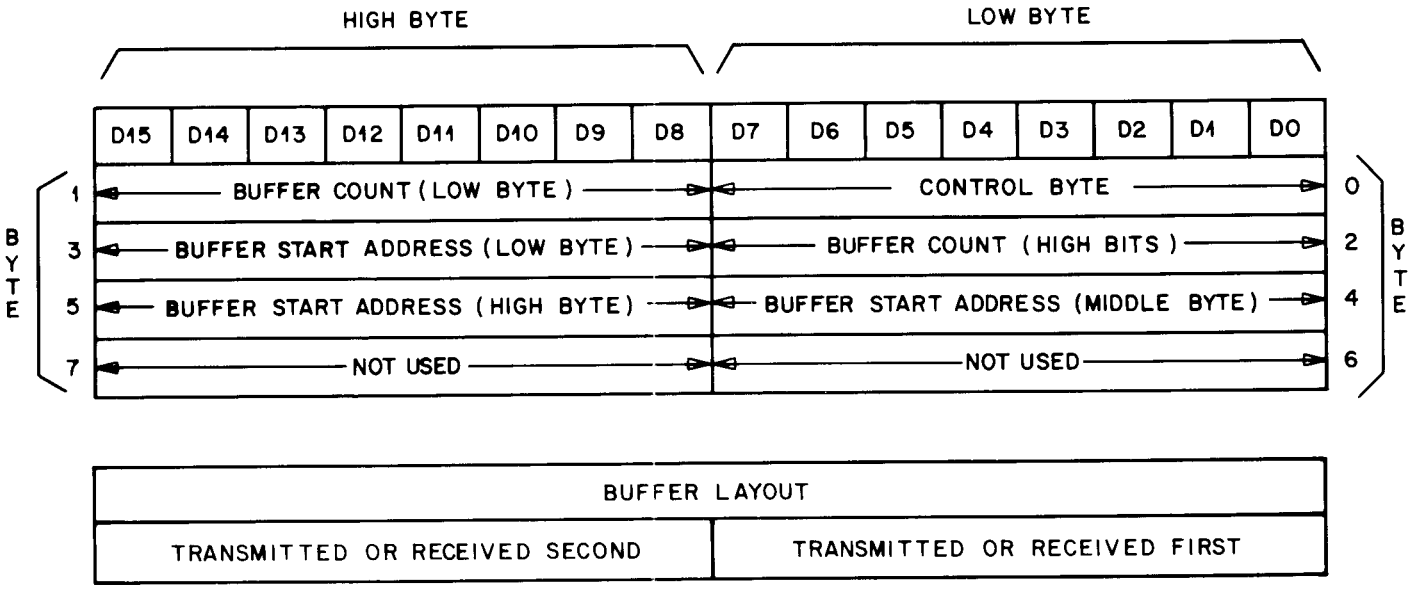
| RLOOK Byte 0 | | | Received Bits in Last Memory Character Bits per Character* | | | |
|---|---|---|---|---|---|---|
| b3 | b2 | b1 | 8 | 7 | 6 | 5 |
| 0 | 0 | 0 | 8 | 7 | 6 | 5 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 2 | 2 | 2 | 2 |
| 0 | 1 | 1 | 3 | 3 | 3 | 3 |
| 1 | 0 | 0 | 4 | 4 | 4 | 4 |
| 1 | 0 | 1 | 5 | 5 | 5 | x |
| 1 | 1 | 0 | 6 | 6 | x | x |
| 1 | 1 | 1 | 7 | x | x | x |

* x = don't care.

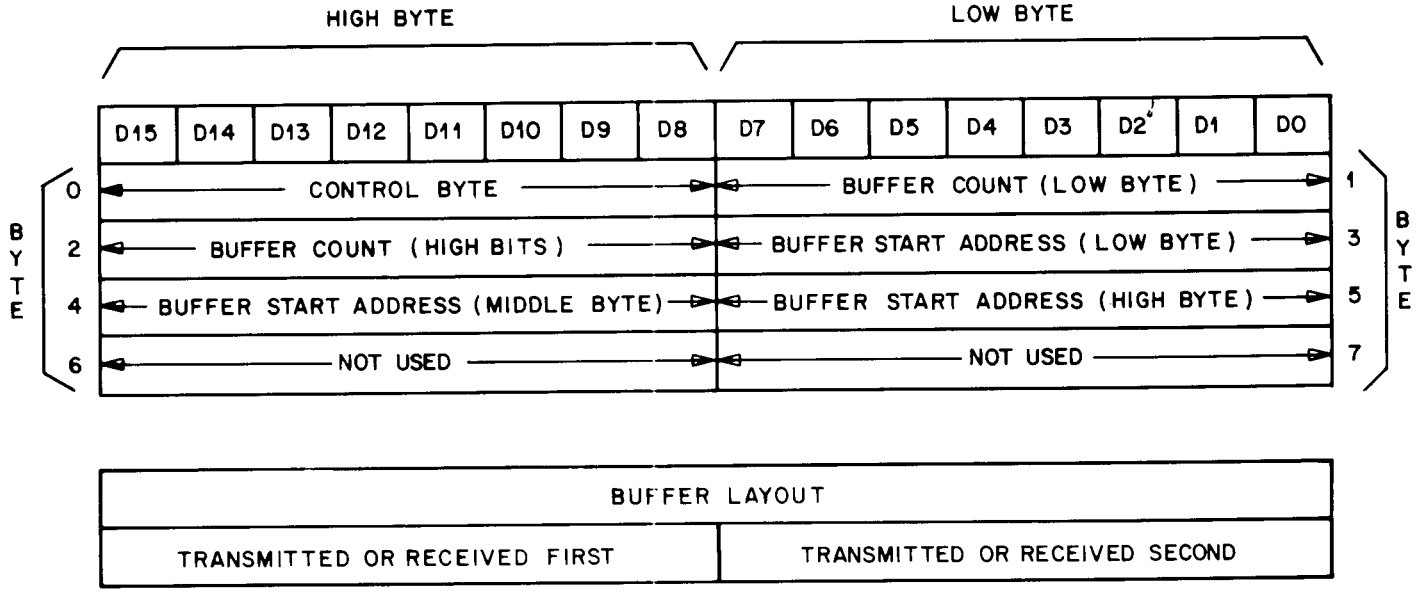
**Table 18. Intel and Motorola Modes***

| Bits | | Mode | Read | | Write | |
|---|---|---|---|---|---|---|
| BYTORD | $\overline{BHE}/\overline{BLE}$ | | D15—D8 | D7—D0 | D15—D8 | D7—D0 |
| 0 | 0 | Intel | Input | Input | Output | Output |
| 0 | 1 | Intel | 3-state | Input | 3-state | Output |
| 1 | 0 | Motorola | Input | Input | Output | Output |
| 1 | 1 | Motorola | Input | 3-state | Output | 3-state |

* DBC = 1; AO = 0.




**a. Receive or Transmit Element in Intel Mode (BYTORD = 0)**




**b. Receive or Transmit Element in Motorola Mode (BYTORD = 1)**

Note: The above figures explain how the elements are laid out in memory for each value of BYTORD in 16-bit mode (DBC = 1).

**Figure 9. Receive or Transmit Element Layout**

# Characteristics

## Electrical Characteristics

$T_A$ = 0 to 70 °C, $V_{DD}$ = 5 V ± 0.25%, $V_{SS}$ = 0 V

| Parameter | Symbol | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Input voltage: | | | | | |
| low | $V_{IL}$ | −0.5 | 0.8 | V | — |
| high | $V_{IH}$ | 2.0 | $V_{DD}$ | V | — |
| Output voltage: | | | | | |
| low | $V_{OL}$ | — | 0.45 | V | $I_{OL}$ = 1.7 mA |
| high | $V_{OH}$ | 2.4 | — | V | $I_{OH}$ = −400 μA |
| Power supply current | $I_{DD}$ | — | 400 | mA | — |
| Input current | | | | | |
| high | $I_{IH}$ | — | 10 | μA | $V_{IH}$ = 5.25 V |
| Output float current: | | | | | |
| low | $I_{OZL}$ | — | −10 | μA | $V_{OL}$ = 0.4 V |
| high | $I_{OZH}$ | — | 10 | μA | $V_{OH}$ = 5.25 V |
| Power dissipation | PD | — | 2.0 | W | $V_{DD}$ = 5.0 |

### Maximum Ratings

Ambient operating temperature ($T_A$) range ..... 0 to 70 °C
Storage temperature (Tstg) range ..... −65 to +125 °C
Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Power dissipation (PD) ..... 2.8 W

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

## Timing Characteristics

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| **Clock Timing** (Figure 10) | | | | |
| tCKHCKL | CLK high time | 240 | 3760 | ns |
| tCKLCKH | CLK low time | 240 | 3760 | ns |
| tCKHCKH | CLK period (sum of tCKHCKL and tCKLCKH) | 500 | 4000 | ns |
| **Receive Clock Timing** (Figure 11) | | | | |
| tRCHRCL | RC high time | 3tCKHCKH | — | — |
| tRCLRCH | RC low time | 3tCKHCKH | — | — |
| tRCHRDX | RD hold time | 1.5CKHCKH | — | — |
| tRDVRCH | RD set-up time | 1.5CKHCKH | — | — |

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| **Transmit Clock Timing** (Figure 12) | | | | |
| tTCHTCL | TC high time | 3tCKHCKH | — | — |
| tTCLTCH | TC low time | 3tCKHCKH | — | — |
| tTCLTDX | TD transition delay | tCKHCKH | 2.5tCKHCKH | — |
| **Reading XPC Registers** (Figure 13) | | | | |
| tAVREL | Address set-up time | 0 | — | ns |
| tREHAX | Address hold time | 0 | — | ns |
| tCSLREL | $\overline{CS}$ set-up time | 0 | — | ns |
| tREHCSX | $\overline{CS}$ hold time | 0 | — | ns |
| tCKHRYL | $\overline{READY}$ wait propagation time | tCKHCKL$_{MIN}$ + tCKLRYL + 10 ns | 13.5tCKHCKH + tCKLRYL | — |
| tCKLRYL | $\overline{READY}$ transition delay | 0 | 265 | ns |
| tREHRYH | $\overline{READY}$ hold time after $\overline{RE}$ goes high | 210 | — | ns |
| tREHREL | Interoperation delay time | tCKHCKH | — | — |
| tRELCKH | $\overline{RE}$ set-up time for ready wait propagation | 120 | — | ns |
| tDVCKL | Data valid set-up time for event counter registers | 25 | — | ns |
| tCSLDV | Time to data valid for nonevent counter registers | 50 | 250 | ns |
| tCSHDZ | Data hold time | 0 | — | ns |
| tAVDX | Data hold time | 0 | — | ns |
| tCSHRYX | $\overline{READY}$ hold time after $\overline{CS}$ goes high | 0 | 50 | ns |
| **Writing XPC Registers** (Figure 14) | | | | |
| tAVWEL | Address set-up time | 0 | — | ns |
| tRYLAX | Address hold time | 0 | — | ns |
| tCSLWEL | $\overline{CS}$ set-up time | 0 | — | ns |
| tRYLCSX | $\overline{CS}$ hold time | 0 | — | ns |
| tWELDV | Data set-up time | — | tCKHCKL$_{MIN}$ | — |
| tRYLDX | Data hold time | 0 | — | ns |
| tWELCKH | $\overline{WE}$ set-up time for ready wait propagation | 140 | — | ns |
| tRYLWEH | $\overline{WE}$ hold time | 0 | — | ns |
| tCKHRYL | $\overline{READY}$ wait propagation time | 3tCKHCKH + tCKLRYL | 13.5tCKHCKH + tCKLRYL | — |
| tCKLRYL | $\overline{READY}$ transition delay | 0 | 265 | ns |
| tWEHRYH | $\overline{READY}$ hold time after $\overline{WE}$ goes high | 245 | — | ns |

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| | **Writing XPC Registers** (Figure 14) | | | |
| tWEHWEL | Interoperation delay time | tCKHCKH | — | — |
| tCSHRYX | $\overline{\text{READY}}$ hold time after $\overline{\text{CS}}$ goes high | 0 | 50 | ns |
| | **DMA Read Cycle** (Figure 15) | | | |
| tCKLDRL | $\overline{\text{DREQ}}$ transition delay | — | 265 | ns |
| tCKHDRH | $\overline{\text{DREQ}}$ transition delay | — | 175 | ns |
| tDALCKL | $\overline{\text{DACK}}$ set-up time | 160 | — | ns |
| tDRHDAH | $\overline{\text{DACK}}$ response time to removal of $\overline{\text{DREQ}}$:<br>DRQDEL = 0<br>DRQDEL = 1 | <br>0<br>0 | <br>tCKHCKH<br>— | <br>—<br>ns |
| tDALRWV | R/$\overline{\text{W}}$, $\overline{\text{BHE}}$/$\overline{\text{BLE}}$ delay time from $\overline{\text{DACK}}$ low | — | 200 | ns |
| tCKLAV | Address valid delay time from CLK low | — | 325 | ns |
| tCKHASL | $\overline{\text{AS}}$ transition delay | — | 160 | ns |
| tCKHASH | $\overline{\text{AS}}$ transition delay | — | 185 | ns |
| tCKLREL | $\overline{\text{RE}}$ transition delay | — | 125 | ns |
| tCKHREH | $\overline{\text{RE}}$ transition delay | — | 190 | ns |
| tRYLCKH | $\overline{\text{READY}}$ set-up time | 70 | — | ns |
| tCKLRYH | $\overline{\text{READY}}$ hold time | 50 | — | ns |
| tDVCKL | Data set-up time<br>without parity<br>with parity | <br>50<br>120 | <br>—<br>— | <br>ns<br>ns |
| tCKHDX | Data hold time | 130 | — | ns |
| tRELREH | Minimum read strobe | 1.5tCKHCKH | — | — |
| tCKHRWZ | R/$\overline{\text{W}}$, $\overline{\text{BHE}}$/$\overline{\text{BLE}}$ hold time | 0 | 220 | ns |
| tCKHAZ | Address hold time | 0 | 290 | ns |
| tCKHASZ | $\overline{\text{AS}}$ hold time | 0 | 220 | ns |
| tCKHREZ | $\overline{\text{RE}}$ hold time | 0 | 220 | ns |
| | **DMA Multiple Byte Read Operation** (Figure 16) | | | |
| tASHASL | Address transition and set-up time | — | tCKHCKH | — |
| tREHREL | Delay time between read operations | | | |
| tCKLDRH* | DMA bus access time:<br>DBC = 0<br>DBC = 1 | <br>4.5tCKHCKH**<br>4.5tCKHCKH** | <br>19.5tCKHCKH†<br>10.5tCKHCKH†† | <br>—<br>— |

| | | | | |
|---|---|---|---|---|
| **DMA Write Cycle** (Figure 17) | | | | |
| tCKLDRL | $\overline{DREQ}$ transition delay | — | 265 | ns |
| tCKHDRH | $\overline{DREQ}$ transition delay | — | 175 | ns |
| tDALCKL | $\overline{DACK}$ set-up time | 140 | — | ns |
| tDRHDAH | $\overline{DACK}$ response time to removal of $\overline{DREQ}$:<br>DRQDEL = 0<br>DRQDEL = 1 | <br>0<br>0 | <br>tCKHCKH<br>— | <br>—<br>ns |
| tDALRWV | R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ delay time from $\overline{DACK}$ low | — | 200 | ns |
| tCKLAV | Address valid delay time from CLK low | — | 325 | ns |
| tCKHASL | $\overline{AS}$ transition delay | — | 160 | ns |
| tCKHASH | $\overline{AS}$ transition delay | — | 185 | ns |
| tCKLWEL | $\overline{WE}$ transition delay | — | 135 | ns |
| tCKLWEH | $\overline{WE}$ transition delay | — | 180 | ns |
| tRYLCKL | $\overline{READY}$ set-up time | 35 | — | ns |
| tCKLRYH | $\overline{READY}$ hold time | 60 | — | ns |
| tCKLDV | Data valid delay time | — | 260 | ns |
| tCKLDX | Data hold time | tCKHCKH | — | — |
| tWELWEH | Minimum write strobe | tCKHCKH | — | — |
| tCKHRWZ | R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ hold time | 0 | 220 | ns |
| tCKHAZ | Address hold time | 0 | 290 | ns |
| tCKHASZ | $\overline{AS}$ hold time | 0 | 220 | ns |
| tCKHWEZ | $\overline{WE}$ hold time | 0 | 220 | ns |
| tCKHDZ | Data time to 3-state | — | 0 | ns |
| **DMA Multiple Write Operation** (Figure 18) | | | | |
| tCKLBEH | $\overline{BHE}$/$\overline{BLE}$ transition delay | — | 210 | ns |
| tASHASL | Address transition and set-up time | tCKHCKH | 2tCKHCKH | — |
| tWEHWEL | Delay time between write operations | 2tCKHCKH | 3tCKHCKH | — |
| tCKLDRH* | DMA bus access time:<br>DBC = 0<br>DBC = 1 | <br>4.5tCKHCKH**<br>4.5tCKHCKH** | <br>11.5tCKHCKH†<br>8.5tCKHCKH†† | <br>—<br>— |

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| **DMA Daisy Chain Timing** (Figure 19) | | | | |
| tLDLCKL | $\overline{\text{LPDREQ}}$ set-up time to be sampled low | 70 | — | ns |
| tCKLDRL | $\overline{\text{DREQ}}$ transition delay after $\overline{\text{LPDREQ}}$ is sampled low | — | 265 | ns |
| tDALPDL | $\overline{\text{PDACK}}$ transition delay after $\overline{\text{DACK}}$ goes low | — | 170 | ns |
| tLDHDRH | $\overline{\text{DREQ}}$ transition delay after $\overline{\text{LPDREQ}}$ goes high | — | 140 | ns |
| DRQDEL = 0: tLDHCKL | $\overline{\text{LPDREQ}}$ set-up time to be sampled high | 75 | — | ns |
| tCKLDRL | $\overline{\text{DREQ}}$ transition delay after $\overline{\text{LPDREQ}}$ is sampled high and XPC is requesting bus time | tCKHCKH | — | — |
| tCKLPDH | $\overline{\text{PDACK}}$ transition delay after $\overline{\text{LPDREQ}}$ is sampled high | — | 160 | ns |
| tCKLDRL | Delay time between XPC relinquishing bus and requesting bus due to lower priority XPC | tCKHCKH | — | — |
| tDRHDAH | $\overline{\text{DACK}}$ response time to removal of $\overline{\text{DREQ}}$ | 0 | tCKHCKH | — |
| DRQDEL = 1: tLDHPDH | $\overline{\text{PDACK}}$ transition delay after $\overline{\text{LPDREQ}}$ goes high | — | 410 | ns |
| tDAHCKL | $\overline{\text{DACK}}$ set-up time to be sampled high | 20 | — | ns |
| tCKLDRL | $\overline{\text{DREQ}}$ transition delay after $\overline{\text{DACK}}$ is sampled high | — | 220 | ns |
| **Interrupt Timing** (Figure 20) | | | | |
| tCKLINTL | Interrupt transition delay | 0 | 140 | ns |
| tREHINTH | Interrupt transition delay | 0 | 150 | ns |
| tINTHINTL | Time before next interrupt | 1.5tCKHCKH | — | — |
| **Reset Timing** (Figure 21) | | | | |
| tCKLMRL | Time before asserting $\overline{\text{MR}}$ after power-on | 2tCKHCKH | — | — |
| tMRLMRH | Reset pulse width | 1.5tCKHCKH | — | — |

* No parity errors and no wait states generated.
** 1-byte or word read.
† 6-byte read
†† 3-word read.

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Transmit Element Acknowledgement** (Figure 22) | | | | | |
| tCKLDRH | DMA bus access time* | — | 8.5tCKHCKH | — | — |
| tCKLRWL | R/$\overline{W}$ transition delay | 0 | — | 160 | ns |
| tASHASL | Address transition and set-up time | — | 3tCKHCKH | — | — |
| tREHWEL | Interoperation delay time | — | 3.5tCKHCKH | — | — |

* No parity errors and no wait states generated.

## Timing Diagrams

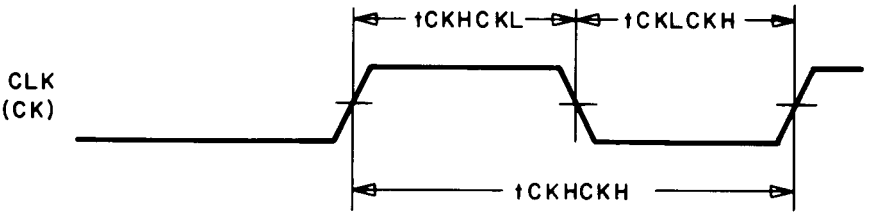
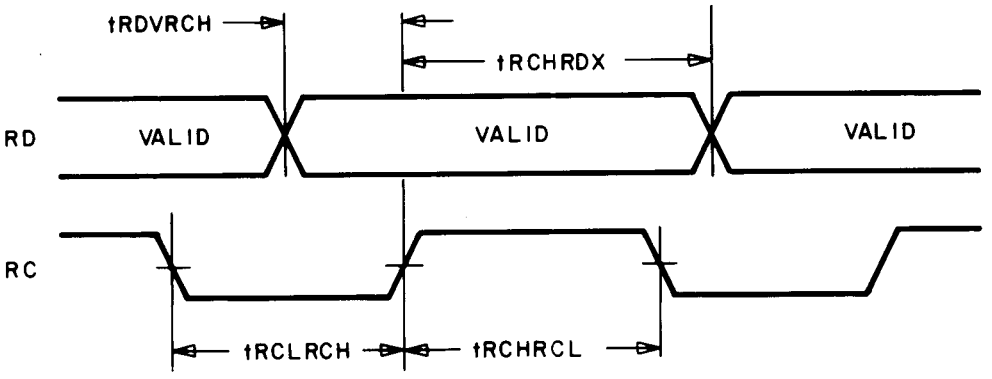



**Figure 10. Clock Timing**




Note: When in loopback modes and TC is tied to RC, the maximum delay on TD (tTCLTDX) meets the minimum RD set-up time (tRDVRCH) up to the maximum fTC = 6fCLK and fRC = 6fCLK.

**Figure 11. Receive Clock Timing**

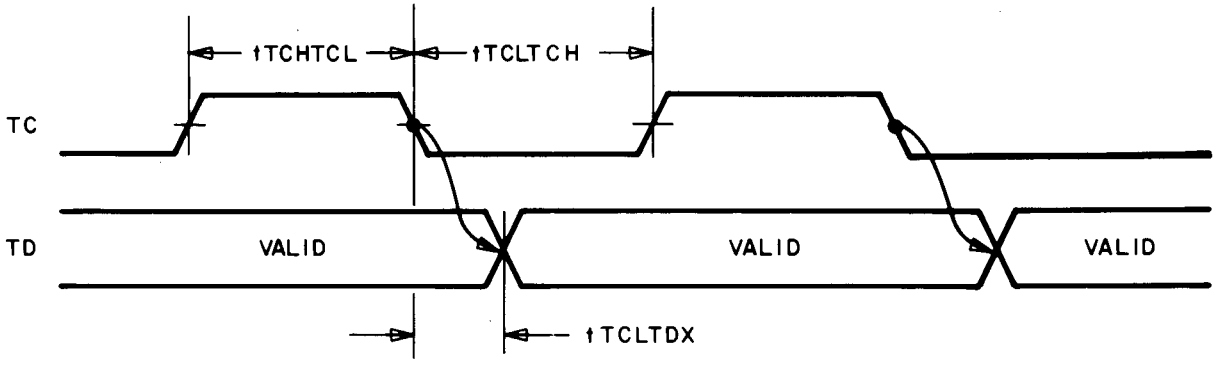



**Figure 12. Transmit Clock Timing**

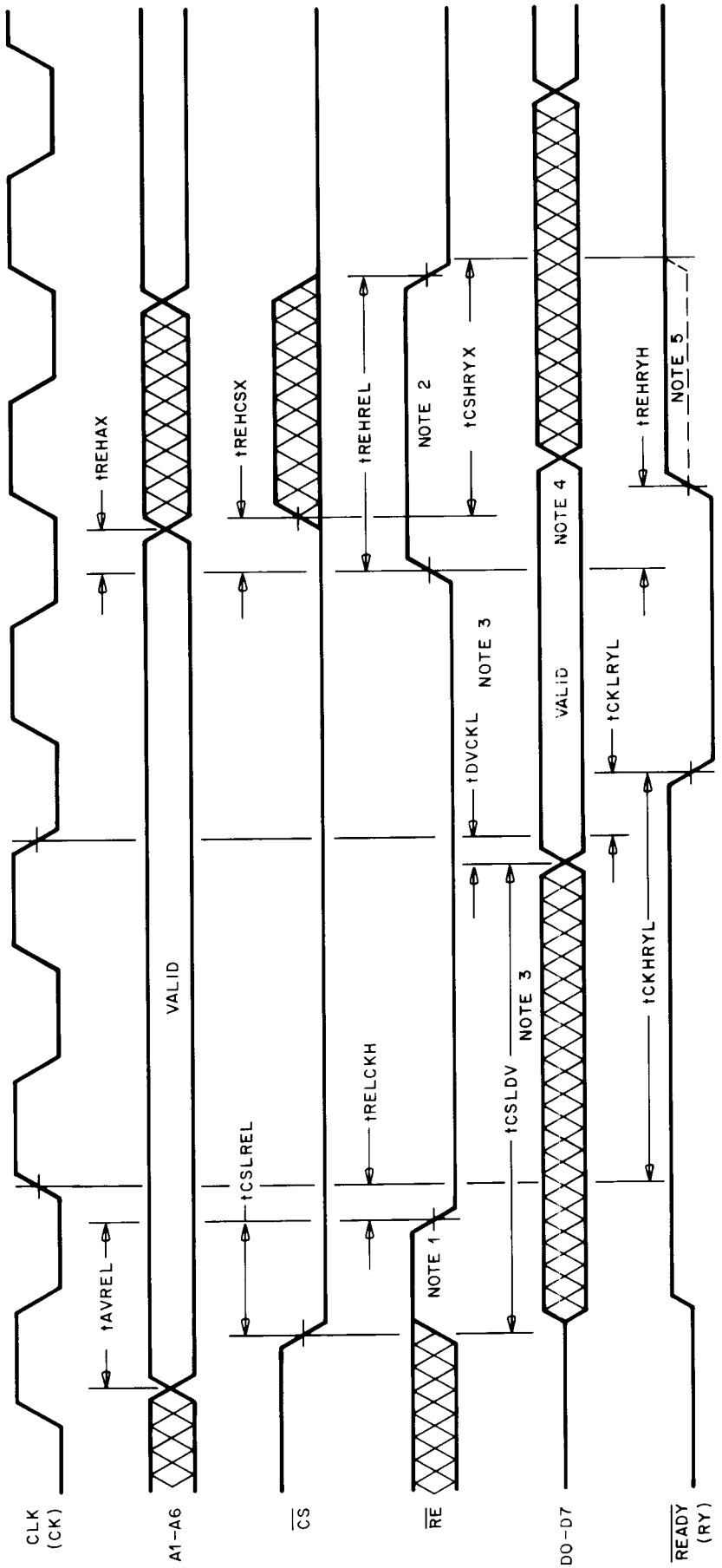
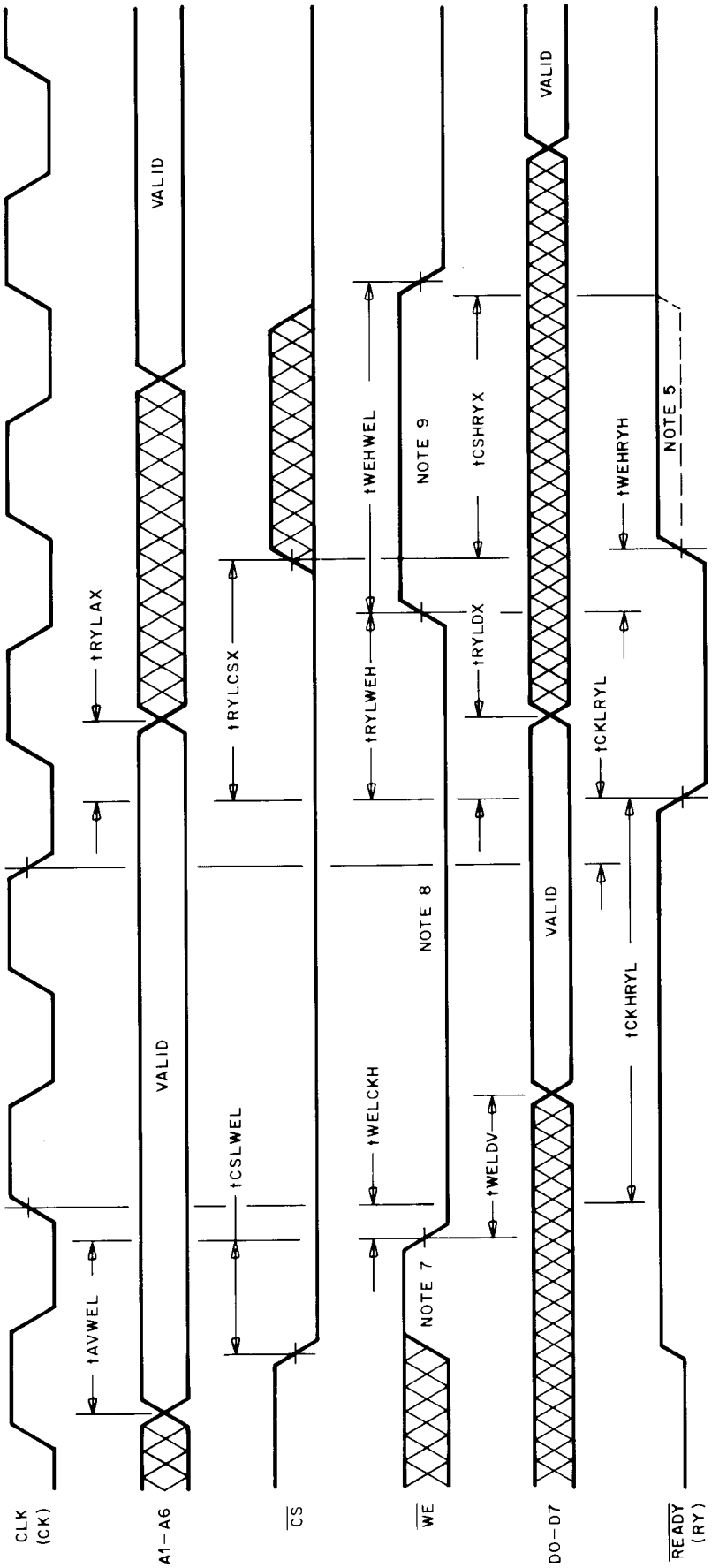



**Figure 13. Reading XPC Registers**

Note: Refer to page following Figure 22 for timing diagram notes.




Note: Refer to page following Figure 22 for timing diagram notes.

**Figure 14. Writing XPC Registers**

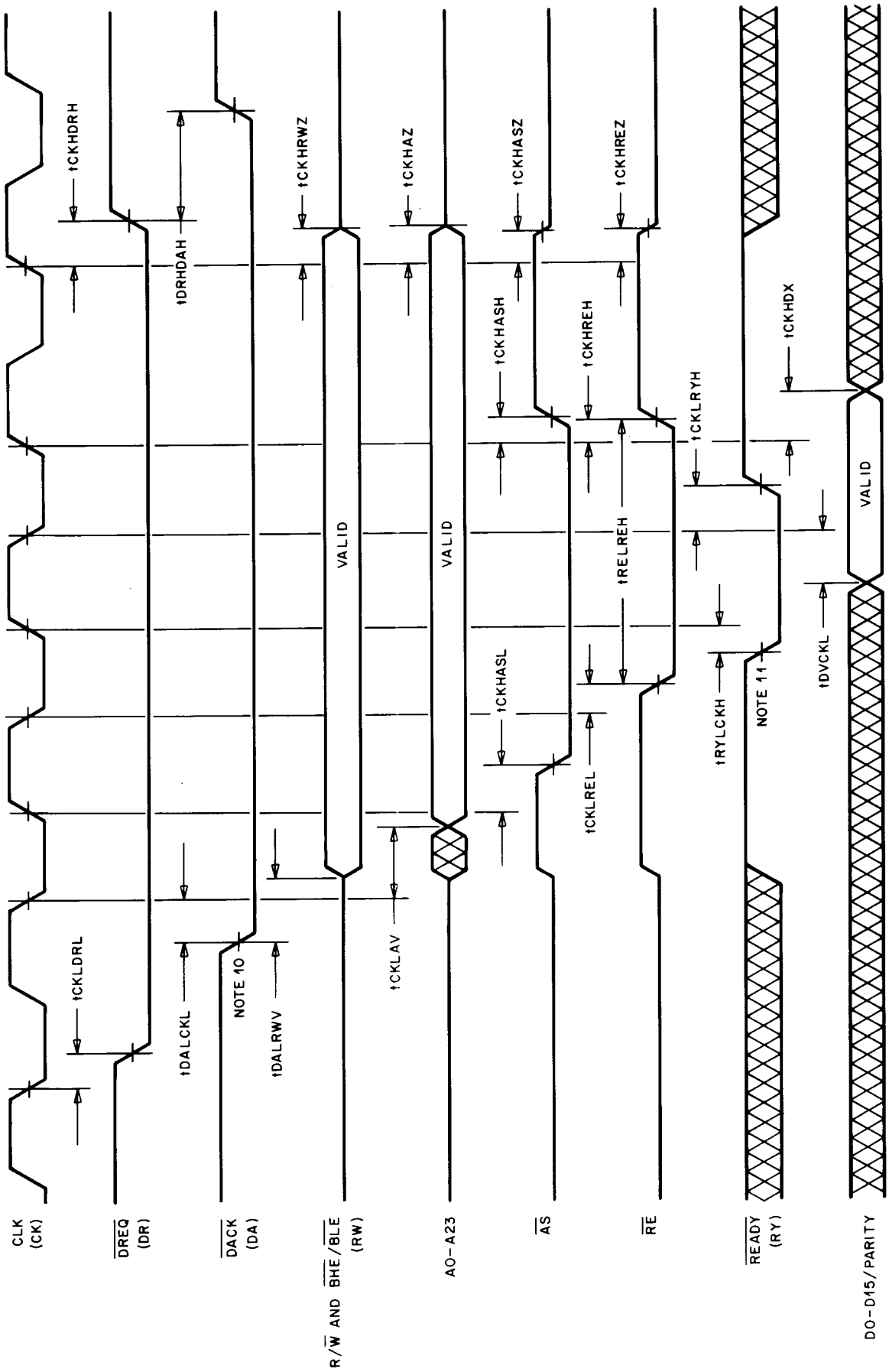
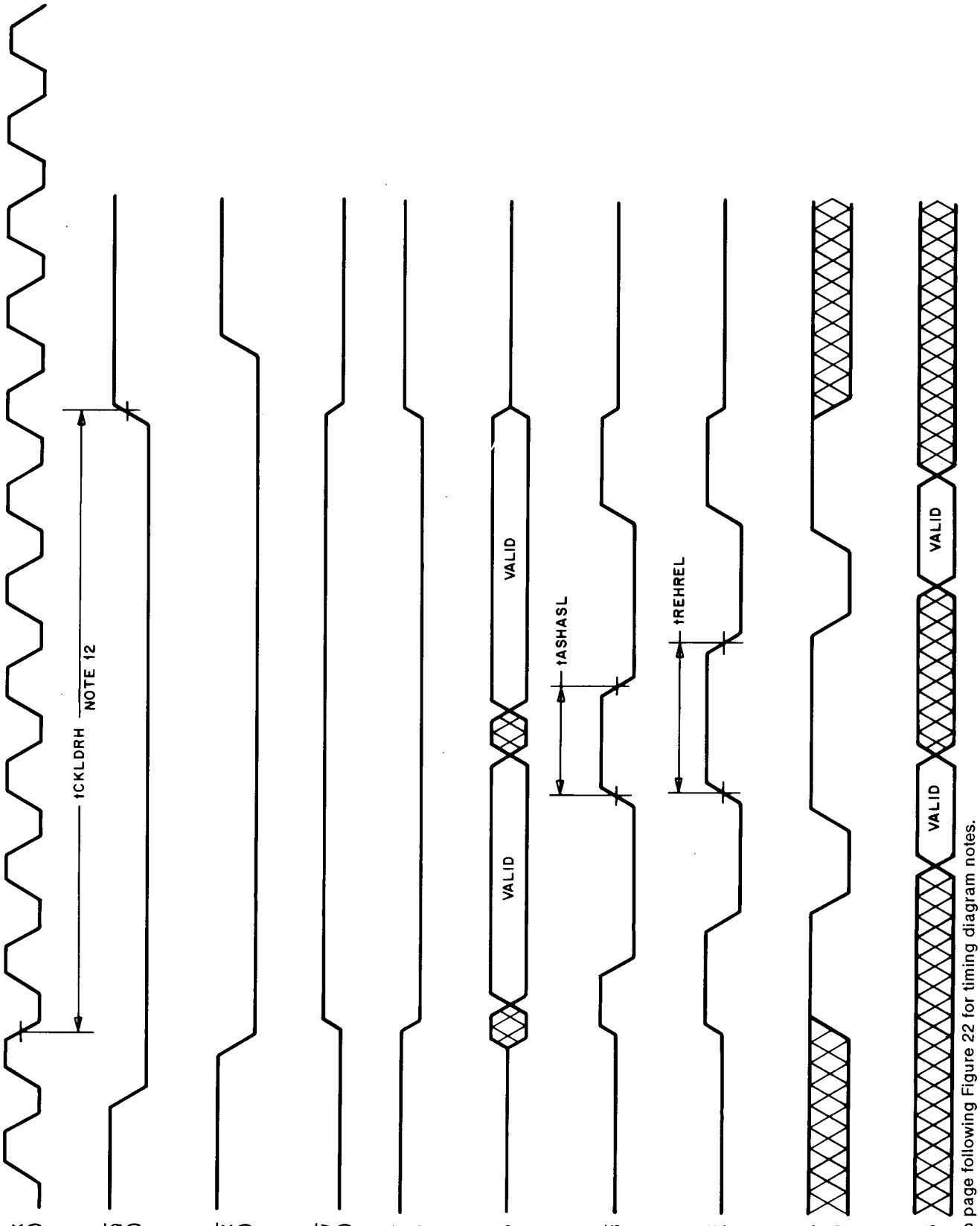



**Figure 15. DMA Read Cycle**

Note: Refer to page following Figure 22 for timing diagram notes.




Note: Refer to page following Figure 22 for timing diagram notes.

**Figure 16. DMA Multiple Byte Read Operation**

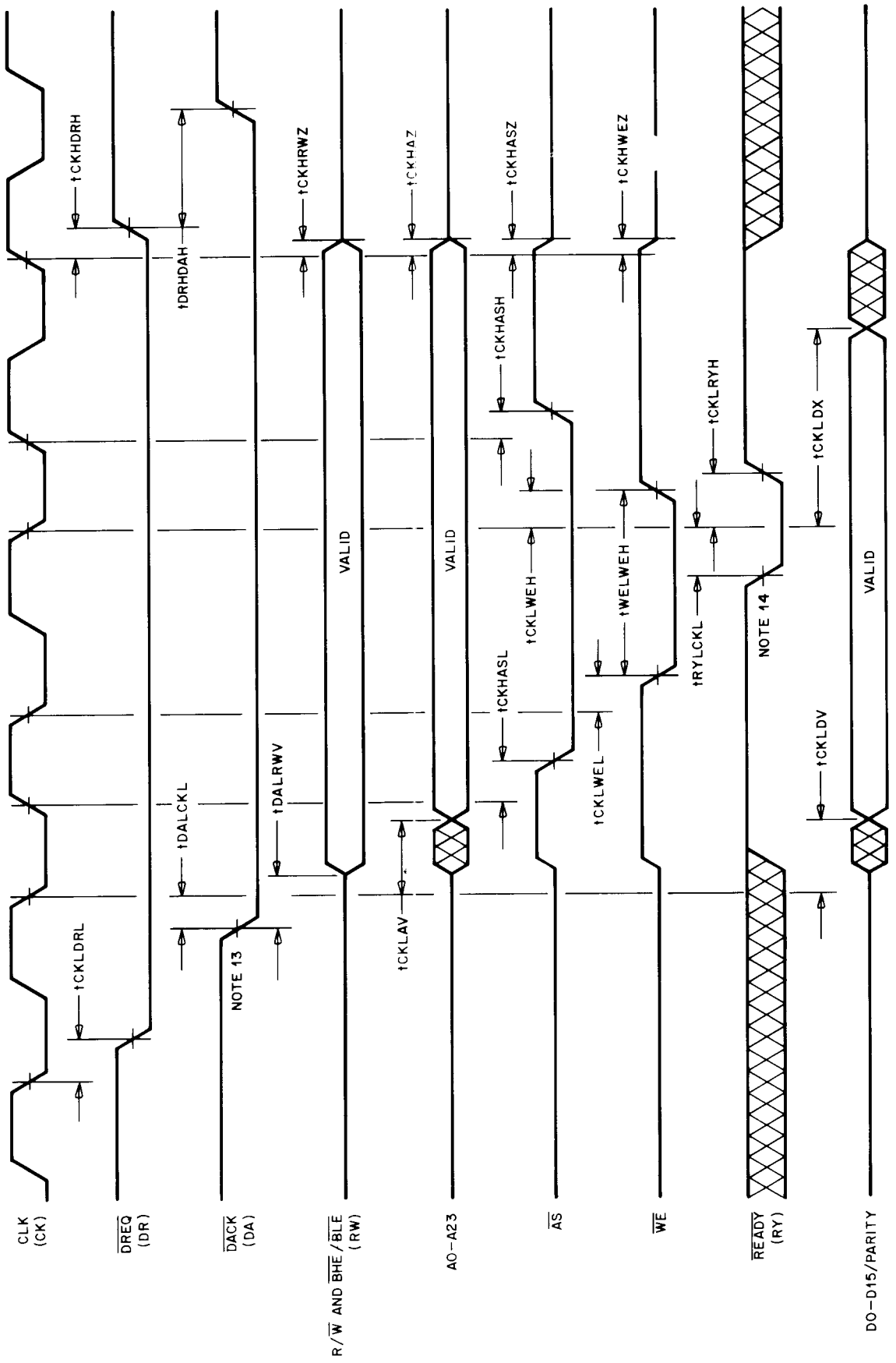
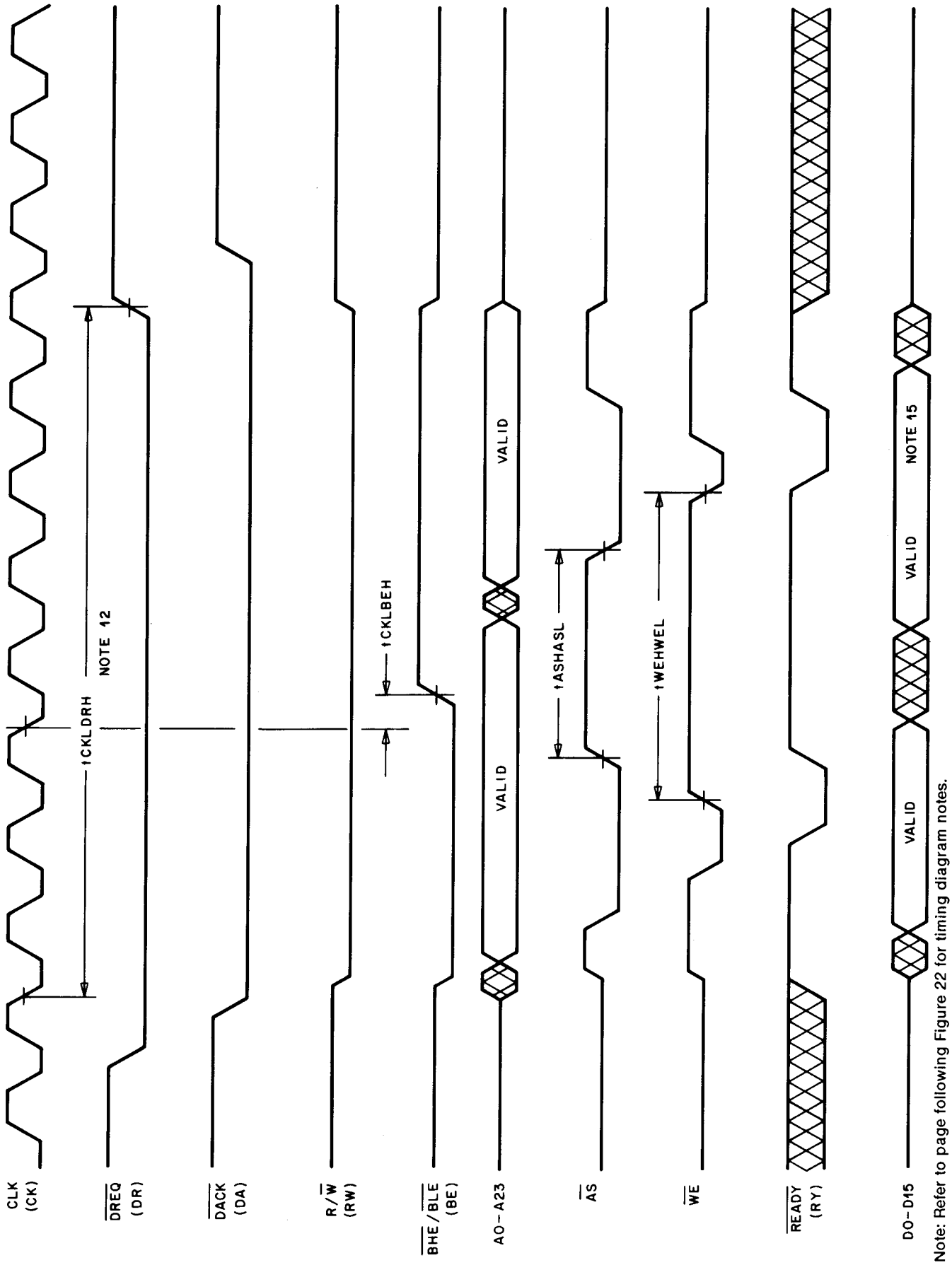


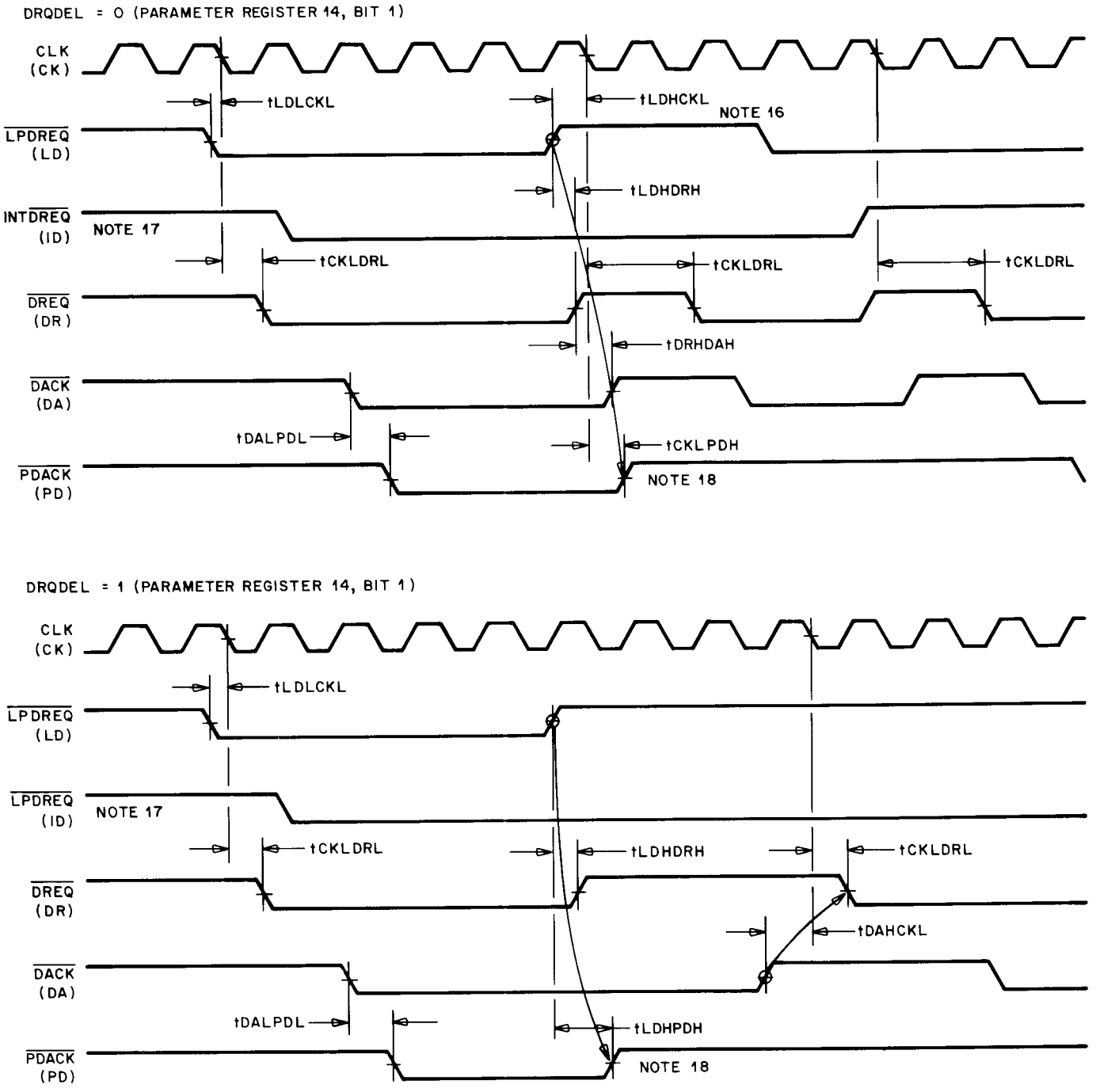

**Figure 17. DMA Write Cycle**

Note: Refer to page following Figure 22 for timing diagram notes.




Note: Refer to page following Figure 22 for timing diagram notes.

**Figure 18. DMA Multiple Byte Write Operation**




Note: Refer to page following Figure 22 for timing diagram notes.

**Figure 19. DMA Daisy Chain Timing Between Any 2 XPC Devices**

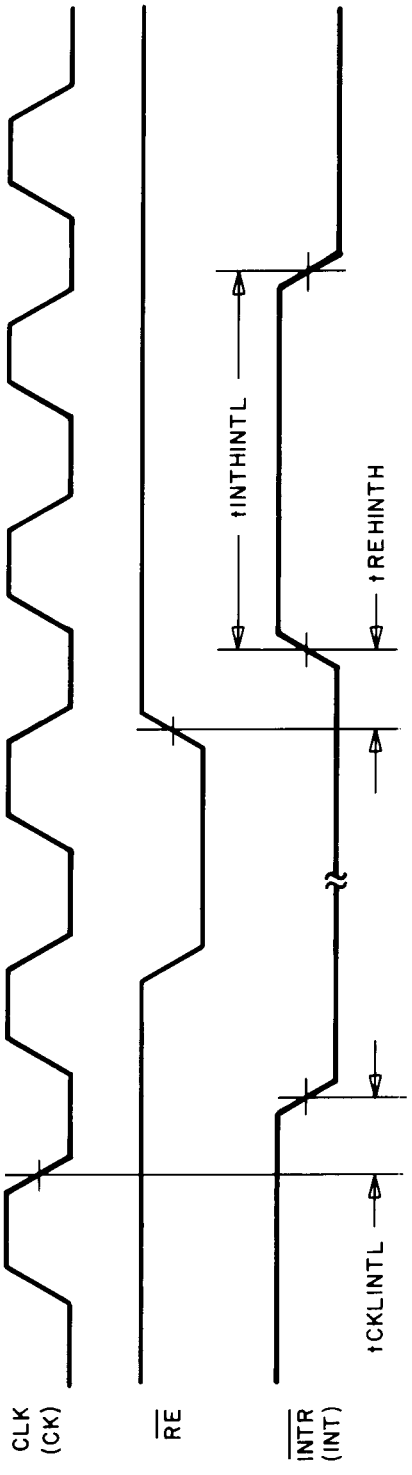



Figure 20. Interrupt Timing

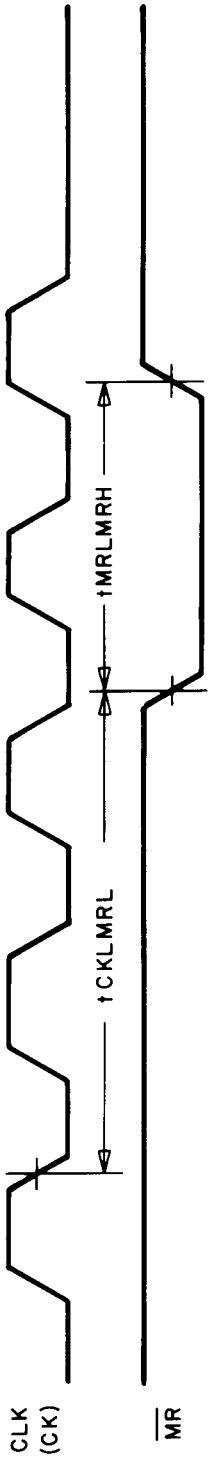
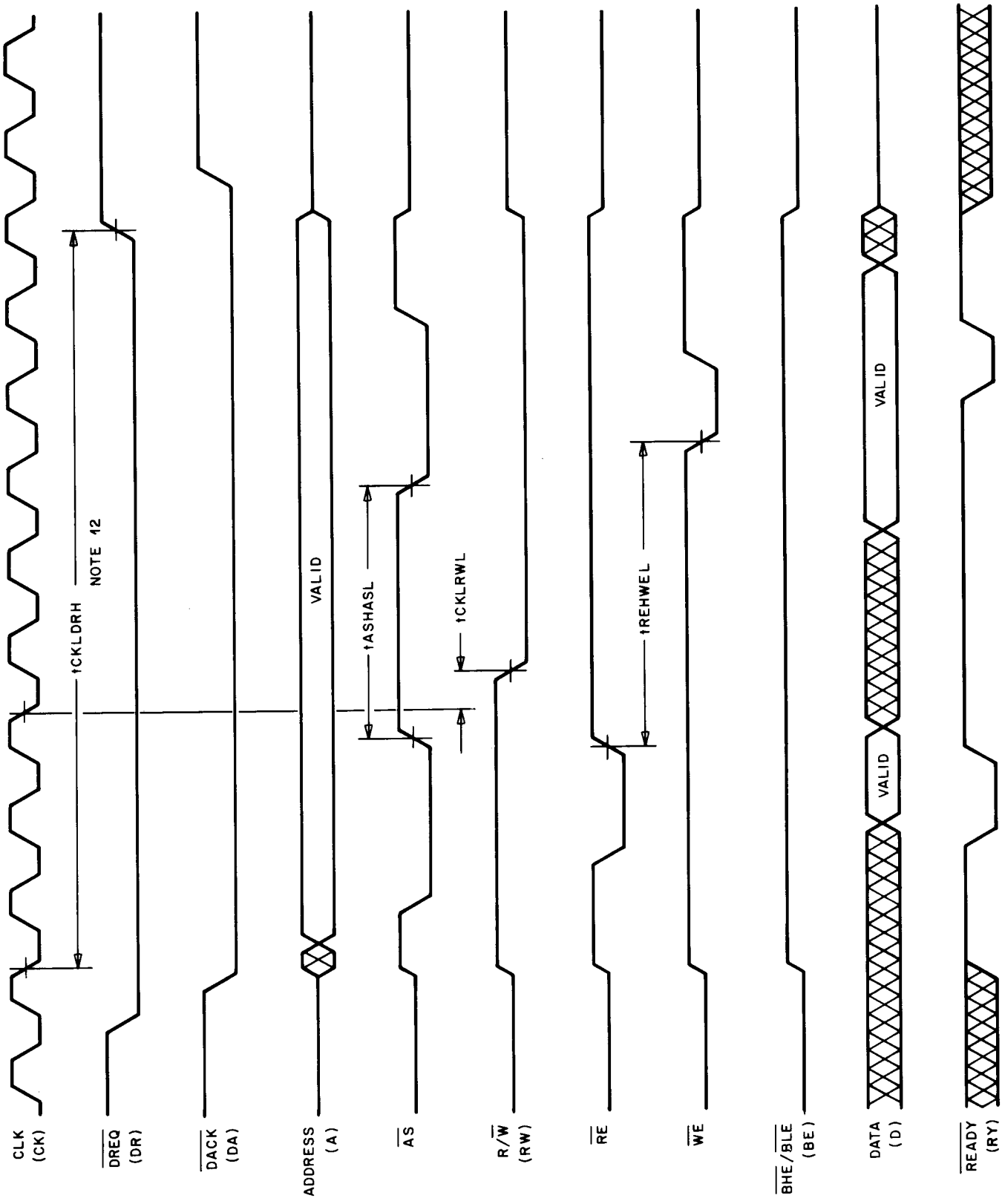



Figure 21. Reset Timing




Note: Refer to page following Figure 22 for timing diagram notes.

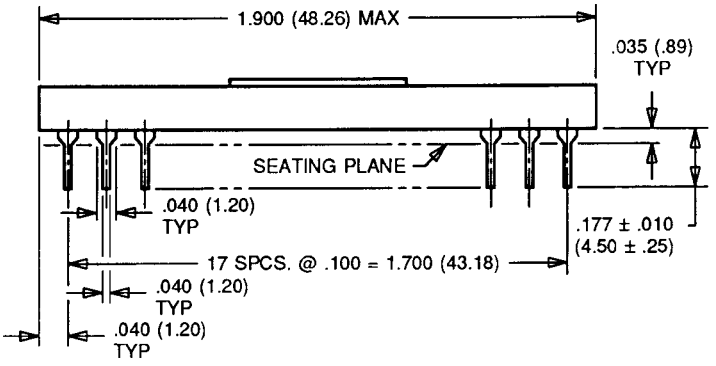
**Figure 22. Transmit Element Acknowledgment (Read-Modify-Write)**

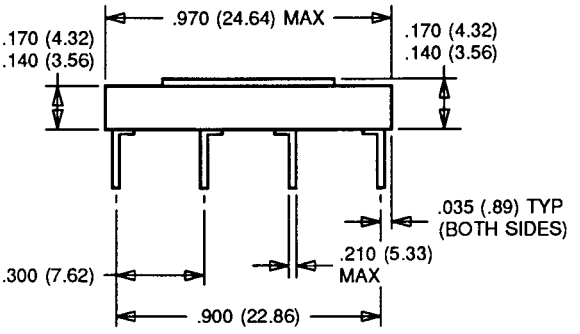
## Timing Diagram Notes

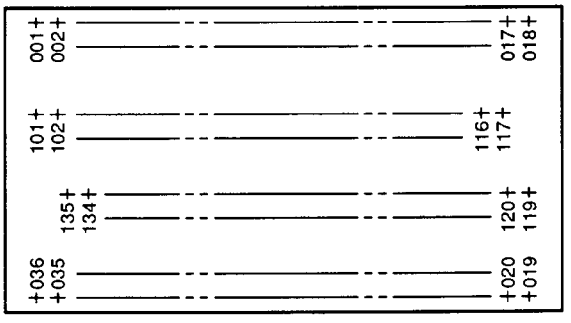
1. $\overline{RE}$ is sampled on the rising edge of CLK. Ready wait propagation does not begin until $\overline{RE}$ is sampled low.
2. tREHREL is also the minimum time before a write can occur.
3. When reading nonevent counter registers, tCSLDV should be used. tDVCKL is the time before the clock edge on which $\overline{READY}$ goes low that the event counter data is valid. tDVCKL should be used only when reading event counter registers.
4. Data remains on the data bus until $\overline{RE}$ goes high or the address changes. Data can change while $\overline{READY}$ is low and should be latched externally with the $\overline{READY}$ signal.
5. If $\overline{CS}$ is high, the XPC does not drive the $\overline{READY}$ pin.
6. $\overline{CS}$ can go high or remain low during an interoperation period.
7. $\overline{WE}$ is sampled on the rising edge of CLK. Ready-wait propagation does not begin until $\overline{WE}$ is sampled low.
8. The register is written some time within $\overline{WE}$ low window.
9. tWEHWEL is also the minimum time before a read can occur.
10. $\overline{DACK}$ is sampled on the falling edge of CLK. The read cycle does not begin until $\overline{DACK}$ is sampled low.
11. $\overline{READY}$ is sampled on the rising edge of CLK. The DMA enters a wait state until $\overline{READY}$ is sampled low.
12. tCKLDRH begins on the first falling edge of CLK after $\overline{DACK}$ is sampled low.
13. $\overline{DACK}$ is sampled on the falling edge of CLK. The write cycle does not begin until $\overline{DACK}$ is sampled low.
14. $\overline{READY}$ is sampled on the falling edge of CLK. The DMA enters a wait state until $\overline{READY}$ is sampled low.
15. D8—D15 (Intel mode: BYTORD = 0) or D0—D7 (Motorola mode: BYTORD = 1) is not valid if $\overline{BHE}/\overline{BLE}$ is high.
16. $\overline{LPDREQ}$ is sampled on the falling edge of CLK. tCKLDRL is measured from the edge on which $\overline{LPDREQ}$ is sampled high.
17. $\overline{INTDREQ}$ is the XPC internal DMA request. It is shown to illustrate the timing between two XPC devices.
18. The removal of $\overline{PDACK}$ is a function of $\overline{LPDREQ}$. $\overline{DACK}$ does not propagate from the CPU to remove $\overline{PDACK}$.

## Outline Diagram

Dimensions are in inches and (millimeters).




BOTTOM VIEW

## Ordering Information

| | | |
|---|---|---|
| T7102A-RC | 70-pin hermetic ceramic PGA package | 0 to 70 °C |

## Notes

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