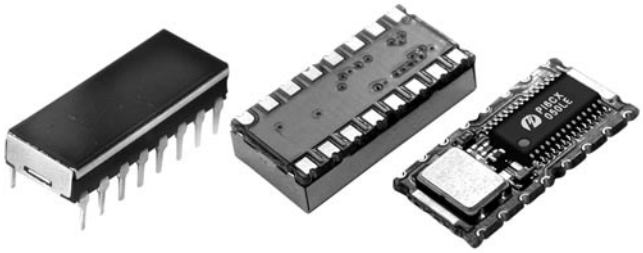
SCR050 Product Brief

3.3V and 5V TTL, Low Jitter PLL Module with Internal VCXO



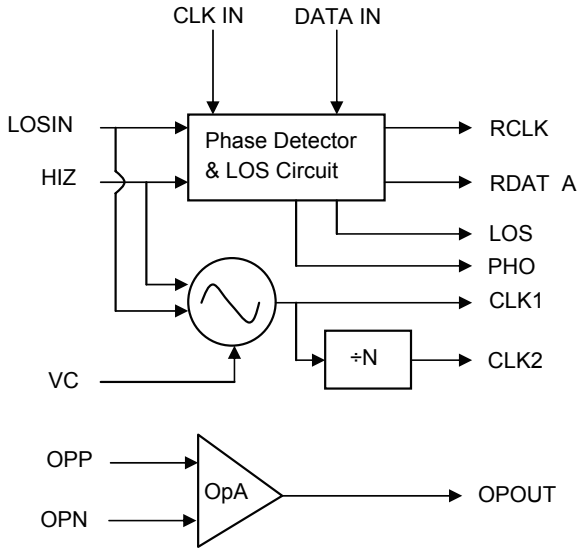
Features

- Integrated PLL with quartz-stabilized VCXO
- User-defined PLL loop response
- Input data rates from 8 kbps to 65 kbps, TTL compatible
- Two-frequency output with Tri-state control
- Recovered clock & data outputs, TTL compatible
- NRZ data compatible
- Loss of Signal (LOS) status alarm with automatic free-run switching
- Input control for forced free-run operating mode
- Rugged, shielded FR4 package available in thru-hole and true SMD

Applications

- CDR for T1/E1 and T3/E3 equipment
- CDR for video distribution systems
- CDR for telemetric/satellite systems
- Frequency translation (step-up) of a reference signal for synchronous applications
- Jitter filtering of a distributed or recovered clock signal

Functional Block Diagram



Description

The SCR050 series offers a versatile PLL solution with an embedded high-performance VCXO for use in networking and telecommunications applications. The SCR050 module performs clock recovery and data retiming (CDR), jitter filtering of an input clock signal, or frequency translation to meet the specific requirements of a given application.

The SCR050 device combines flexible IC functionality from Pericom® with high-performance fundamental-mode quartz VCXO technology from SaRonix™ into a single, modular solution for ultra-low output jitter and fast acquisition of the data/clock inputs. The TTL-compatible device features a user-configurable loop filter to fine-tune the PLL response for the particular application, output disable controls, and a Loss of Signal (LOS) alarm.

Owing to unique invention, the SCR050 is an RFI-shielded modular design set on an FR4 base, available with true SMD pads or a molded leadframe, and featuring a body thickness less than 3.5mm. The SCR050 solution is mechanically interchangeable and socket-compatible with similar devices available on the market.

Performance Features

Parameter	Specification
Input data rate (NRZ)	8 kbps to 65.536 Mbps
Input data rate (RZ)	8 kbps to 32.768 Mbps
Operating Frequency (CLK1)	12 to 65.536 MHz (as specified)
Operating Frequency (CLK2)	0.05 to 32.768 MHz (as specified)
Free-Run Accuracy *Aging:	+/-20 ppM through +/-100 ppM max (as specified) over all conditions including operating temperature, calibration tolerance, rated input (supply) voltage, load changes, aging*, shock and vibration 10 years @ 40°C average ambient operating temperature
Operating Range	0 to +70°C or –40 to +85°C (as specified)
Track and hold range	+/-20 ppM through +/-100 ppM min (as specified)
Input Lock Acquisition Time	15ms typ
Supply Voltage	3.3V or 5V (7V absolute max) (as specified)
Output Logic	TTL compatible, 5 TTL load
Rise/Fall Time	5ns max (measured between 0.5 and 2.5V)
Jitter attenuation	> 50dB (RDATA, RCLK)
Jitter generation	< 0.001 UI (when locked to input)
Phase (computed) jitter	0.7ps RMS (1-sigma) max, 12kHz to 40MHz frequency band (free run mode)

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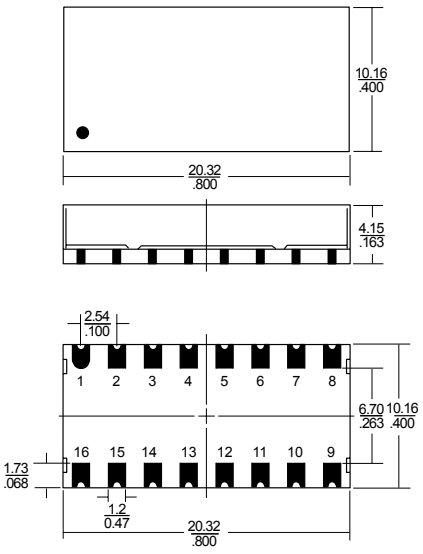
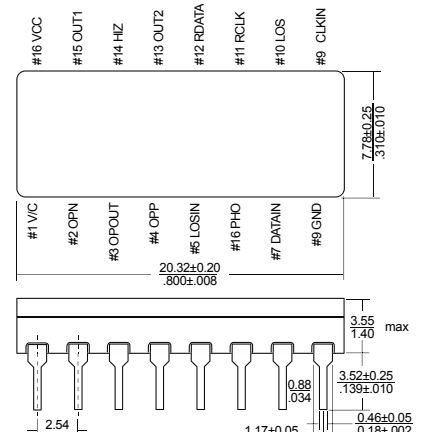
Package Diagrams



S Package w/ Surface Mount



T Package with Thru Hole DIP

Pin Description

Pin Name	Description
VC	Control voltage for internal low-jitter VCXO
OPN	Negative input terminal to internal operational amplifier
OPOUT	Output terminal of internal operational amplifier
OPP	Positive input terminal to internal operational amplifier
LOSIN	TTL input. Logic 1 disables VC and internal VCXO reverts to nominal frequency (free-run, stability as specified). Logic 0 or NC enables VC and internal VCXO for acquisition. LOSIN is pulled-down internally.
PHO	Output signal of phase detector
DATAIN	TTL input. Input data stream to phase detector (NRZ compatible)
GND	Circuit and case ground
CLKIN	TTL input. Input clock signal to phase detector
LOS	TTL output. Logic 1 upon 256 consecutive transition-free DATAIN bits. Logic 0 upon first transition
RCLK	TTL output. Recovered clock, jitter-attenuated
RDATA	TTL output. Recovered data stream, retimed with RCLK
CLK2	TTL output. A binary quotient of CLK1 (as specified)
HIZ	TTL input. Logic 0 disables all clock and data outputs to Hi-Z. Logic 1 or NC activates all outputs
CLK1	TTL output. Output clock of internal low-jitter VCXO (as specified)
VDD	Supply voltage (as specified)

Part Numbering Guide

SCR050 S A A A A - 032.7680/016.3840(T)

SaRonix Clock Recovery Model

Package Type
S: Surface Mount
T: Thru Hole DIP

CLK2 Divide
A: /2 F: /64
B: /4 G: /128
C: /8 H: /256
D: /16 K: disabled
E: /32

Temp. Range & Free Run Accuracy
AA: ±20ppM, 0~70ºC
A: ±25ppM, 0~70ºC
B: ±50ppM, 0~70ºC
C: ±100ppM, 0~70ºC (std)
E: ±50ppM,-40º~85ºC
H: ±32ppM, -40º~85ºC
T: ±100ppM, -40º~85ºC (std)

Absolute Pull Range:
C: ±20ppM
F: ±32ppM
G: ±50ppM
H: ±100ppM

CLK2 Freq (MHz)
CLK1 Freq MHz)

Supply Voltage
A: 5.0V
3: 3.3V

Packaging
(T) = Tape & Reel
SMD only
Blank = Bulk

About SaRonix

SaRonix, Inc is a wholly owned subsidiary of Pericom Semiconductor Corporation. Since 1975, SaRonix has specialized in high-performance frequency control products. Today, Pericom and SaRonix combine advanced quartz oscillator technologies with flexible silicon IC solutions and other discrete devices to deliver a range of integrated modular timing solutions for telecommunications, datacom, storage fabric, and wireless applications.