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MICRONAS

August 1990

MAS 7541A
12-BIT DAC

APPLICATIONS

- Instrumentation
- Digital Synchro Conversion
- Programmable Amplifiers

FEATURES

- +/- 1/2 LSB DNL and INL
- No Laser Trimming
- Linearity TC 1.0 pmm/C Max
- 2 kV ESD Protection on Digital Inputs
- TTL/CMOS Compatible
- 3 MSB's Decoded
- Low Sensitivity to Amplifier Offset
- All 4096 Codes Tested
- AD/7541/7541A Replacement
- Available in Die Form
- Low Cost

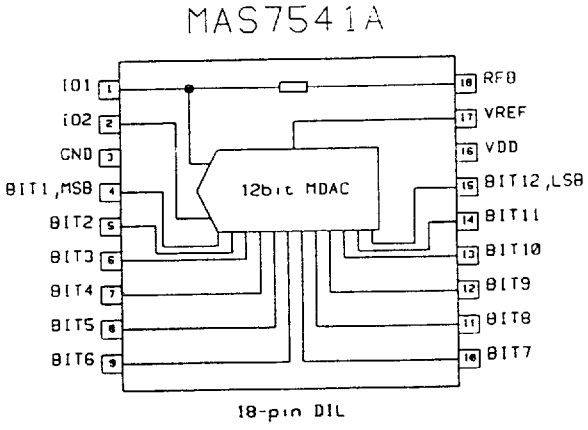
GENERAL DESCRIPTION

The MAS7541A is a low cost, monolithic CMOS, 12-bit multiplying digital to analog converter (DAC). Its high performance is achieved without laser trimming. This is made possible by the use of highly accurate and stable, low TCR thin film resistor process developed at Micronas and a 3 MSB to 7 decoding design technique. Hidden errors are eliminated by testing all the 4096 different input codes.

The device offers advantages like high stability over time and temperature and low sensitivity to output amplifier offset combined to excellent performance-to-cost ratio. All digital inputs have high ESD protection over 2 kV.

The device is offered in a 18 pin Plastic DIP and Cerdip packages as well as in die form.

BLOCK DIAGRAM



ORDERING INFORMATION

Relative. Accuracy	Gain Error	Temperature range and package	
Tmin-Tmax	Ta = +25°C	Commercial 0°C to +70°C	Industrial -25°C to +85°C
		Plastic DIP	Cerdip
±1 LSB	±6 LSB	MAS7541A-1CN	MAS7541A-1IO
±1/2LSB	±3 LSB	MAS7541A-0CN	MAS7541A-0IO

NOTE: In lieu of cerdip package Micronas reserves the right to ship side braze packaged parts.

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Electrical characteristics

VDD = +15V, VREF = 10V, I01 = I02 = GND = 0V, Unipolar unless otherwise specified

Parameter	Symbol	Version	MIN	Ta=+25°C TYP	MAX	Tmin-Tmax Limits	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution	N	All	12			12	Bits	
Integral Nonlinearity[1]	INL	7541A-1			±1	±1	LSB	Relative accuracy 11 bits
		7541A-0			±1/2	±1/2	LSB	Relative accuracy 12 bits
Differential Nonlinearity[2]	DNL	7541A-1			±1	±1	LSB	Monotonic to 12 bits
		7541A-0			±1/2	±1/2	LSB	Monotonic to 12 bits
Gain Error	Gfse	7541A-1			±6	±8	LSB	Measured using internal Rfb
		7541A-0			±3	±5	LSB	DAC register loaded with all 1s
Output Leakage Current at I01 (pin1)	Ilkg	C			±5	±10	nA	All digital inputs = 0V
		I			±5	±10	nA	
TEMPERATURE[3] STABILITY								
Gain Error TC	TCGfse	All		±1.0			ppm/°C	
Integral Nonlinearity TC	TCINL	All		±0.1			ppm/°C	
Differential Nonlinearity TC	TCDNL	All		±0.1			ppm/°C	
REFERENCE INPUT								
Input Resistance	Rref	All	7	10	15		kΩ	Input Resistance TC ±150ppm/°C
Voltage Range[3]		All				±25	V	
DIGITAL INPUTS								Unipolar Coding: Binary
Input High Voltage	VIH	All	2.4		VDD	2.4	V	Bipolar Coding: Offset Binary
Input Low Voltage	VIL	All	-0.3		0.8	0.8	V	
Input Current[4]	Iin	All			±1	±10	µA	
Input Capacitance[3]	Cin	All			8	8	pF	
POWER SUPPLY								
Voltage Range	VDD	All	+5	+15	+16		V	Accuracy guaranteed only at +15V
Supply Current	IDD	All		2.0	2.5	2.5	mA	All Digital Inputs VIL or VIH
	IDD	All		0.2	0.5	1.0	mA	All Digital Inputs 0V or 5V to VDD
TEMPERATURE RANGE		C	0		+70		°C	
		I	-25		+85		°C	

NOTES:
1. Integral Nonlinearity is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any given input combination.
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3. Guaranteed by design but not production tested.
4. Logic inputs are MOS gates. Iin typical is less than 1 nA at 25°C.

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AC performance characteristics

These characteristics are included for design guidance only and are subject to sample testing only.
VDD = +15V, VREF = 10V, IO1 = IO2 = AGND = 0V except where stated. Output Amp is HOS-050.

Parameter	Symbol	Version	Ta = +25°C MIN	TYP	MAX	Tmin-Tmax Limits	Units	Test Conditions/Comments
PROPAGATION DELAY	tPD	All		100			ns	I01 load R = 100Ω, Cext = 13pF All data inputs 0V to VDD or VDD to 0V From 50% digital input change to 90% of final analog output.
CURRENT SETTLING TIME Full Scale Transition	ts	All		0.6			us	Settling to ±0.01% FSR (strobet). All data inputs 0V to VDD or VDD to 0V
OUTPUT CAPACITANCE CIO1 (pin 16) CIO2 (pin 15) CIO1 (pin 16) CIO2 (pin 15)	Co	All			 200 70 70 200	 200 70 70 200	 PF pF pF pF	 Digital inputs VIH Digital inputs VIH Digital inputs VIL Digital inputs VIL
DIGITAL TO ANALOG GLITCH ENERGY	Q	All		1000			nVs	VREF = 0V, DAC Register alternatively loaded with all 0's and 1's
MULTIPLYING FEED THROUGH ERROR AT I01	FT	All		1.0 0.1			mVpp mVpp	VREF = 20Vpp, f = 10kHz sine wave VREF = 20Vpp, f = 1kHz sine wave
POWER SUPPLY REJECTION Ratio	PSRR	All			±0.02		%/%	VDD = 14-16V

ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

VDD to GND	-0.3, +17V
Digital Input Voltage to GND	-0.3V, VDD +0.3V
VREF or VRFB to GND	+/-25V
Output Voltage (PIN 1, PIN 2)	-0.3V, VDD +0.3V
Power Dissipation (Any Package) to +75°C	450 mW
Derates above 75°C by	6 mW/°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C

CAUTION:
1. Do not apply voltages higher than VDD or less than GND potential on any terminal other than VREF or RFB.
2. The digital inputs are diode clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all time until ready to use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. this is a stress rating only and functional oderation at or above this specification in not implied.

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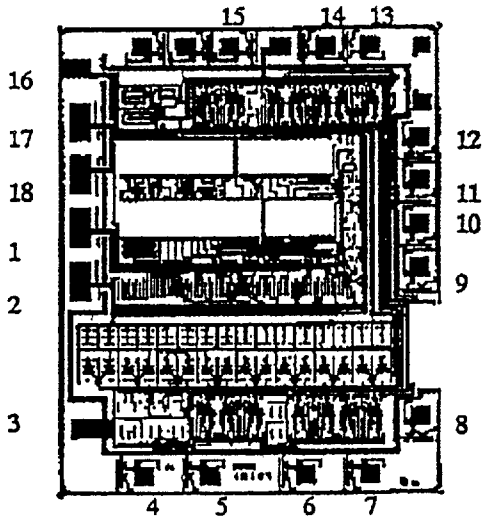
Dice characteristics



1. IO1
2. IO2
3. GND
4. BIT 1 (MSB)
5. BIT 2
6. BIT 3
7. BIT 4
8. BIT 5
9. BIT 6
10. BIT 7
11. BIT 8
12. BIT 9
13. BIT 10
14. BIT 11
15. BIT 12 (LSB)
16. VDD
17. VREF
18. RFB

DIE SIZE 87 X 109 mils, 9.500 sq. mils (2.21 x 2.77 mm, 6.12 sq. mm)

Wafer test limits

TA = +25°C, VDD = +15V, VREF = -10V, IO1 = IO2 = GND = 0V

Parameter	Symbol	Limits	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Integral Nonlinearity	INL	±1	LSB	Note 1. Relative Accuracy 11 bits
Differential Nonlinearity	DNL	±1	LSB	Note 2. Monotonicity 12 bits
Gain Error	Gfse	±6	LSB	Measured using internal Rfb DAC register loaded with all 1s
Output Leakage Current at IO1 (pin 1)	Ilkg	±10	nA	
REFERENCE INPUT				
Input Resistance	Rref	7/15	kΩ	Pad 17, 10 kΩ nominal
DIGITAL INPUTS				
Input High Voltage	VIH	2.4	V	
Input Low Voltage	VIL	0.8	V	
Input Current	Iin	±1	μA	VIN = 0V or VDD
POWER SUPPLY				
Supply Current	IDD	2.5	mA	All Digital Inputs VIL or VIH
	IDD	0.5	mA	All Digiatal Inputs 0V or 5V to VDD

NOTES
1. End-point linearity
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.

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MAS 7541A 12-BIT MONOLITHIC CMOS MDAC

Application Information

Unipolar Operation

The connections required for digital unipolar operation are shown in Figure 1. The reference voltage V_{REF} may be either positive or negative. The 2kΩ potentiometer in the V_{REF} line and the 1kΩ resitor in the feedback loop are optional and are only needed when the gain error must be trimmed to less than 0.3% F.S.R. They should track each other to better than 0.1%, but dont have to track 7541A's internal network resistors.

As shown in Figure 4 the DAC current output is typically connected to an external OP-AMP with it's non-inverting input tied to ground. The amplifier selected should have a low input bias current and low drift over temperature. To maintain specified MAS 7541A linearity, the amplifiers input offset voltage should be nulled to less than ±200μV (0.1LSB). Table 1 shows the code table for unipolar operation.

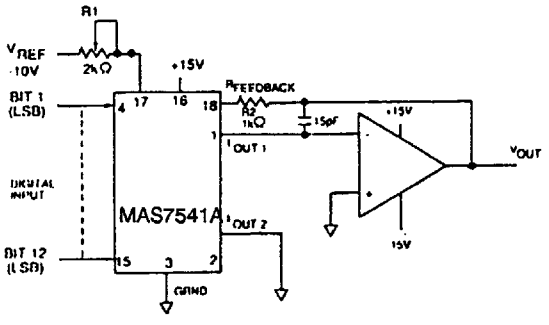

FIGURE 1: Unipolar Operation

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99975 V_{REF}
100000000000	-0.50000 V_{REF}
011111111111	-0.49975 V_{REF}
000000000000	0

TABLE 1: Unipolar Operation Code Table

Bipolar Operation

The connections required for bipolar operation are shown in Figure 2. The digital input is offset binary coded and produces an output according to the code table shown in Table 2.

As in the case of unipolar operation the gain trim resistors can be omitted in applications that do not require minimum gain error. Amplifier considerations of low input bias current, low drift and offset nulling are also applicable for bipolar operation.

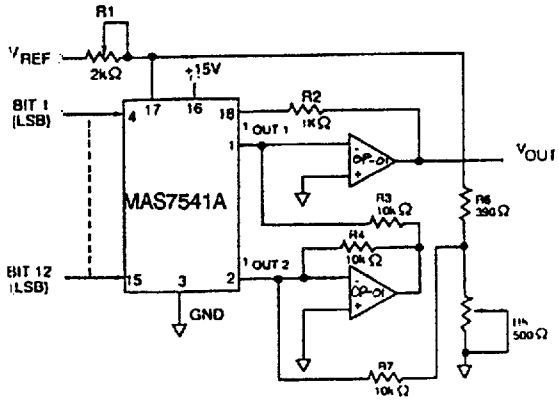

FIGURE 2: Bipolar Operation

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99951 V_{REF}
100000000001	-0.00049 V_{REF}
100000000000	0
010000000000	+0.50000 V_{REF}
000000000000	+1.00000 V_{REF}

TABLE 2: Bipolar Operation Code Table