

54AC/74AC157 • 54ACT/74ACT157

Quad 2-Input Multiplexer

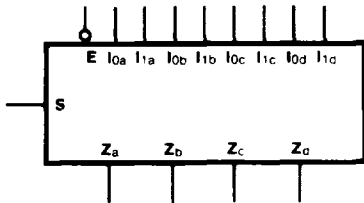
Description

The 'AC/ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'AC/ACT157 can also be used as a function generator.

- Outputs Source/Sink 24 mA
- 'ACT157 has TTL-Compatible Inputs

Ordering Code: See Section 6

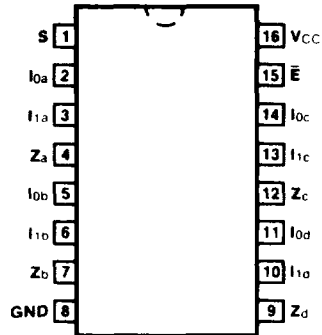
Logic Symbol



Pin Names

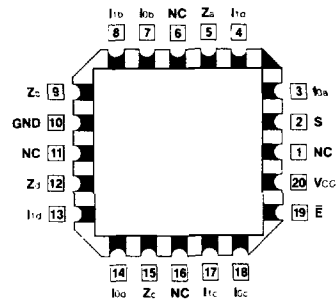
- | | |
|-----------------------------------|----------------------|
| I _{0a} - I _{0d} | Source 0 Data Inputs |
| I _{1a} - I _{1d} | Source 1 Data Inputs |
| E | Enable Input |
| S | Select Input |
| Z _a -Z _d | Outputs |

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

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Pin Assignment for LCC

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Functional Description

The 'AC/ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'AC/ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the 'AC/ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/ACT157 can

generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

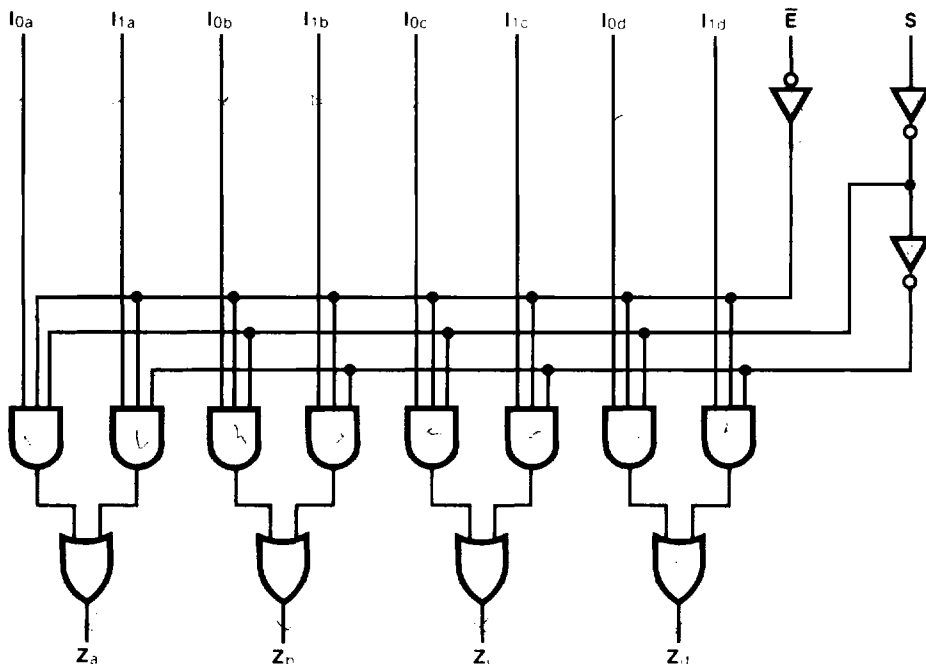
Inputs				Outputs
\bar{E}	S	I ₀	I ₁	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input (ACT157)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

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Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay S to Z _n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	14.5 11.0	1.0 1.0	13.0 10.0	ns	3-6
t _{PHL}	Propagation Delay S to Z _n	3.3 5.0	1.0 1.0	6.5 5.0	11.0 8.5	1.0 1.0	13.5 10.5	1.0 1.0	12.0 9.5	ns	3-6
t _{PLH}	Propagation Delay E to Z _n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	14.0 10.5	1.0 1.0	13.0 10.0	ns	3-6
t _{PHL}	Propagation Delay E to Z _n	3.3 5.0	1.0 1.0	6.5 5.5	11.0 9.0	1.0 1.0	13.0 10.5	1.0 1.0	12.0 9.5	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	1.0 1.0	5.0 4.0	8.5 6.5	1.0 1.0	10.0 7.5	1.0 1.0	9.0 7.0	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	1.0 1.0	5.0 4.0	8.0 6.5	1.0 1.0	10.0 7.5	1.0 1.0	9.0 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay S to Zn	5.0	1.0	5.5	9.0	1.0	13.0	1.0	10.0	ns	3-6
tPHL	Propagation Delay S to Zn	5.0	1.0	5.5	9.5	1.0	12.5	1.0	10.5	ns	3-6
tPLH	Propagation Delay E to Zn	5.0	1.0	6.0	10.0	1.0	13.0	1.0	11.5	ns	3-6
tPHL	Propagation Delay E to Zn	5.0	1.0	5.0	8.5	1.0	12.5	1.0	9.0	ns	3-6
tPLH	Propagation Delay In to Zn	5.0	1.0	4.0	7.0	1.0	10.0	1.0	8.5	ns	3-5
tPHL	Propagation Delay In to Zn	5.0	1.0	4.5	7.5	1.0	10.0	1.0	8.5	ns	3-5

*Voltage Range 5.0 Is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance	50.0	pF	Vcc = 5.5 V