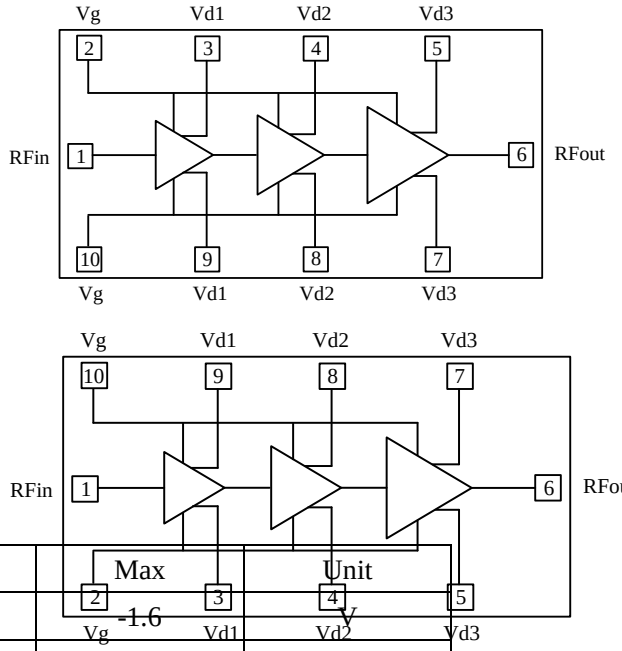
Feature

- Frequency ： 15.5GHz～17.5GHz
- Power Gain：20dB
- Psat：47dBm
- PAE：30%
- +28V@3.0A(Quiescent)
- Dimension ： 3.60mm×5.90mm×0.10mm

Function Diagram



DC Electrical Specification（T_A = +25℃）

Parameter	Min	Typical	Max	Unit
Vd	-2.2	-2.0	-1.6	V
Vg	24	28	32	V
Id	3.5	4.0	4.5	A
Idd		6.0	6.5	A
Ig		0.1	1	mA
Igg		2	10	mA

Microwave Electrical Specification（T_A = +25℃，Vd = +28V，Vg = -2.0V）

Parameter	Min	Typical	Max	Unit
f	15.5～17.5			GHz
Psat	47	47.8		dBm
Gp	19	20		dB
ΔGp			±0.5	dB
PAE	30	35		%
Gain	28	30	33	dB
ΔGain			±2.5	dB
VSWR(in)		2.0	2.5	-
Second Harmonic			-30	dBc

Note ： 1）The MMIC has been 100% DC and RF tested on chip.

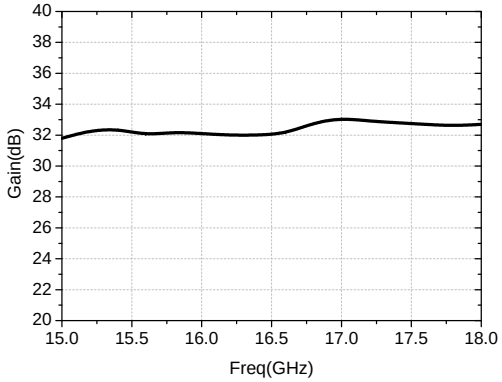
2）Testing Condition：Vd=+28V，Vg=-1.8V，P_{in}=27dBm，Pulse width 100μs，duty cycle 10%；

Max Limited Values

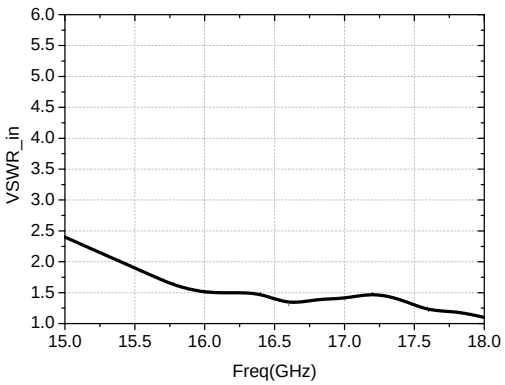
Parameter	Values
Max Vd	+36V
Max Vg	-5V
CW P_p	+32dBm
T_{STG}	-65℃～+150℃
T_{op}	+200℃
Z_0	5：1

Testing Curves（Vd=+28V，Vg=-1.8V）

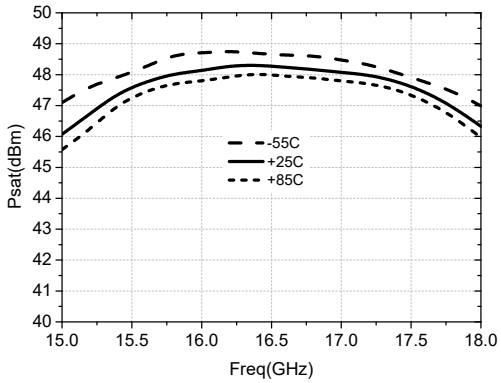
Small Signal Gain（P_{in}=-10dBm）



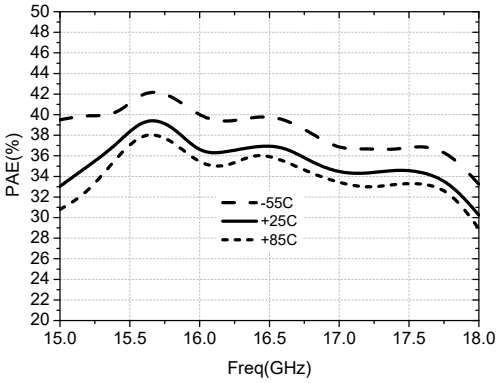
VSWRin（P_{in}=-10dBm）



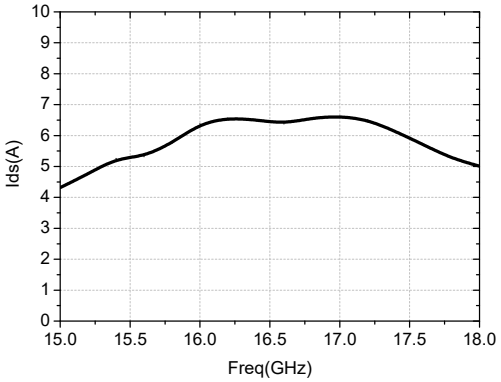
High-low temeprture Pout（P_{in}=27dBm）



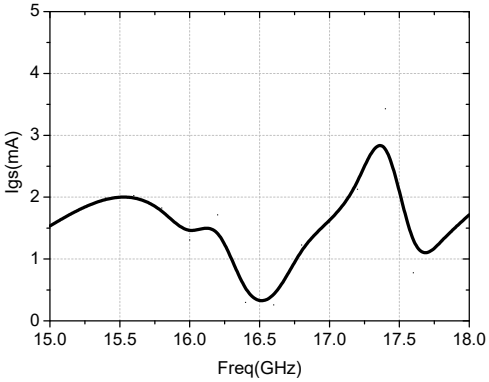
High-low temeprture PAE（,P_{in}=27dBm）



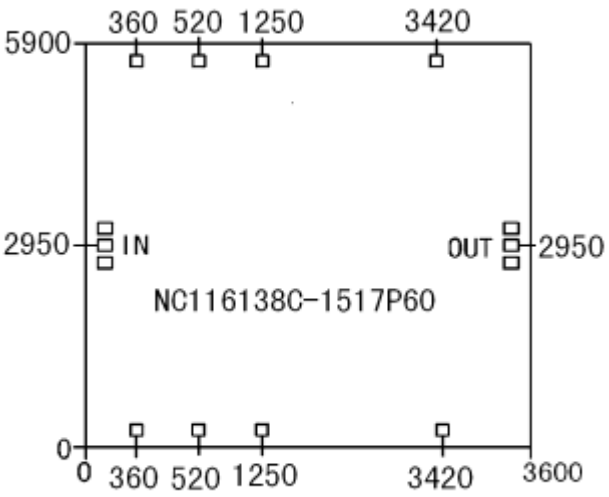
Ids



Igs

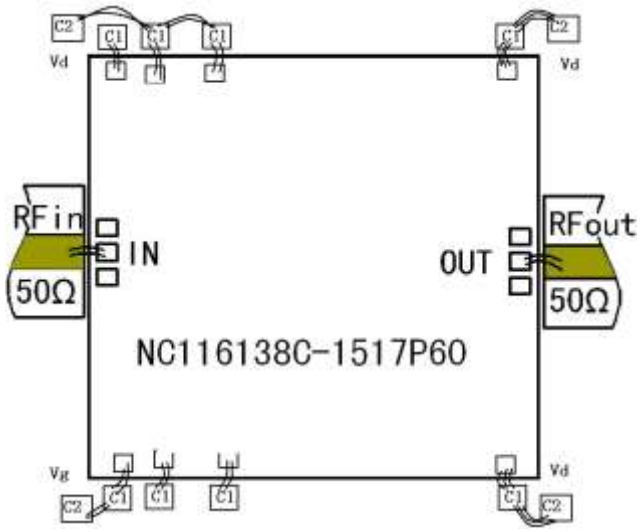


Outline and Dimension



Note ： All the unit is um；
Input and output pad dimension:100×120um^2
Bias pad dimension:100×100um^2

Assembly Diagram



note ： External capacitance c=100pF,c2=2PF；

Please add above 0.01μF capacitor filter at the gate bias, the diameter ,Bonding wire diameter is 25um.

Attention

1） The MMIC needs to be stored in a dry and clean N2 environment;
2） The chip substrate material 6H-SiC is very brittle and must be used carefully to avoid damage to the chip;
3） The thermal expansion coefficient of the carrier should be close to that of 6H-SiC, and the coefficient of thermal expansion of the wire is 4.2×10-6/℃. When using continuous wave, it is recommended that the carrier material be copper-molybdenum-copper, copper-molybdenum-copper-copper, diamond-copper, etc.
4） Please avoid holes between the chip and the carrier during assembly, and ensure good heat dissipation of the case and carrier;
5） It is recommended to use gold tin solder for sintering, Au:Sn=80%: 20%, sintering temperature not exceeding 300 ℃, time is not longer than 30 seconds, the sintering process avoids rapid temperature change, and needs to gradually rise and fall;
6） It is recommended to use a gold wire with a diameter of 25μm～30μm. The temperature of the bonding platform chassis does not exceed 250 ℃, the bonding time is as short as possible, and the bonding process avoids rapid temperature changes;
7） Pay attention to anti-static during the use and assembly of the chip, wear a grounded anti-static bracelet, and the grounding of the sintering and bonding stations is good;
8） If you have any questions, please contact the supplier.