

512MB (2 x 64M x 32) / 1GB (4 x 64M x 32) NOR Flash Multi-Chip Package 3V Page Mode Memory

FEATURES

- Single power supply operation
 - 3 Volt read, erase, and program operations
- I/O Control
 - Wide I/O voltage range (V_{IO}): 1.8V to V_{CC}
 - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input.
- Separate 1024-byte One Time Program (OTP) array with two lockable regions
- Uniform sector architecture
 - One thousand twenty four 128 Kbyte sectors
- 100,000 erase cycles per sector typical
- 20-year data retention typical
- Commercial, industrial and military temperature ranges
- Organized as 2 ranks of 64M x 32 (512MB),
4 ranks of 64M x 32 (1GB)

PERFORMANCE CHARACTERISTICS

- High Performance
 - 110, 120 ns
 - 32-byte page read buffer
 - 15, 20 ns page read times
 - 512-byte write buffer reduces overall programming time for multiple-word updates
- Package option
 - 107 BGA, 14mm x 17mm
 - 1.0mm pitch
- Footprint compatible with W764M32V1-XBX
- Software features
 - Suspend and resume commands for program and erase operations
 - Data# polling and toggle bits provide status
 - CFI (Common Flash Interface) parameter table
- Hardware features
 - Advanced Sector Protection (ASP)
 - Hardware reset input (RESET#) resets device
 - Status Register, data polling, and ready/busy pin methods to determine device status.

GENERAL DESCRIPTION

The W7264M32V1-XSBX device is a 3V single power flash memory and utilizes four chips organized as 67,108,864 words. The W7464M32V1-XSBX device is a 3V single power flash memory and utilizes eight chips organized as 67,108,864 words. These devices have a 32-bit wide data bus. One write enable per 16-bit data word. Each device requires a single 3 volt power supply for both read and write functions.

* This product is subject to change without notice.

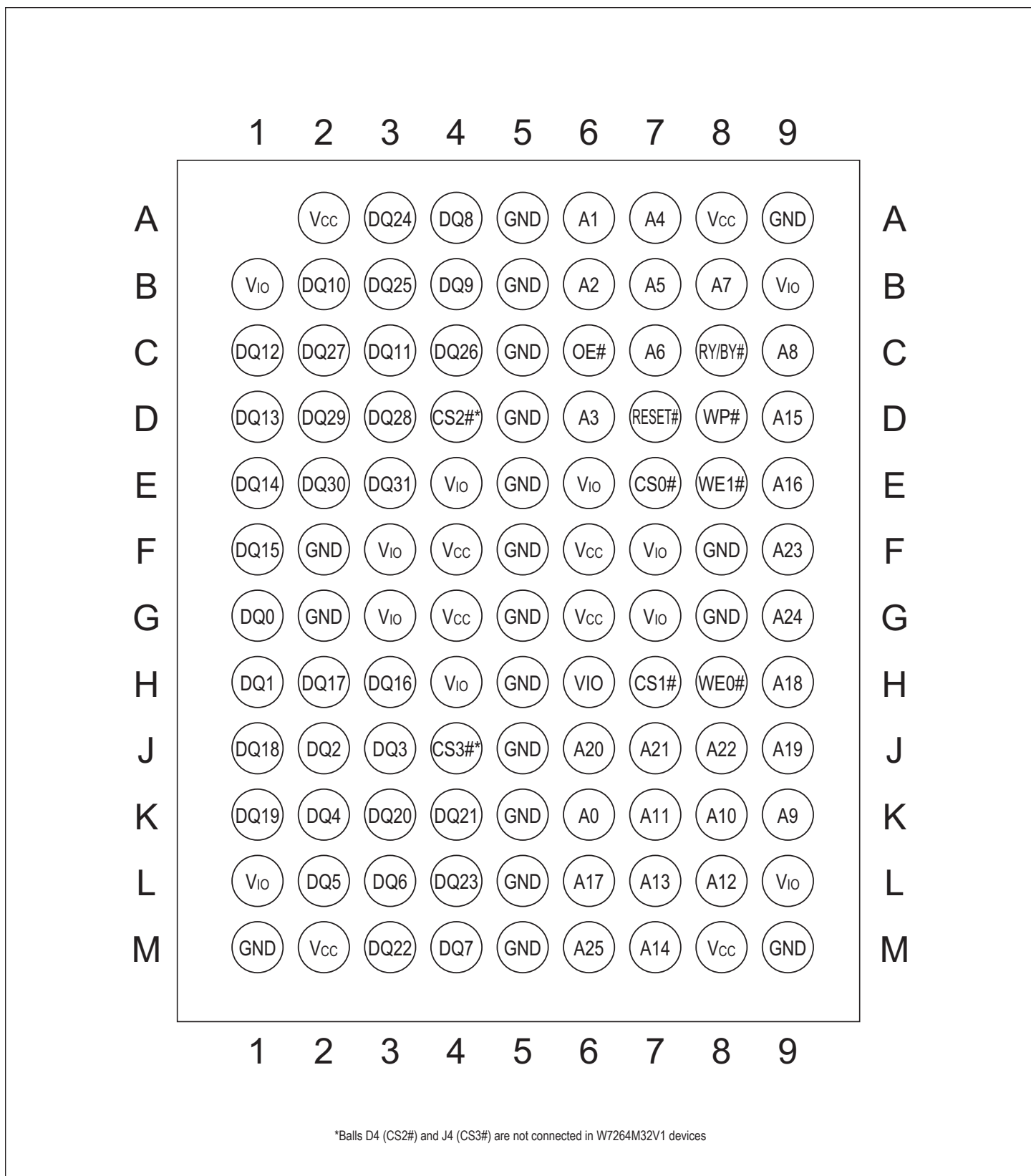
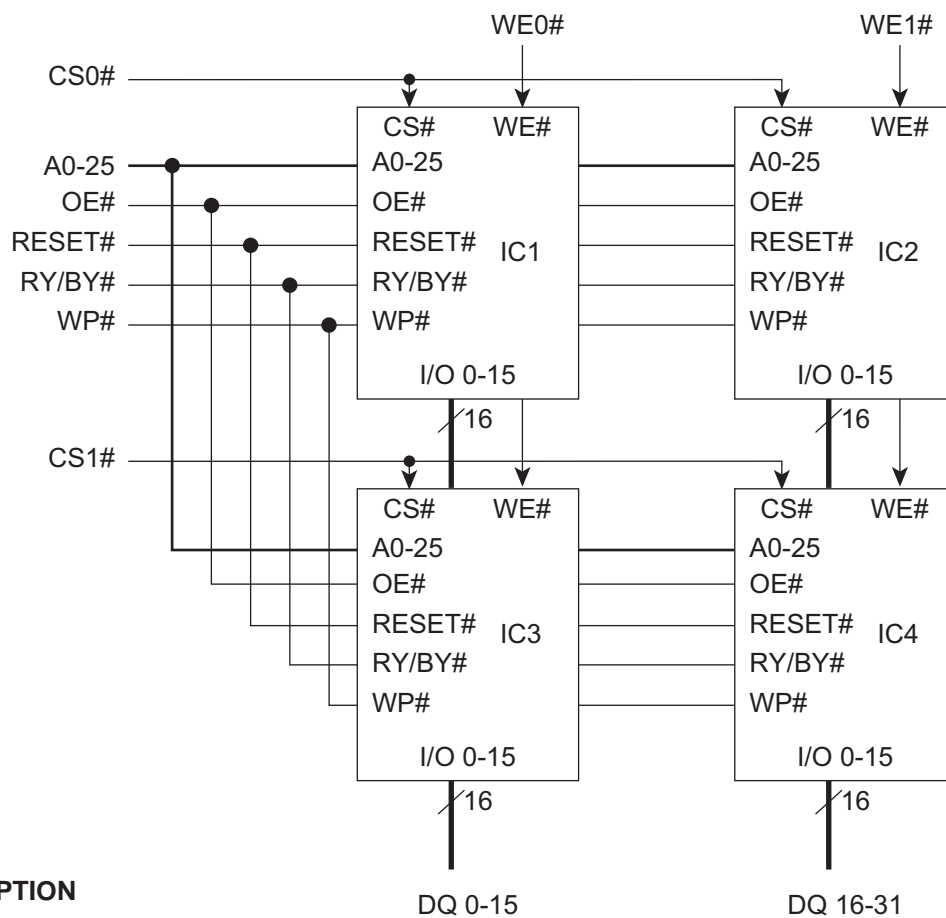
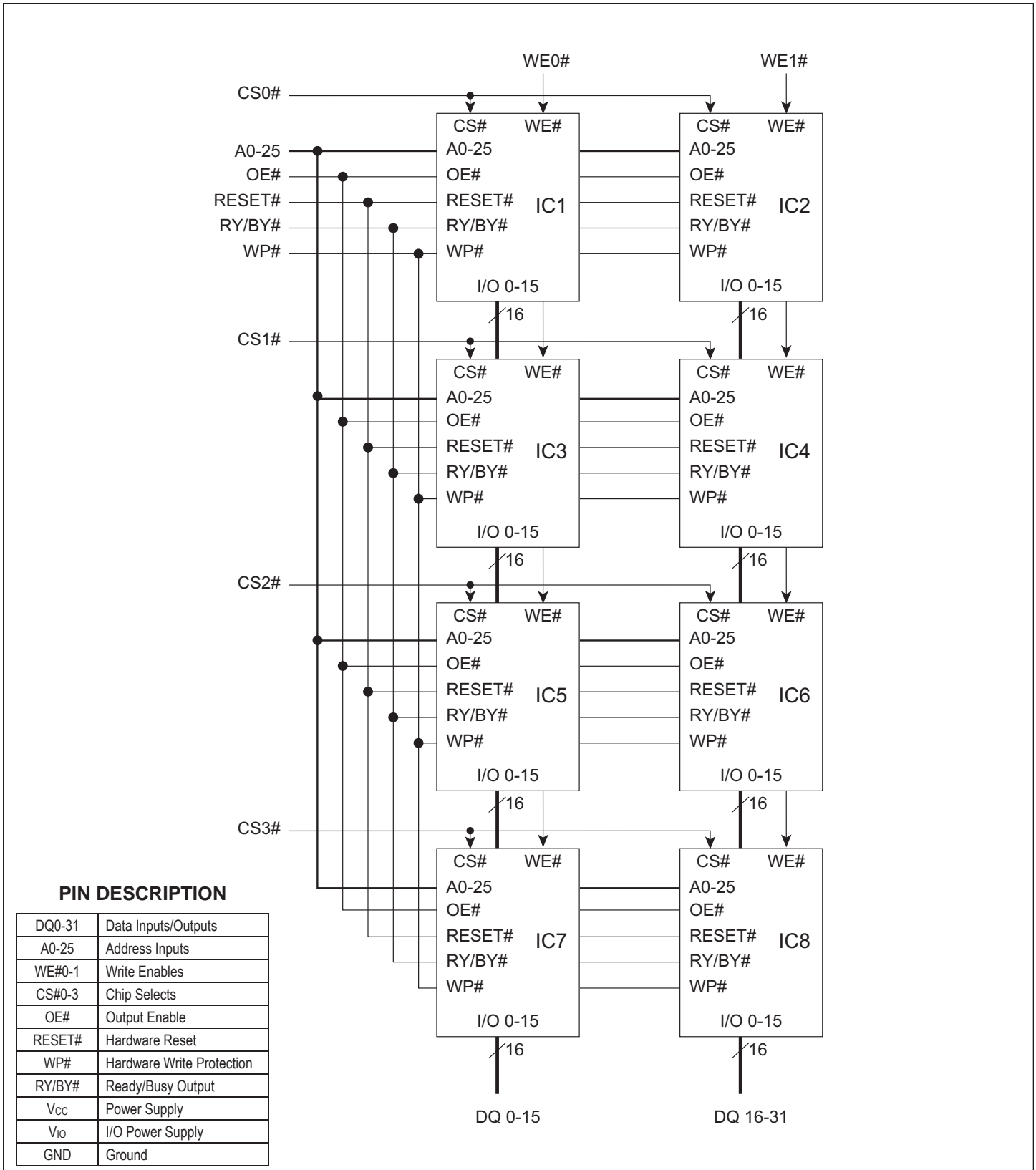
FIGURE 1 – PIN CONFIGURATION (TOP VIEW)


FIGURE 2 – W7264M32V1 (512MB) BLOCK DIAGRAM

PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-25	Address Inputs
WE#0-1	Write Enables
CS#0-1	Chip Selects
OE#	Output Enable
RESET#	Hardware Reset
WP#	Hardware Write Protection
RY/BY#	Ready/Busy Output
V _{CC}	Power Supply
V _{IO}	I/O Power Supply
GND	Ground

FIGURE 3 – W7464M32V1 (1GB) BLOCK DIAGRAM


ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range (other than RESET#)	-0.5 to $V_{IO} + 0.5$	V
I/O Voltage Range (V_{IO})	-0.5 to +4.0	V
RESET#	-0.5 to $V_{CC} + 0.5$	V
Storage Temperature Range	-55 to +125	°C

- NOTES:
- Minimum DC voltage on input or input or I/Os is -0.5V. During voltage transitions, inputs or I/Os pins may overshoot GND to -2.0V for periods of up to 20ns. Maximum DC voltage on input or I/Os pins is $V_{CC} + 0.5V$. During voltage transitions, input or I/O pins may overshoot to $V_{CC} + 2.0V$ for periods up to 20ns
 - Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of the data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
I/O Voltage	V_{IO}	1.7	$V_{CC} + 0.2$	V

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = V_{IO}$	V
Input Rise and Fall	1.5	ns
Input and Output Reference Level	$V_{IO} \times 0.5$	V
Output Timing Reference Level	$V_{IO} \times 0.5$	V

- NOTES:
- I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z_0 = 50\Omega$.
 V_z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

W7264M32V1 (512MB) BGA THERMAL RESISTANCE

Description	Symbol	Typical	Units	Notes
Junction to Board	Theta JB	16.3	°C/W	1
Junction to Case (Top)	Theta JC	11.9	°C/W	1

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

W7464M32V1 (1GB) BGA THERMAL RESISTANCE

Description	Symbol	Typical	Units	Notes
Junction to Board	Theta JB	20.4	°C/W	1
Junction to Case (Top)	Theta JC	14.9	°C/W	1

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

DC CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Max	Unit
Input Load Current (512MB)	I _{LI}	V _{IN} = V _{SS} to V _{CC} , V _{CC} = V _{CC(MAX)}		±4.0	µA
Output Leakage Current (512MB)	I _{LO}	V _{OUT} = V _{SS} to V _{CC} , V _{CC} = V _{CC(MAX)}		±2.0	µA
Input Load Current (1GB)	I _{LI}	V _{IN} = V _{SS} to V _{CC} , V _{CC} = V _{CC(MAX)}		±8.0	µA
Output Leakage Current (1GB)	I _{LO}	V _{OUT} = V _{SS} to V _{CC} , V _{CC} = V _{CC(MAX)}		±4.0	µA
V _{CC} Active Current for Read (6)	I _{CC1}	CS# = V _{IL} , OE# = V _{IH} , V _{CC} = V _{CC(MAX)} ; address switching at 5MHz		120	mA
V _{CC} Intra-Page Read Current (6)	I _{CC2}	CS# = V _{IL} #, OE# = V _{IH} , V _{CC} = V _{CC(MAX)} ; f = 33MHz		50	mA
V _{CC} Active Erase/Program Current (1, 6)	I _{CC3}	CS# = V _{IL} #, OE# = V _{IH} , V _{CC} = V _{CC(MAX)}		200	mA
V _{CC} Standby Current (512MB) (7)	I _{CC4}	CS#, RESET#, OE# = V _{IH} , V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC MAX}		800	µA
V _{CC} Standby Current (1GB) (7)	I _{CC4}	CS#, RESET#, OE# = V _{IH} , V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC MAX}		1.6	mA
V _{CC} Reset Current (3, 5, 6)	I _{CC5}	CS# = V _{IH} , RESET# = V _{IL} , V _{CC} = V _{CC MAX}		40	mA
Automatic Sleep Mode (512MB) (2, 5, 7)	I _{CC6}	V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC MAX} , t _{ACC} + 30 ns		12	mA
		V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC MAX} , t _{ASSB}		800	µA
Automatic Sleep Mode (1GB) (2, 5, 7)	I _{CC6}	V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC MAX} , t _{ACC} + 30 ns		24	mA
		V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC MAX} , t _{ASSB}		1.6	mA
V _{CC} current during power up (5, 6)	I _{CC7}	RESET# = V _{IO} , CS# = V _{IO} , V _{CC} = V _{CC MAX}		160	mA
Input Low Voltage	V _{IL}		-0.5	0.3 x V _{IO}	V
Input High Voltage	V _{IH}		0.7 x V _{IO}	V _{IO} + 0.4	V
Output Low Voltage (4)	V _{OL}	I _{OL} = 100 µA for DQs, I _{OL} = 2mA for RY/BY#		0.15 x V _{IO}	V
Output High Voltage	V _{OH}	I _{OH} = 100 µA	0.85 x V _{IO}		V
Low V _{CC} Lock-Out Voltage (5)	V _{LKO}		2.25	2.5	V

NOTES:

- I_{CC} active while Embedded Algorithm is in progress.
- Automatic sleep mode enables the lower power mode when addresses remain stable for the specified designated time.
- If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
- The recommended pull-up resistor for RY/BY# output is 5k to 10k Ohms.
- Guaranteed by design, not tested
- Current value is for 1-rank of 32-bit data flash only.
- Max value when all chips of the device are in this low power mode

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

Parameter	Symbol		-110		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	60		60		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	25		25		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	30		30		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		45		ns
Write Enable Pulse Width High (3)	t _{WHWL}	t _{WPH}	20		20		ns
Single Word Programming Time (1)	t _{WHWH1}			400		400	μs
Buffer Programming Time				750		750	μs
Sector Erase (2)	t _{WHWH2}			1.1		1.1	sec
Read Recovery Time before Write (3)	t _{GHWL}		0		0		ns
Address Setup Time to OE# low during toggle bit polling		t _{ASO}	15		15		ns
Write Recovery Time from RY/BY# (3)		t _{RB}	0		0		ns
Program/Erase Valid to RY/BY# (3)		t _{BUSY}		80		80	ns

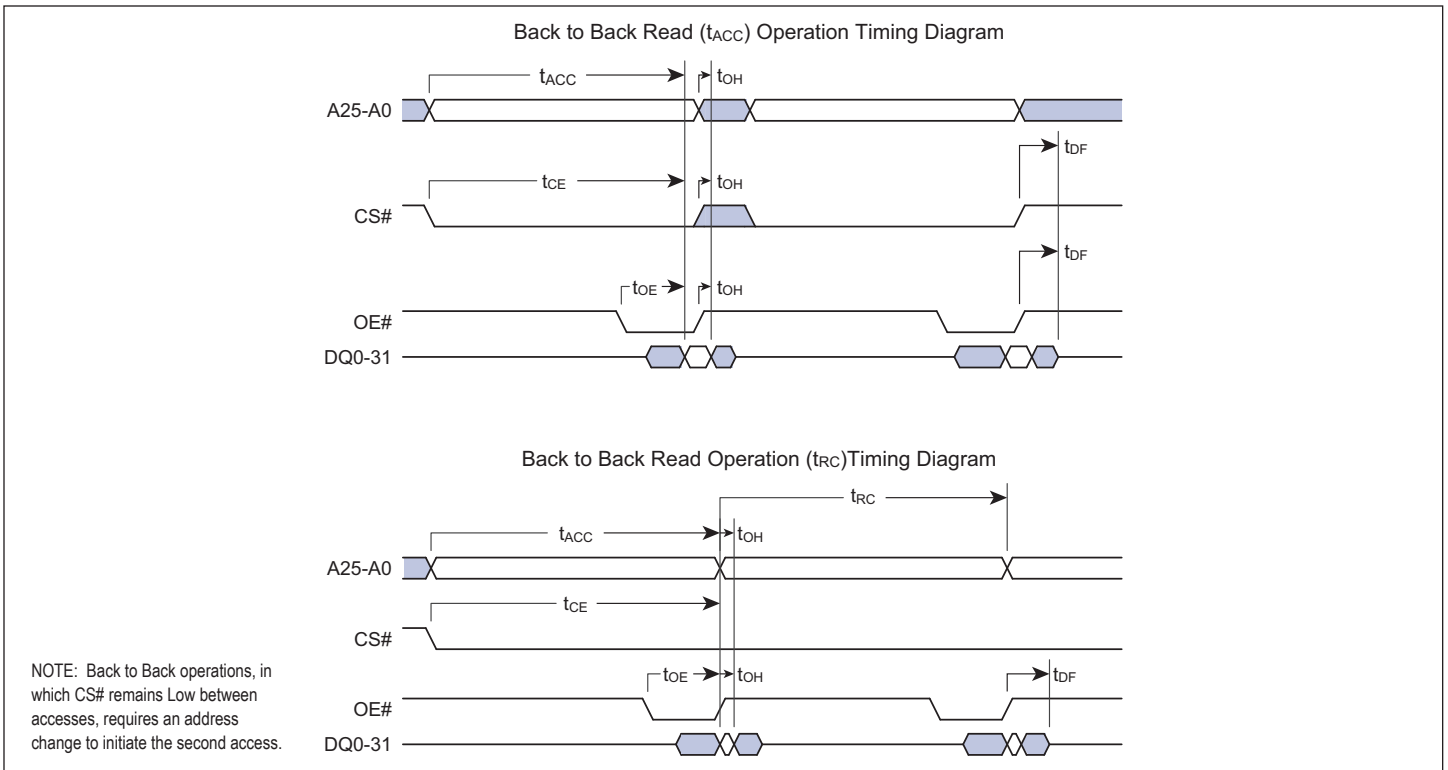
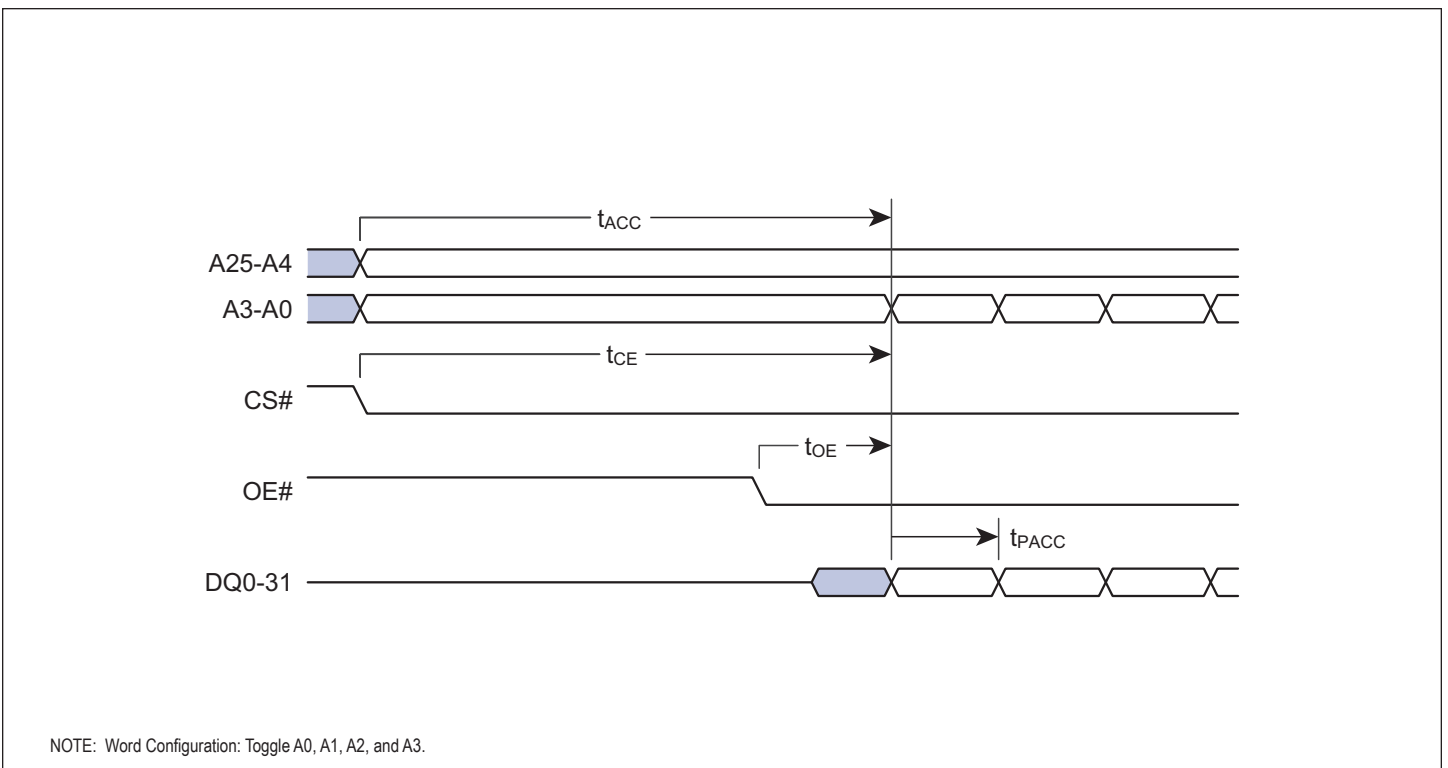
NOTES:

1. Typical value for t_{WHWH1} is 125 μs.
2. Typical value for t_{WHWH2} is 0.275 sec.
3. Guaranteed by design, not tested.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

Parameter	Symbol		-110		-120		Unit
			Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	110		120		ns
Address Access Time	t _{AVQV}	t _{ACC}		110		120	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		110		120	ns
Page Access Time		t _{PACC}		15		20	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		25		25	ns
Chip Select High to Output High Z	t _{EHQZ}	t _{DF}		15		15	ns
Output Enable High to Output High Z	t _{GHQZ}	t _{DF}		15		15	ns
Output Hold from Addresses, CS# or OE# Change, Whichever occurs first	t _{AXQX}	t _{OH}	0		0		ns
Output Enable Hold Time (1)	Read	t _{OEH}	0		0		ns
	Toggle and Data# Polling		10		10		ns

1. Guaranteed by design, not tested.

FIGURE 5 – AC WAVEFORMS FOR READ OPERATIONS

FIGURE 6 – PAGE READ TIMING


POWER ON AND RESET PARAMETERS

Parameter	Description	Limit	Value	Unit
t_{VCS}	V_{CC} Setup Time to first access (1, 2)	Min	300	μs
t_{VIO}	V_{IO} Setup Time to first access (1, 2)	Min	300	μs
t_{RPH}	RESET# Low to CS# Low (1, 2)	Min	35	μs
t_{RP}	RESET# Pulse Width	Min	200	ns
t_{RH}	Time between RESET# (High) and CS# (low) (1)	Min	50	ns
t_{CEH}	CS# Pulse Width High (1)	Min	20	ns

NOTES:

1. Not tested.
2. Timing measured from V_{CC} reaching V_{CC} minimum and V_{IO} reaching V_{IO} minimum to V_{IH} on Reset and V_{IL} on CS#.
3. RESET# Low is optional during POR. If RESET is asserted during POR, the later of t_{RPH} , t_{VIO} , or t_{VCS} will determine when CS# may go Low. If RESET# remains Low after t_{VIO} , or t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VIO} , or t_{VCS} . RESET must also be High t_{RH} before CS# goes Low.
4. $V_{CC} \geq V_{IO} - 200$ mV during power-up.
5. V_{CC} and V_{IO} ramp rate can be non-linear.
6. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH} .

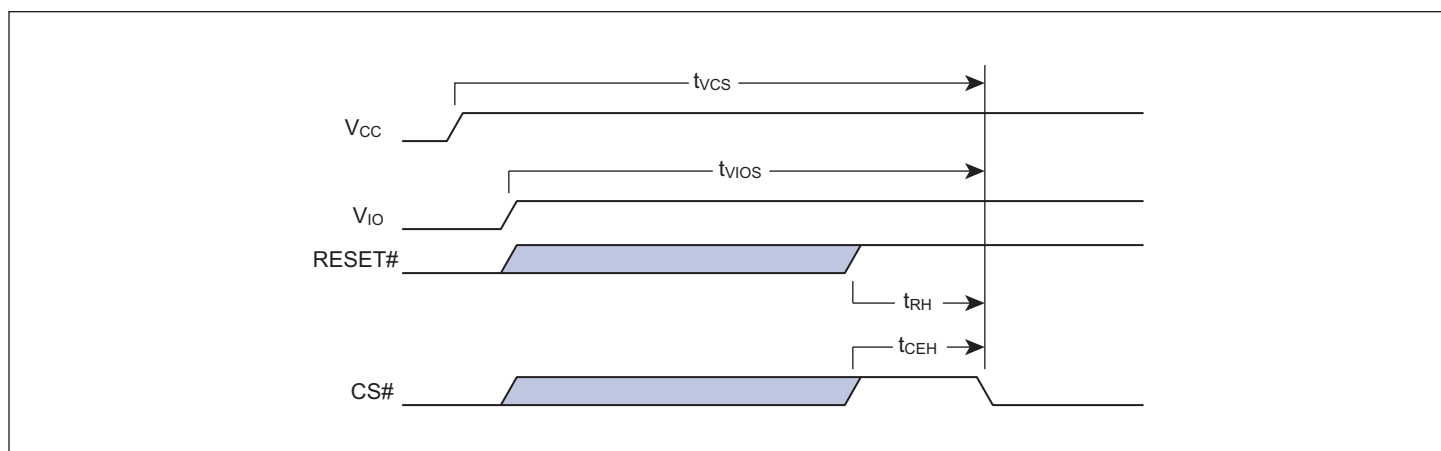
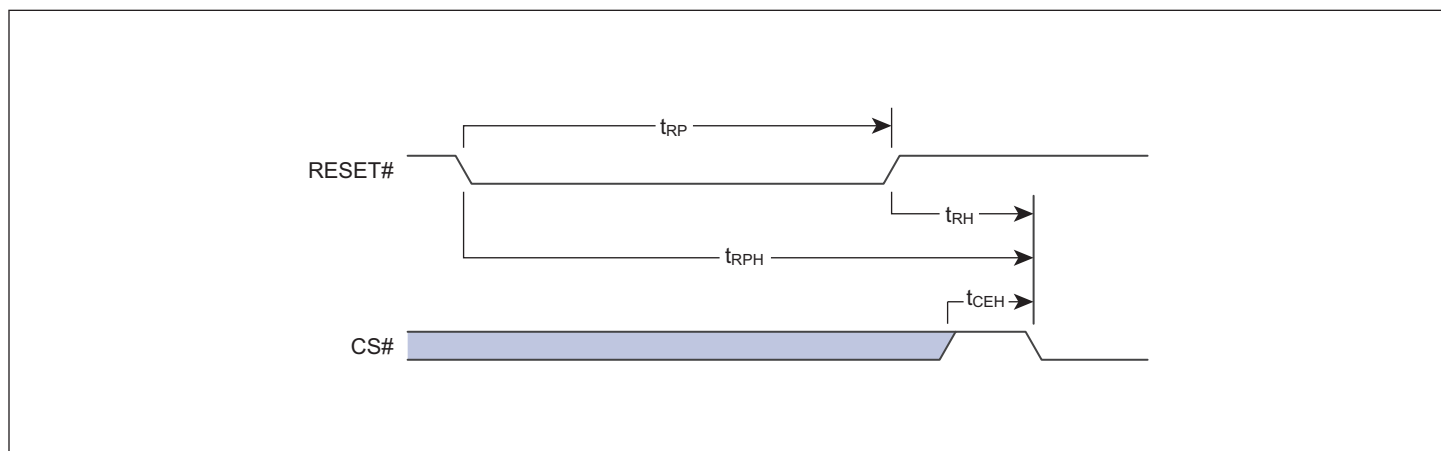
FIGURE 7 – POWER-UP DIAGRAM

FIGURE 8 – HARDWARE RESET


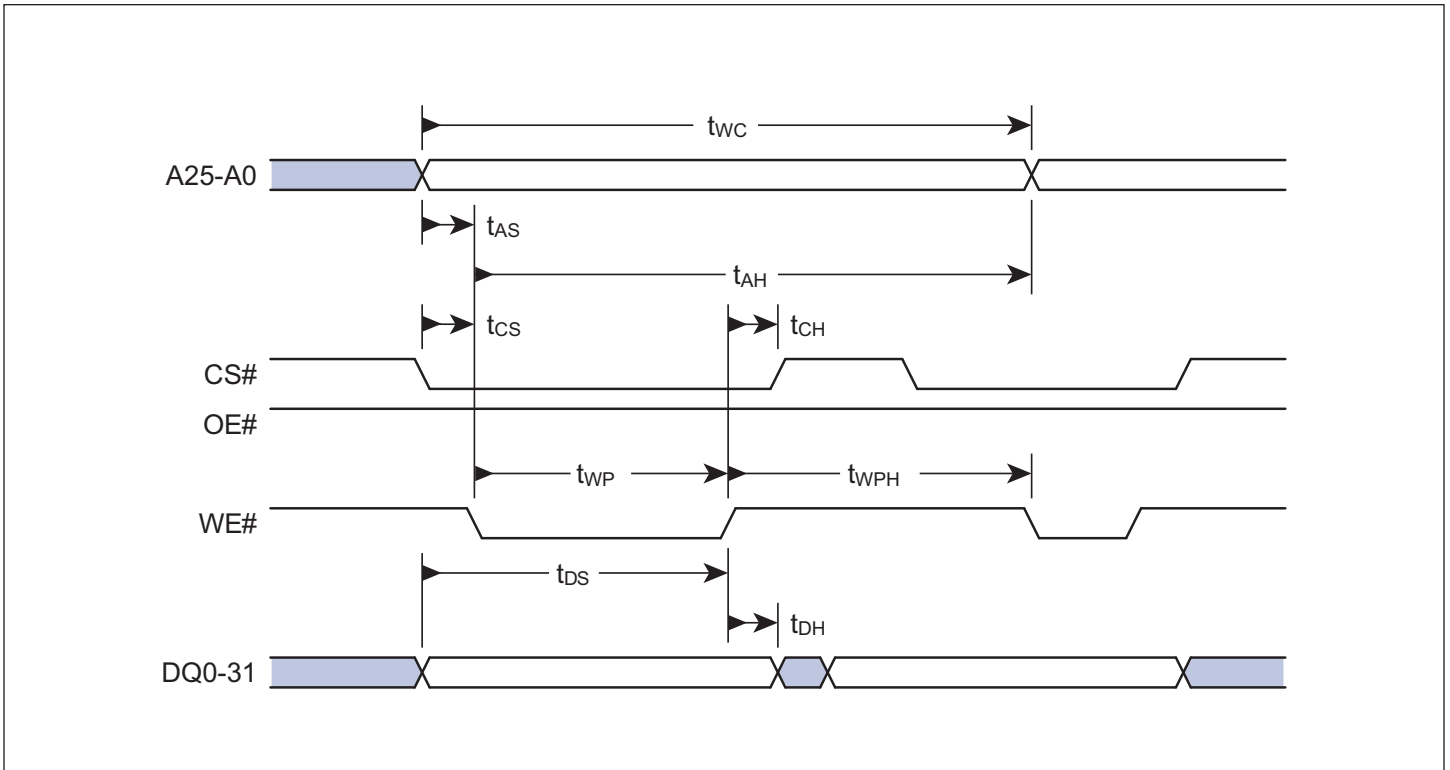
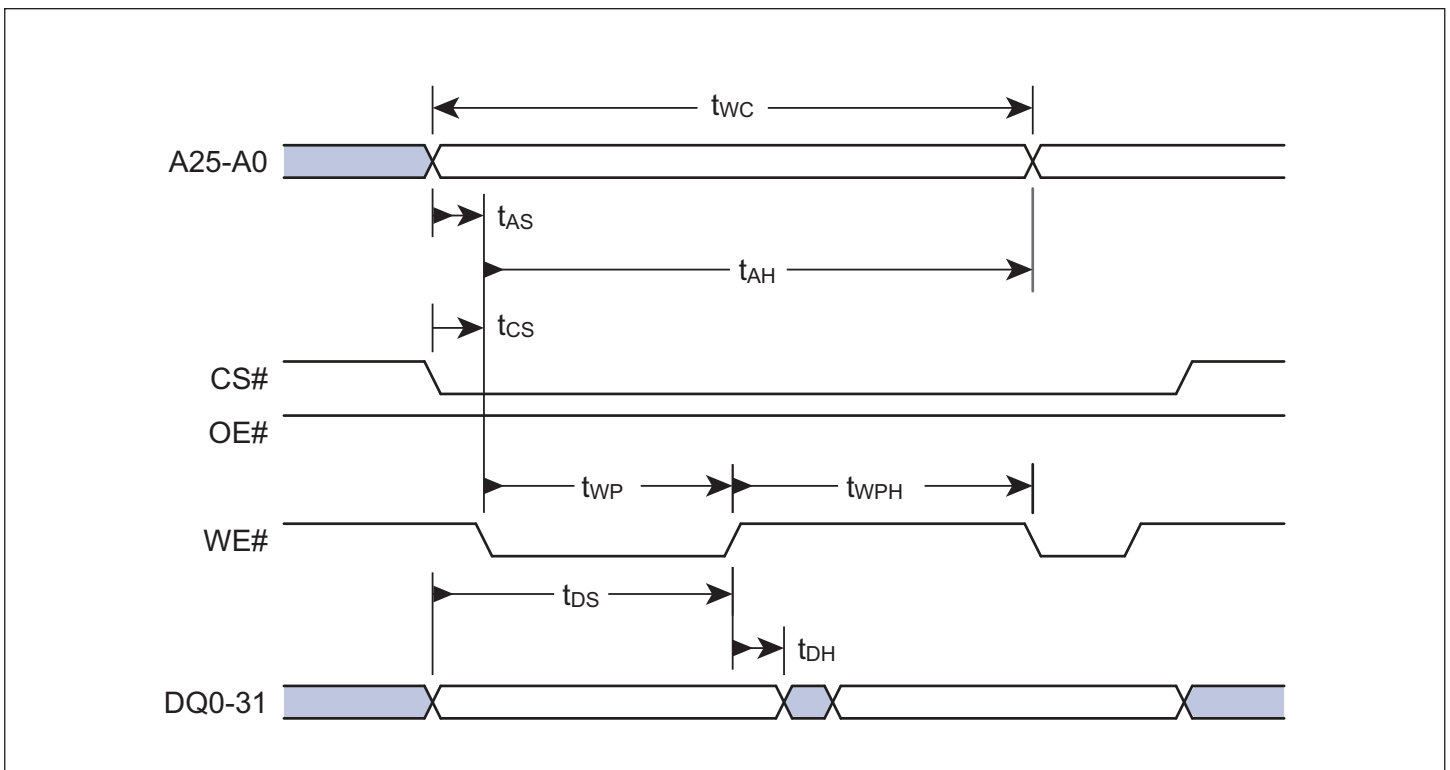
FIGURE 9 – BACK TO BACK WRITE OPERATION TIMING DIAGRAM

FIGURE 10 – BACK TO BACK (CS#V_{IL}) WRITE OPERATION TIMING DIAGRAM


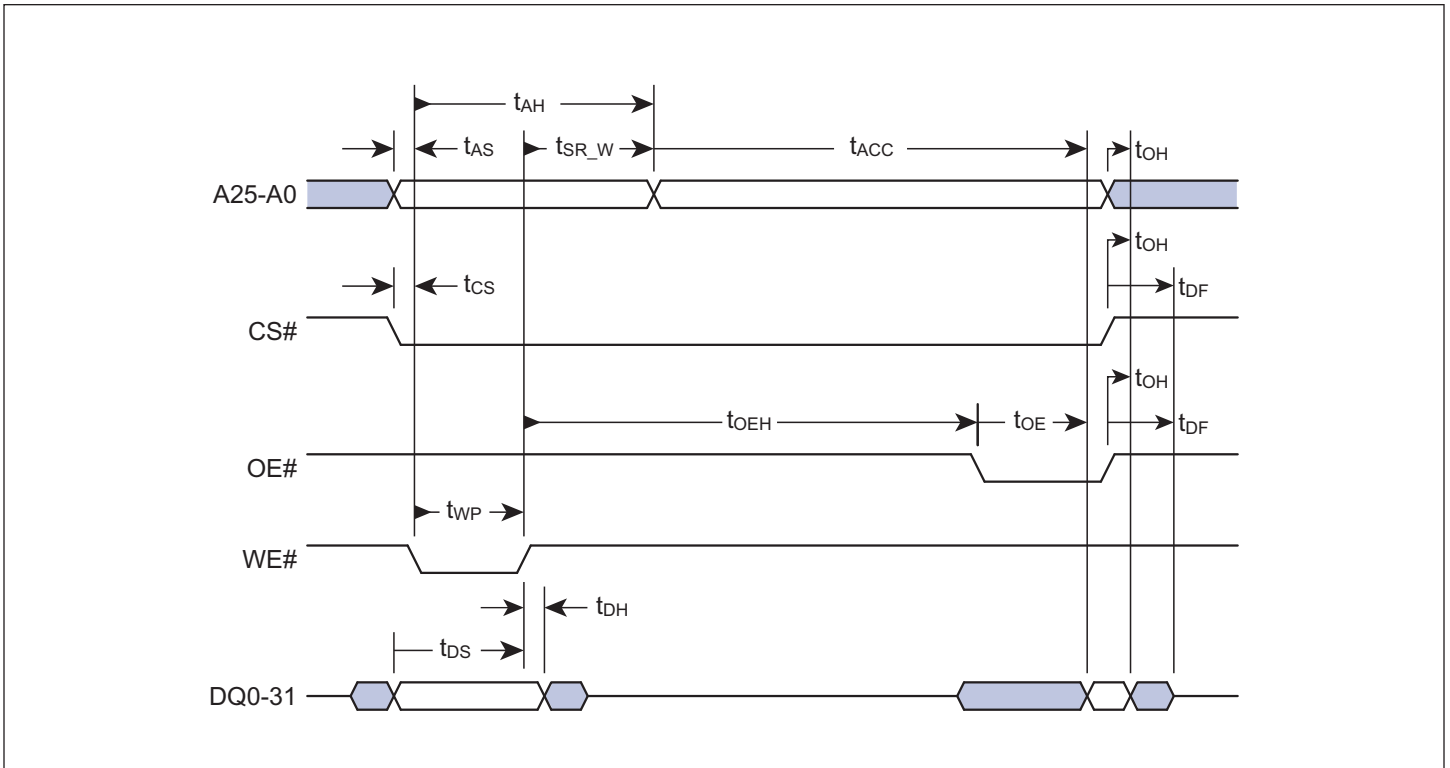
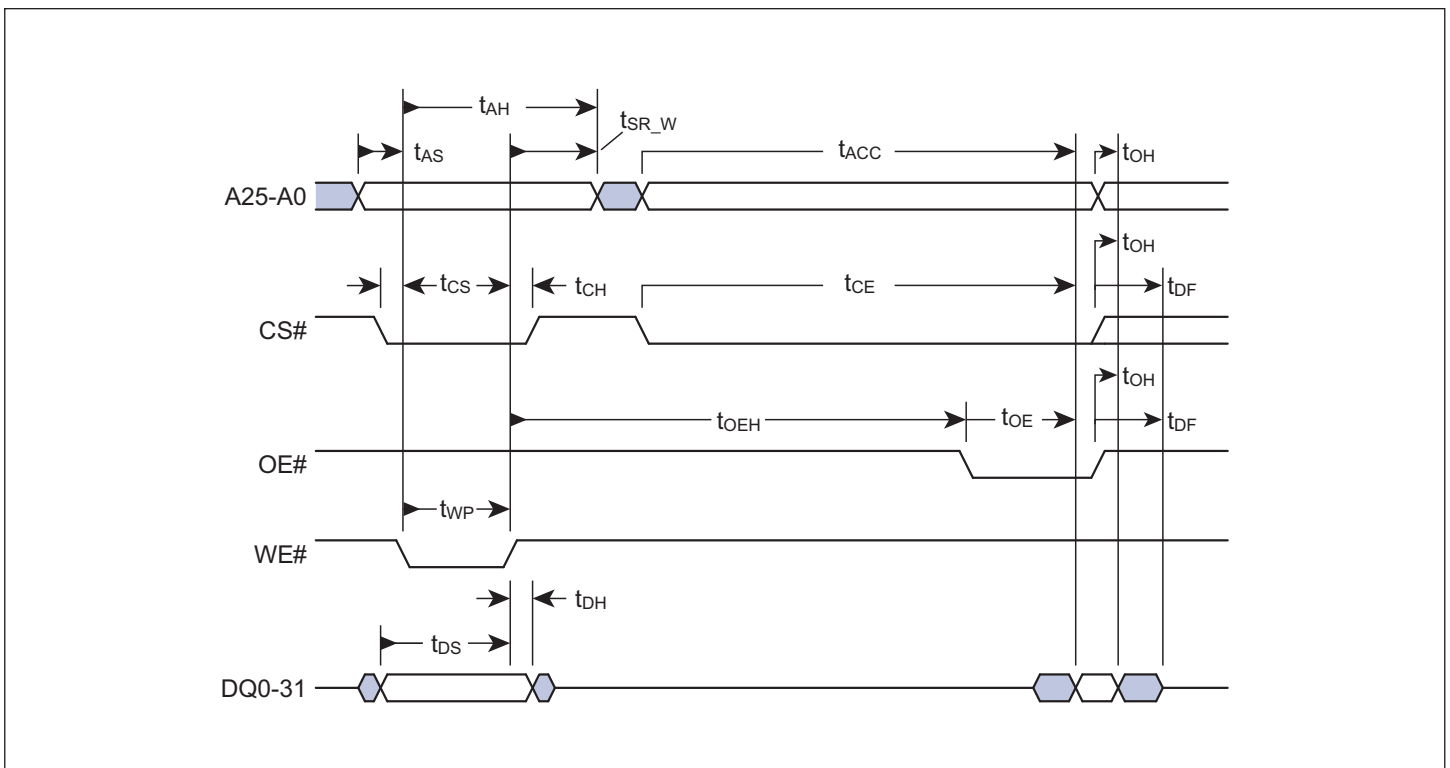
FIGURE 11 – WRITE TO READ (t_{ACC}) OPERATION TIMING DIAGRAM

FIGURE 12 – WRITE TO READ (t_{CE}) OPERATION TIMING DIAGRAM




FIGURE 13 – READ TO WRITE (CS# V_{IL}) OPERATION TIMING DIAGRAM

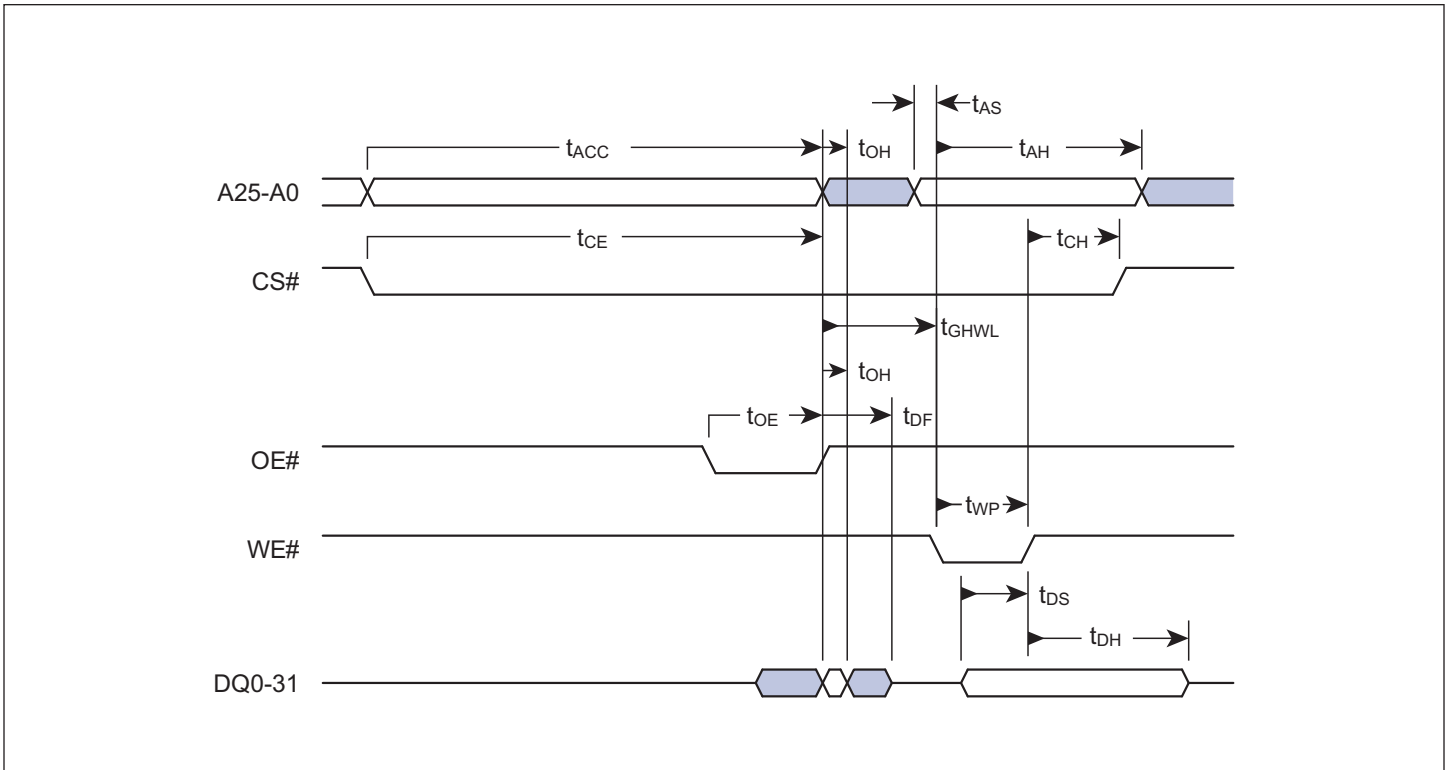


FIGURE 14 – READ TO WRITE (CS# TOGGLE) OPERATION TIMING DIAGRAM

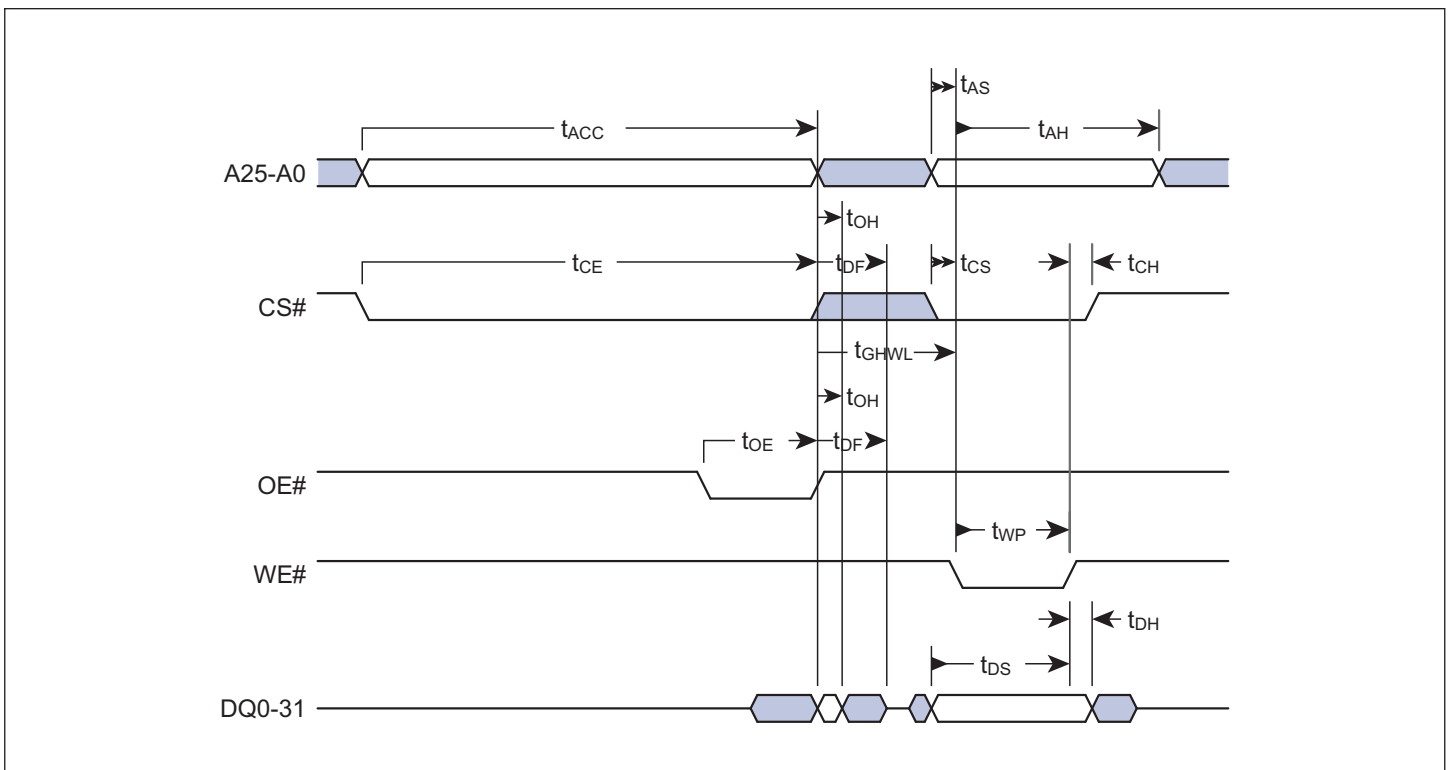


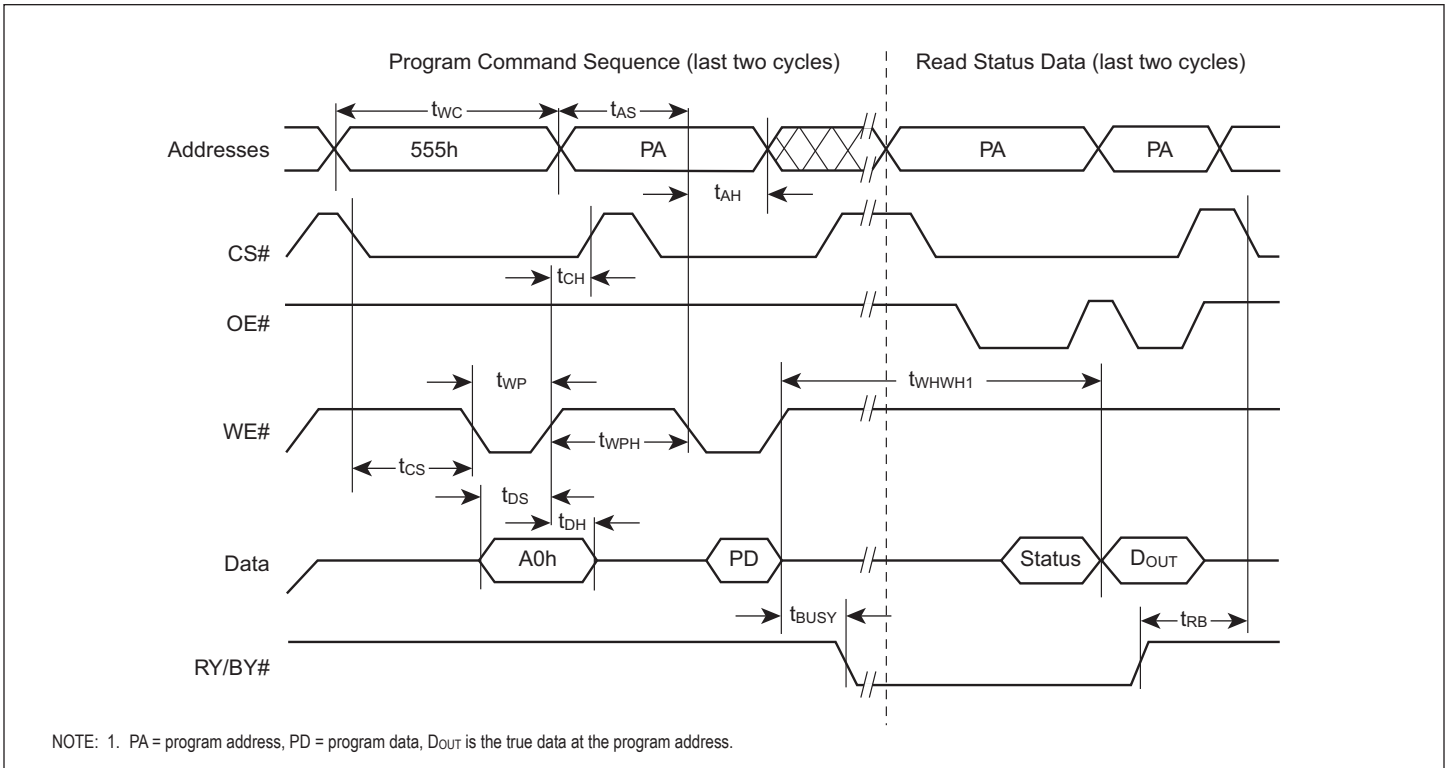
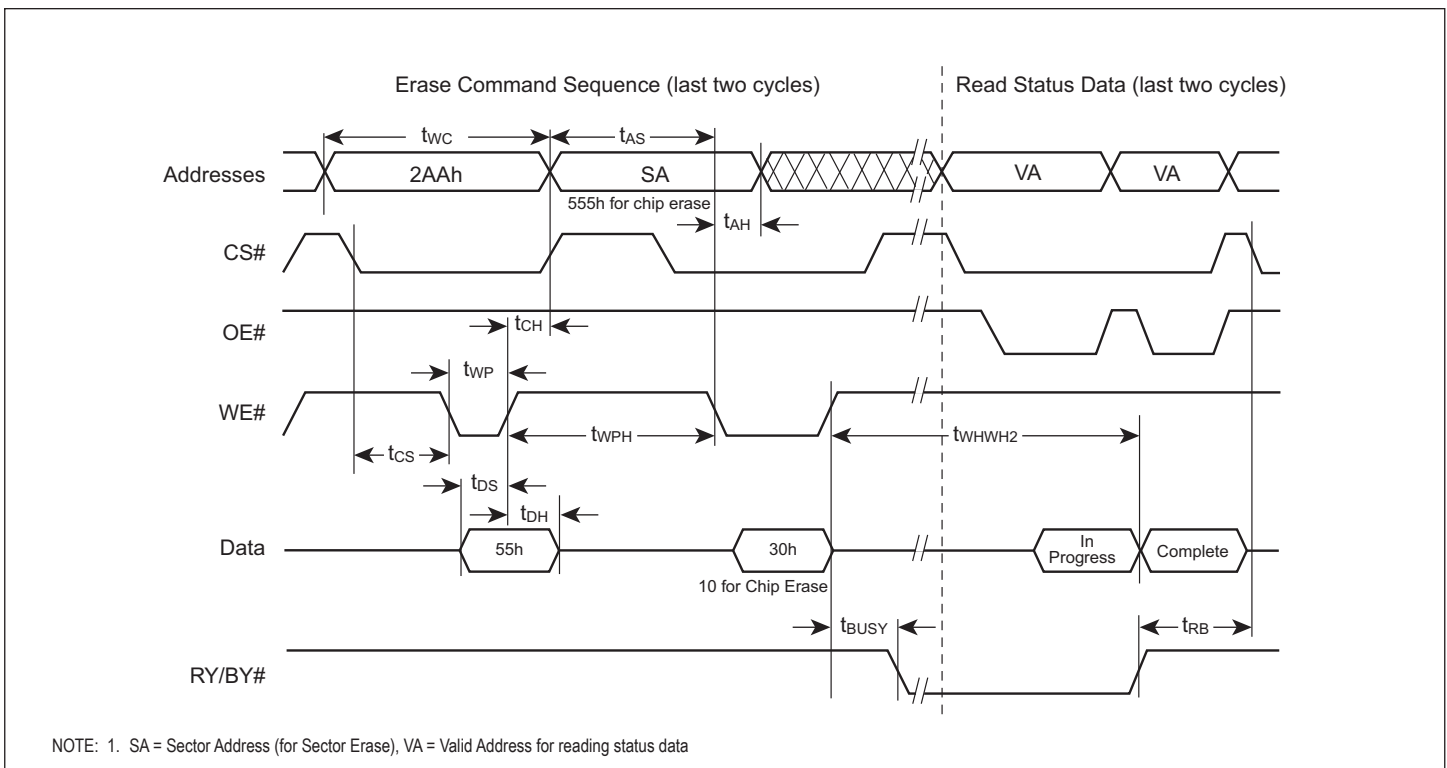
FIGURE 15 – PROGRAM OPERATIONS

FIGURE 16 – CHIP/SECTOR ERASE OPERATION TIMINGS




FIGURE 17 – DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)

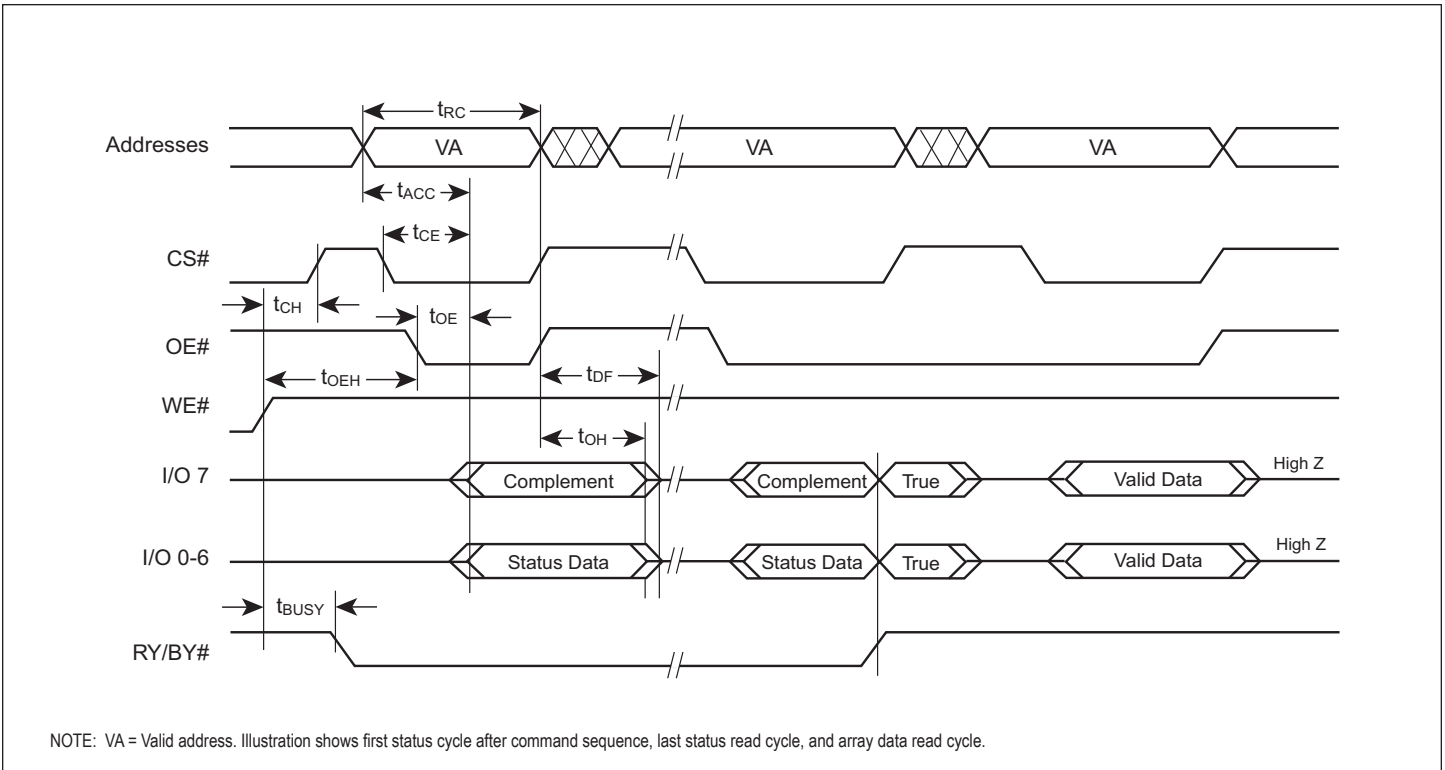


FIGURE 18 – TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)

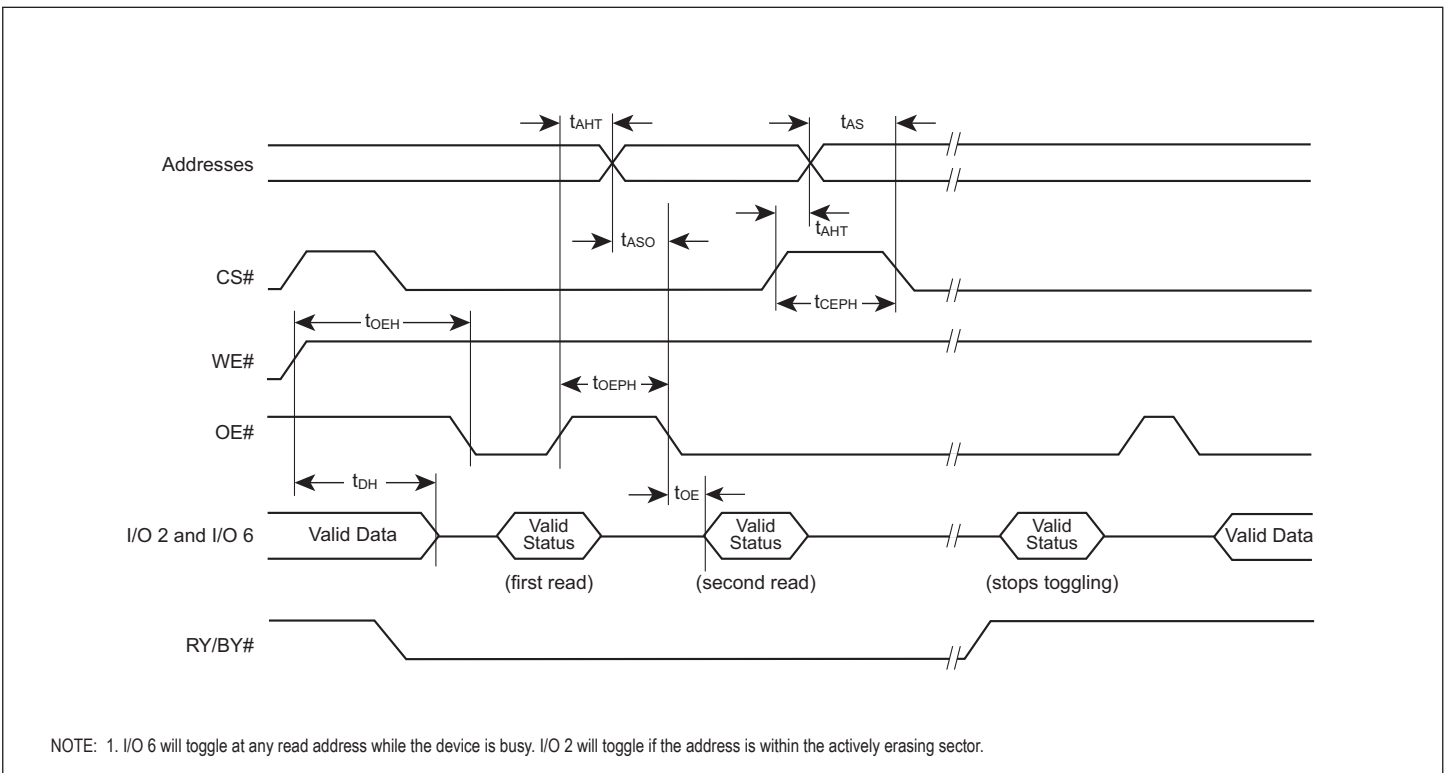
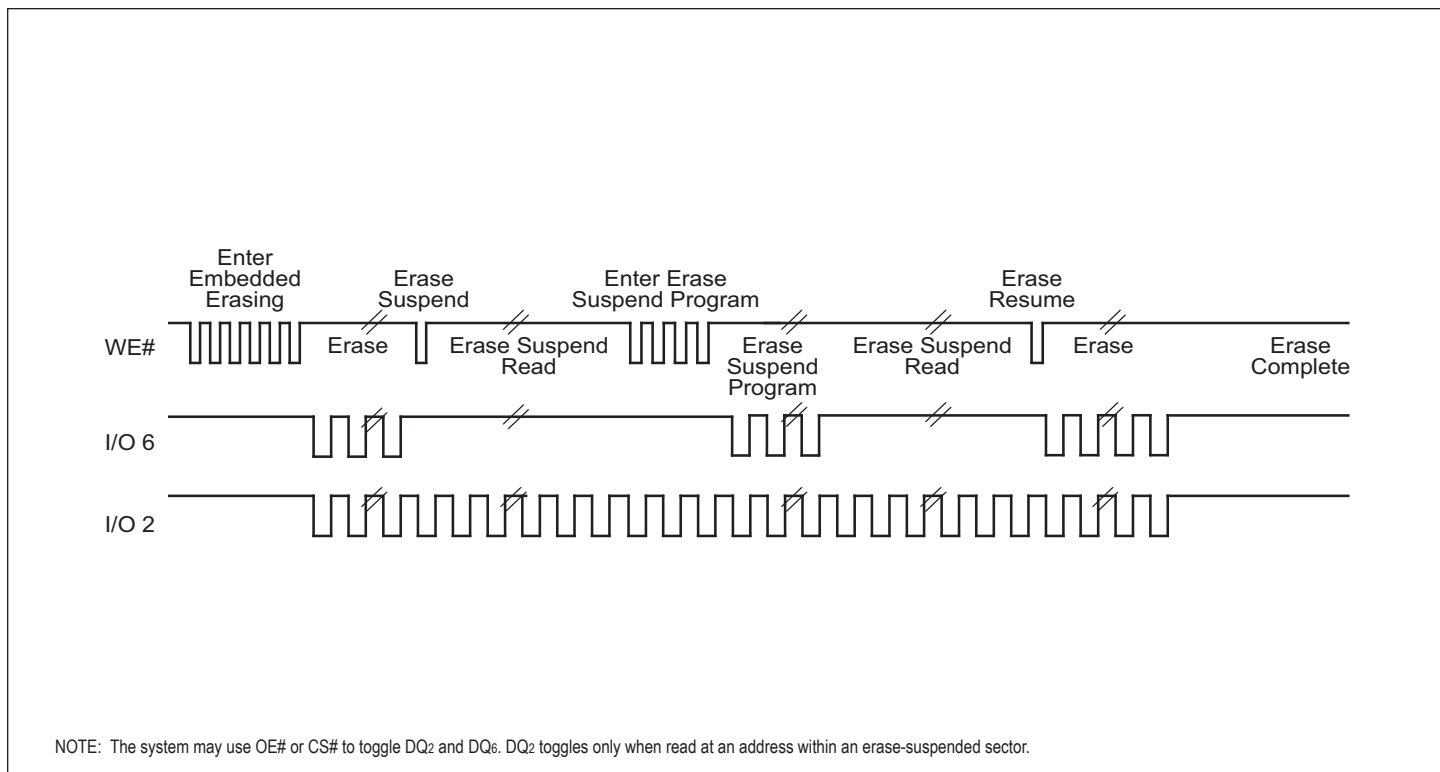
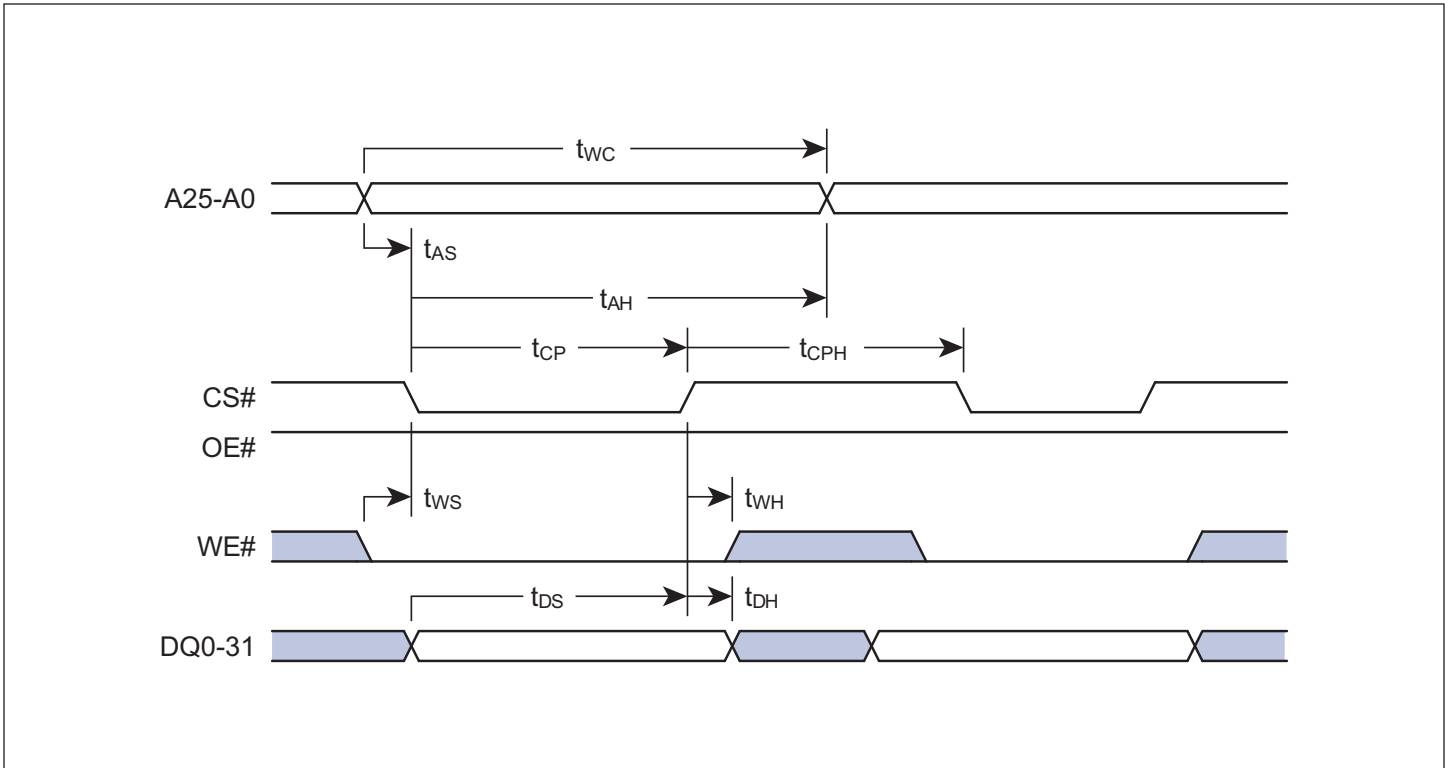
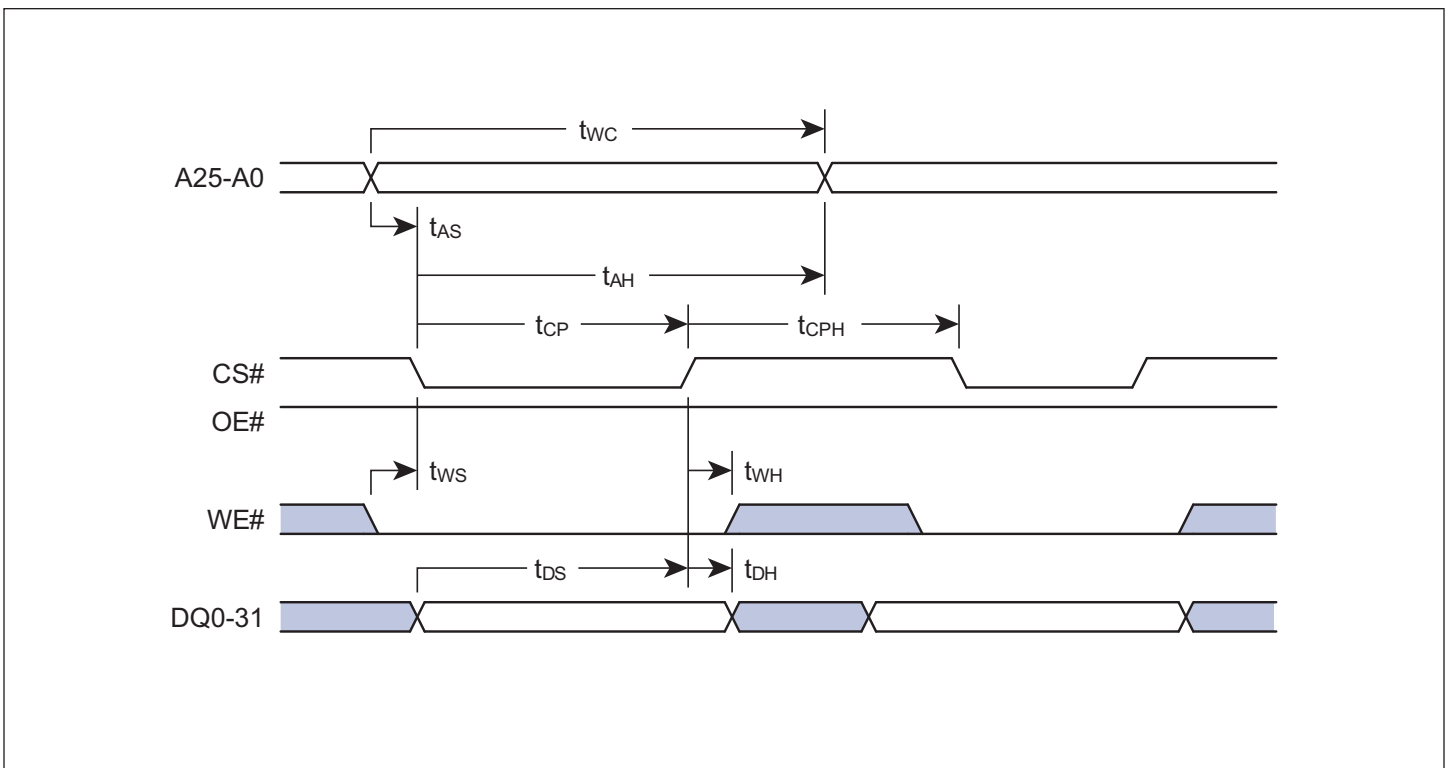
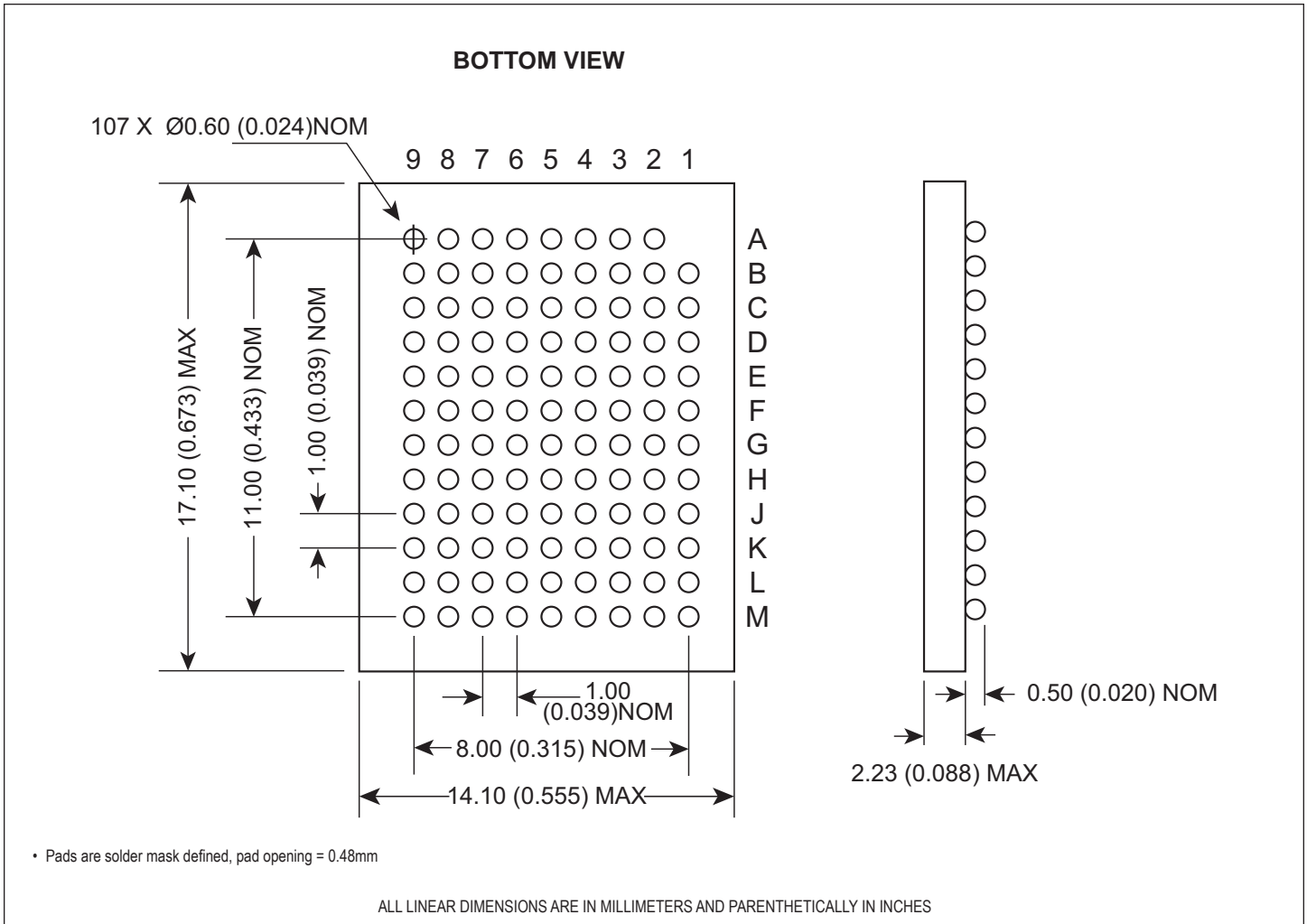


FIGURE 19 – I/O 2 Vs. I/O 6

AC CHARACTERISTICS – ALTERNATE CS# CONTROLLED ERASE AND PROGRAM OPERATIONS

Parameter		Description		Speed Options		Unit
JEDEC	Std			110	120	
t _{AVAV}	t _{WC}	Write Cycle Time	Min	60	60	ns
t _{AVWL}	t _{AS}	Address Setup Time	Min	0	0	ns
t _{ELAX}	t _{AH}	Address Hold Time	Min	45	45	ns
	t _{AHT}	Address Hold Time From CS# or OE# High during toggle bit polling	Min	0	0	ns
t _{DVEH}	t _{DS}	Data Setup Time	Min	30	30	ns
t _{EHDX}	t _{DH}	Data Hold Time	Min	0	0	ns
	t _{CEPH}	CS# High during toggle bit polling (1)	Min	20	20	ns
	t _{OEPH}	OE# High during toggle bit polling (1)	Min	20	20	ns
t _{GHLEL}	t _{GHLEL}	Read Recovery Time Before Write (OE# High to WE# Low) (1)	Min	0	0	ns
t _{WLLEL}	T _{WS}	WE# Setup Time	Min	0	0	ns
t _{EHWH}	t _{WH}	WE# Hold Time	Min	0	0	ns
t _{ELEH}	t _{CP}	CS# Pulse Width	Min	25	25	ns
t _{EHEL}	t _{CPH}	CS# Pulse Width High	Min	20	20	ns
t _{WHWH1}	t _{WHWH1}	Buffer Programming Time	Typ	180	180	μs
t _{WHWH2}	t _{WHWH2}	Sector Erase Operation	Typ	0.3	0.3	sec

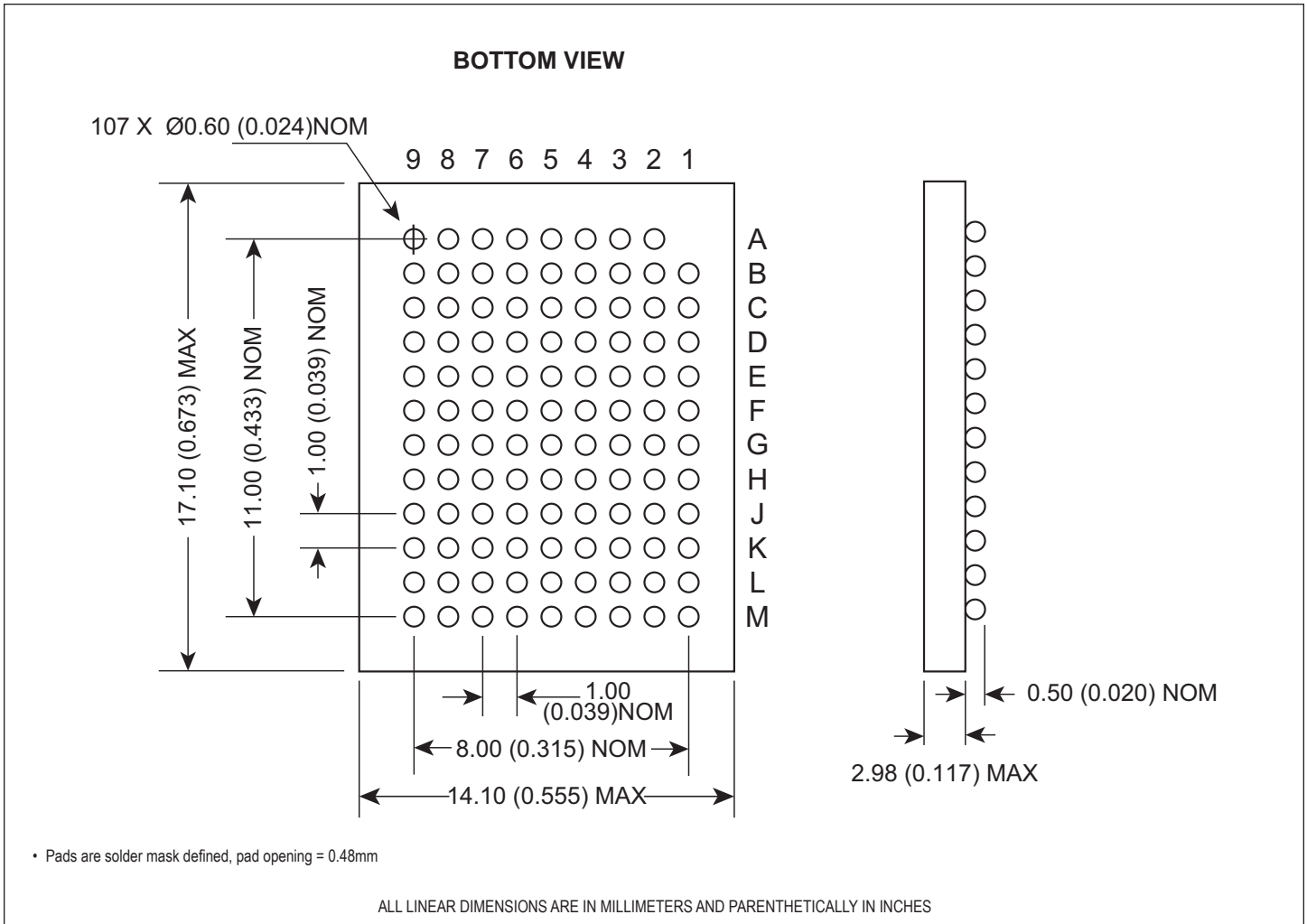
NOTE: 1. Not tested.

FIGURE 20 – BACK TO BACK (CS#) WRITE OPERATION TIMING DIAGRAM

FIGURE 21 – (CS#) WRITE TO READ OPERATION TIMING DIAGRAM


W7264M32V1 (512MB) – 107 PBGA (PLASTIC BALL GRID ARRAY)




W7464M32V1 (1GB) – 107 PBGA (PLASTIC BALL GRID ARRAY)





ORDERING INFORMATION

W 7 X 64M32 V 1 - XXX SB X

MICROSEMI CORPORATION _____

NOR FLASH _____

Rank _____

2 = 2 ranks of 64M x 32 (512MB)

4 = 4 ranks of 64M x 32 (1GB)

ORGANIZATION, 64M x 32 _____

3.3V POWER SUPPLY _____

1 = 1G Based Component _____

ACCESS TIME (ns) _____

110 = 110ns

120 = 120ns

PACKAGE TYPE _____

SB = 107 PBGA, 14mm x 17mm

DEVICE GRADE _____

M = Military -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

Blank = No temperature range specified for non-qualified product

Document Title

512MB (2 x 64M x 32) / 1GB (4 x 64M x 32) NOR Flash Multi-Chip Package 3V Page Mode Memory

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	December 2012	Advanced
Rev 1	Changes (Pgs. 1, 5, 6, 7, 9, 15, 19) 1.1 Add V _{IO} for 1.8V operations 1.2 Misc. updates and timings 1.3 Change data sheet status to Preliminary	December 2013	Preliminary
Rev 2	Changes (Pgs. 1, 5, 6, 7, 9, 15, 19) 2.1 Remove marking code 2.2 Update DC characteristics table for I _{CC4} and I _{CC6} 2.3 Remove marking code from footprint 2.4 Remove ES from Access Time list in Ordering Information 2.5 Change data sheet status to Final	November 2014	Final
Rev 3	Change (Pg 1) 3.1 Correct data sheet status note on page 1	June 2015	Final
Rev 4	Change (Pg 5) (ECN #9628) 4.1 Update JB and JC	October 2015	Final