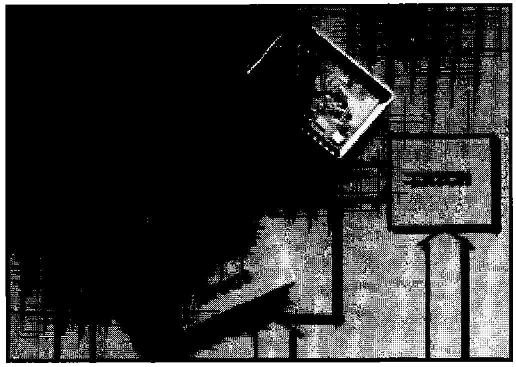
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9478
14-Bit, 500kHz Sampling A/D Converter

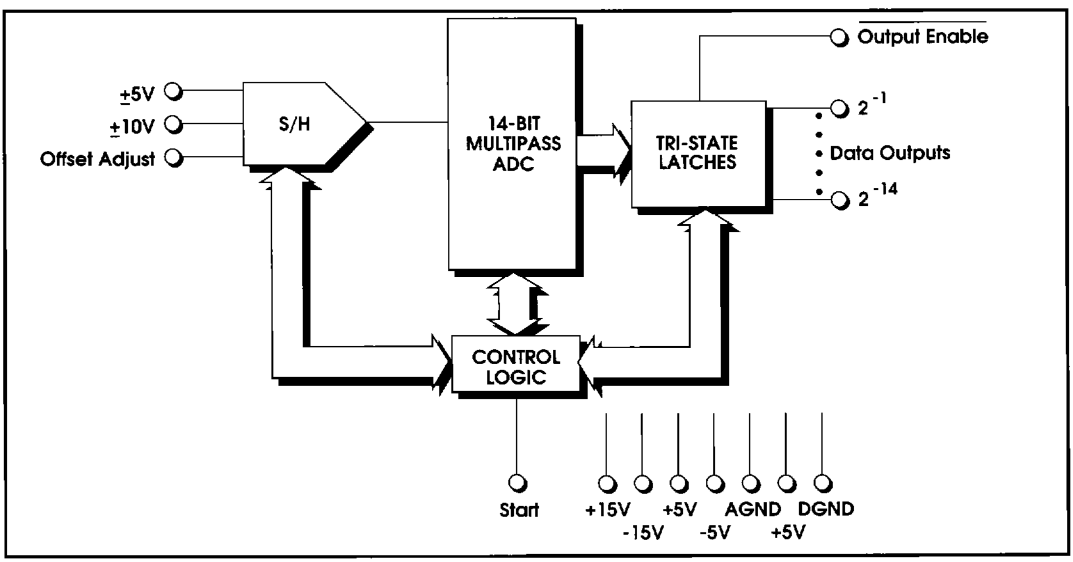


Features
- 500kHz Throughput
- 14-Bit Resolution
- Internal Sample-and-Hold
- Internal Reference
- Tri-state Outputs
- ±0.003% FSR Accuracy

Applications
- High-speed Data Acquisition
- Test Equipment
- Process Control
- Medical Instrumentation

The **SP9478** is a complete 14-bit ADC and high speed sample-and-hold in a single package. The **SP9478** features a 500kHz throughput rate, and is complete with an internal reference and all necessary control logic. Only a START command is required to control and initiate conversions.

User-selectable input full scale ranges of ±2.5V, ±5V and ±10V. Tri-state outputs provide easy microprocessor bus interfacing. Packaged in a 32-pin DIL metal package, the **SP9478** is available in both commercial (0°C to +70°C) and military (-55°C to +125°C) temperature ranges, with MIL-STD-883C screening.



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Specifications

(Typical @ 25°C and nominal supply voltages unless otherwise specified)

MODEL	SP9478C	SP9478B	UNITS
RESOLUTION	14	14	Bits
ANALOG INPUTS			
Voltage Range	±5, ±10	±5, ±10	Volts
Input Impedance	10K on ±5V FSR	10K on ±5V FSR	Ω
	20K on ±10V FSR	20K on ±10V FSR	Ω
DIGITAL INPUTS			
Logic levels			
Logic 1	2.4 min.	2.4 min.	Volts
Logic 0	0.4 max.	0.4 max.	Volts
Logic Loading	1 TTL load	1 TTL load	—
START Command	Positive edge triggered	Positive edge triggered	—
Output Enable (OE)	Active low	Active low	—
CONVERSION AND THROUGHPUT			
Throughput	500	500	kHz
A/D Conversion Time	1.2	1.2	µs
S/H Acquisition Time	0.8	0.8	µs
STATIC PERFORMANCE			
Integral Linearity			
@ 25°C	±1 max.	±1 max.	LSB
@+125°C	—	±4.2 max.	LSB
@-55°C	—	±3.6 max.	LSB
Differential Linearity			
@ 25°C	±0.5 typ.; ±1 max.	±0.5 typ.; ±1 max.	LSB
-55°C to +125°C	—	±0.5 typ.; ±1 max.	LSB
No missing codes	14 max.	14 max.	bits
Offset Error			
@ 25°C	±0.3%	±0.3%	FSR
-55°C to +125°C	—	±0.3%	FSR
Gain Error			
@ 25°C	±0.5%	±0.5%	FSR
-55°C to +125°C	—	±0.7%	FSR
DYNAMIC PERFORMANCE			
SNR+Distortion			
Fin=10kHz, Input =0dB	80 typ.	80 typ.	dB
Fin=100kHz, Input=-20dB	75 typ.	75 typ.	dB; refered to 0dB input
Noise	1.6 typ.	1.6 typ.	LSB; peak-to-peak
SAMPLE-AND-HOLD			
Acquisition Time			
±5V step, to ±0.01%	350 typ.; 800 max.	500 typ.; 900 max.	ns
Aperture Time	20 typ.	20 typ.	ns
Aperture Uncertainty	100 typ.	100 typ.	ps
STABILITY			
Integral Linearity Tempco	2 typ.	2 typ.	ppm/°C
Differential Linearity Tempco	2 typ.	2 typ.	ppm/°C
Offset Error Drift	5 typ.	5 typ.	ppm/°C
Gain Error Drift	25 typ.	25 typ.	ppm/°C
DIGITAL OUTPUTS			
Coding	Straight binary	Straight binary	—
Output Drive	2 typ.	2 typ.	TTL loads
Logic "0"	0.8max.	0.8max.	V
Logic "1"	2.4 min.	2.4 min.	V

Specifications (continued)
(Typical @ 25°C and nominal supply voltages unless otherwise specified)

MODEL	SP9478C	SP9478B	UNITS
POWER SUPPLY REQUIREMENTS			
+15V	45 typ.	45 typ.	mA
-15V	45 typ..	45 typ.	mA
+5V Digital	175 typ.	175 typ.	mA
+5V Analog	85 typ.	85 typ.	mA
-5V Analog	25 typ.	25 typ.	mA
Dissipation	2.75 typ.	2.75 typ.	W
ENVIRONMENTAL			
Operating Temperature	0 to +70	-55 to +125	°C

Using the SP9478

Grounding and Interconnections

Figure 1 shows the interconnection diagram for interfacing the **SP9478** to a microprocessor. The analog and digital grounds must remain separated and as low an impedance as possible. Ideally, the grounds should be tied together directly at the power supplies. Ground plane under the converter is recommended.

Power Supplies

The **SP9478** requires five (5) supply voltages — +15V, -15V, +5V analog, -5V analog and +5V digital. To simplify

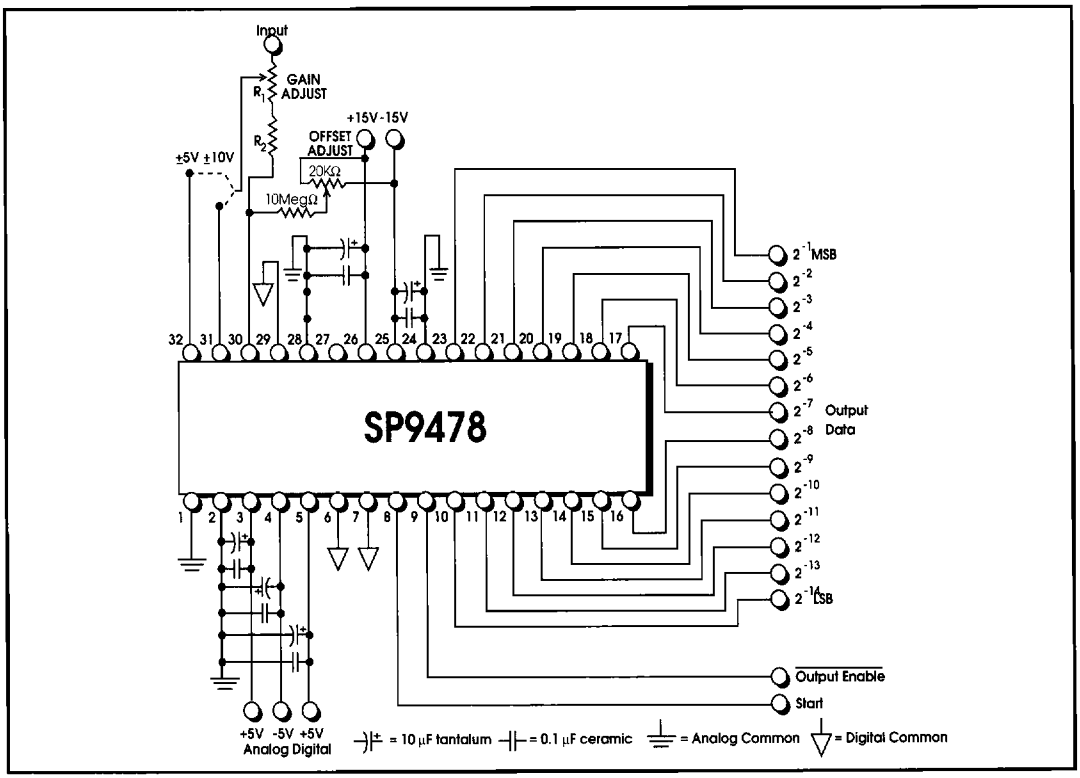

Figure 1. Interconnection

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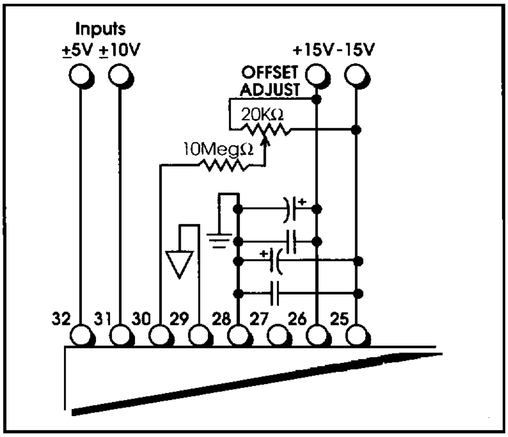


Figure 2. Offset Adjustment

the system requirements, the analog +5V may be supplied by the +5V digital supply, provided the grounding considerations above are maintained.

Input Full Scale Range

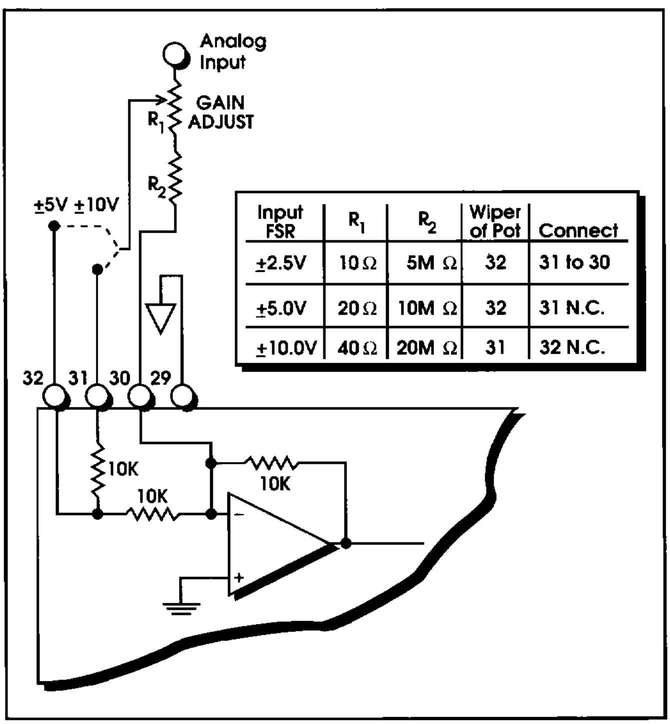
The **SP9478** has provisions for ±10V FS (pin 31) and ±5V FS (pin 32) input ranges. The input signal referenced to analog ground (pin 28) is tied directly to the appropriate input. It is also possible for the **SP9478** to accomdate a ±2.5V FS input range. To do this, pins 30 and 31 are tied together, and the ±2.5V FS input signal is applied to pin 32. Please refer to Figure 3 to see how this affects input impedance.

Offset Adjustment

Figure 2 shows the offset adjust circuit recommended for use with the **SP9478**. The potentiometer should be a 10-turn, 1%, 100ppm or better in order to minimize its contribution to temperature coefficient effects.

Gain Adjustment

Figure 3 shows the gain adjust circuit recommended for use with the **SP9478**. The table included in the Figure provides the appropriate resistor values and interconnections depending on the full scale range used. The resistor and potentiometer should be 1%, 100ppm or better in order to minimize their contribution to temperature coefficient effects.



Input FSR	R_1	R_2	Wiper of Pot	Connect
±2.5V	10Ω	5M Ω	32	31 to 30
±5.0V	20Ω	10M Ω	32	31 N.C.
±10.0V	40Ω	20M Ω	31	32 N.C.

Figure 3. Gain Adjustment

Timing

Figure 4 shows the timing requirements for the **SP9478**. Since all sample-and-hold and converter timing signals are generated internally, only a START command control signal is required. As shown in the figure, this should be a TTL square wave of 60/40 duty cycle to achieve the maximum throughput. It is important to note that the 0.8μs sample and 1.2μs hold/convert times are minimums. The converter throughput cannot be increased by reducing these times. It can be increased by lengthening these times by any arbitrary ratio, as long as

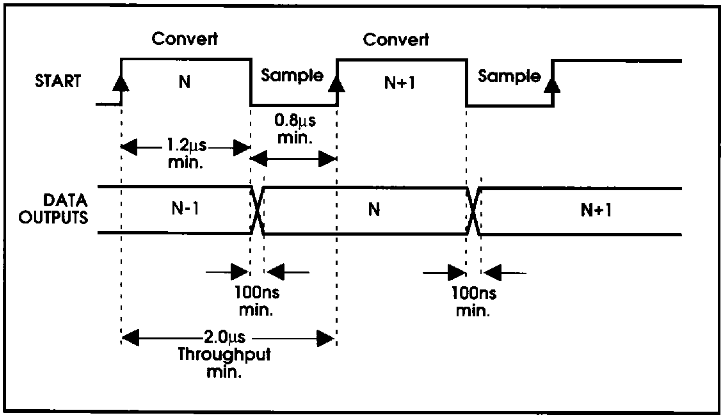


Figure 4. Timing

Performance

Signal to Noise + Distortion

Figure 5 shows a typical dynamic plot of signal-to-noise plus distortion for the **SP9478**. Here SINAD is 79.84dB. The measurement was done with a 10kHz fundamental frequency, at a 312kHz throughput rate.

Linearity Error

Figure 6 contains a typical error plot of the **SP9478**. The linearity error at room temperature is ±0.5 LSB and ±0.6 LSB maximum at the temperature extreme.

Noise Performance

Noise is an important A/D converter parameter which is usually overlooked when specifying high resolution converters. Ideally, when a DC input is applied to an ADC, it should produce only a single output code. Converters with resolutions greater than 12 bits however, tend to produce several adjacent codes in response to a constant DC input. This is due to noise from a variety of sources, both from within and external to the converter.

The number of codes that appear is a measure of the noise resolution of the converter. A good method for measuring the noise resolution is to determine the magnitude of voltage difference at which two different DC voltages can just be resolved. By increasing the difference between the two DC voltage inputs until two distinctive

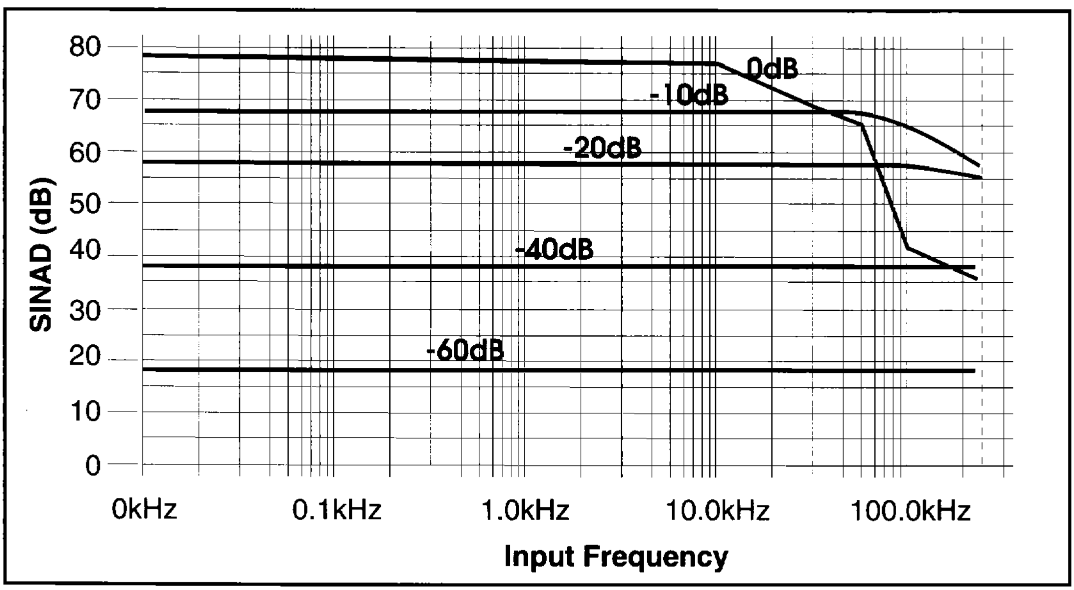


Figure 5. SINAD Plot

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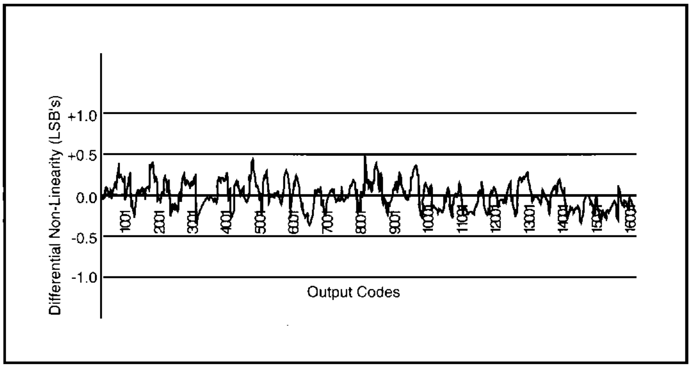


Figure 6. Linearity

ADC. This 8-bit word is converted back to a quantized analog signal by a very fast, 14-bit linear 8-bit DAC. The resultant analog DAC output is subtracted from the analog input held at the output of the S/H. This difference signal is an analog error signal which is a measure of the difference between the analog input and the result of the first 8-bit flash ADC conversion.

codes plus their adjacent noise codes are discernable, the noise resolution of the converter, in millivolts, can be determined. The noise resolution is therefore the number of LSB's of noise in the converte; this then relates to the effective number of bits of the converter.

The four plots shown in Figure 8 show the frequency of codes produced by the SP9478 when the input is two DC voltages 0 (i.e. the same voltage), 1, 2 and 3 millivolts apart. From these plots, the noise resolution of the **SP9478** can be determined to be 1mV, which is the voltage difference at which the two voltages can just be resolved. The 1mV noise resolution translates to 1.6 LSB's, or 0.01% FSR. As a frame of reference, a continuous distribution which approximates the noise functions is fitted to each plot.

The error signal is amplified such that it now spans the full scale range of the flash ADC, and, on the falling edge of the START command, a second 8-bit conversion is performed. The two MSB's of the second 8-bit conversion are used to correct the 8-bit word from the first 8-bit conversion. The six (6) LSB's of the second conversion are added with the corrected 8-bit word from the first conversion. The resultant 14-bit word is the correct digital output, which is latched into the tri-state output latches.

With no START command input, the S/H is normally in the sample mode, and its output follows the input signal applied to the **SP9478**. On the rising edge of the START command, the S/H switches to the hold mode. After a 100ns delay,

Theory of Operation

As shown in Figure 7, the **SP9478** uses a two-pass, digital subranging architecture, comprised of two 8-bit conversions, digitally added to yield the corrected 14-bit digital output. The signal applied to the input of the ADC from the sample-and-hold (S/H) is converted to an 8-bit word by an 8-bit flash

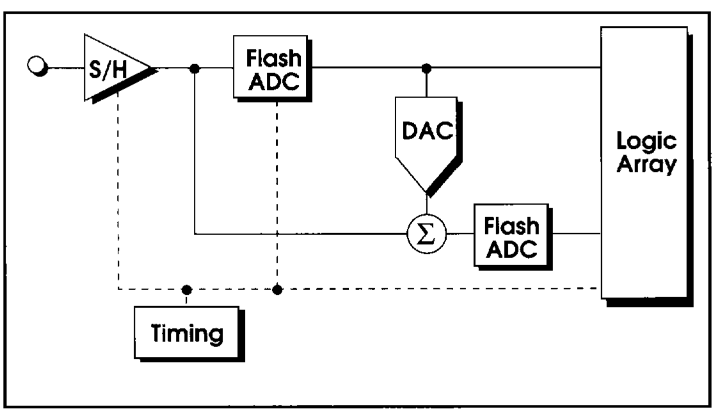


Figure 7. ADC Block Diagram

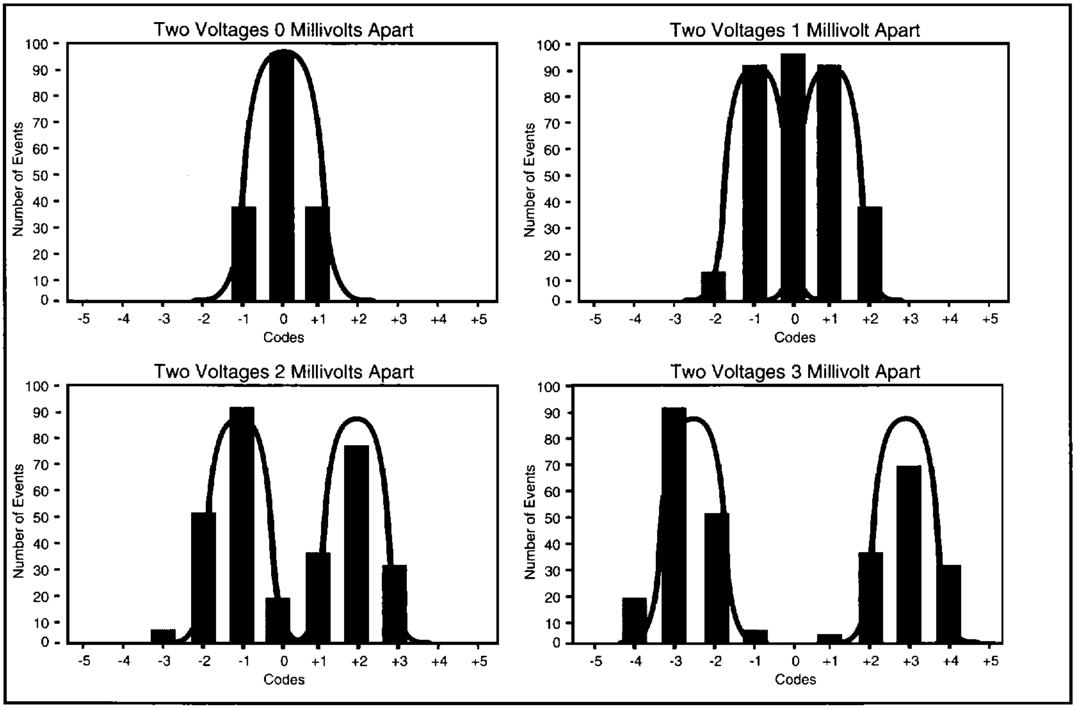
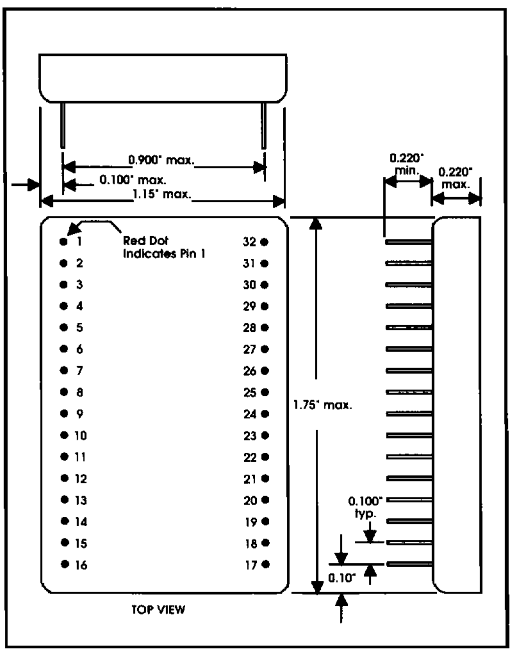


Figure 8. Noise Resolution

Mechanical Dimensions



Pin Assignments

Analog Ground 1.	32. ±5V Input
Analog Ground 2.	31. ±10V Input
+5V Analog 3.	30. Offset Adjust
-5V Analog 4.	29. Digital Ground
+5V Digital 5.	28. Analog Ground
Digital Ground 6.	27. N.C.
Digital Ground 7.	26. +15V
Start 8.	25. -15V
OE 9.	24. Analog Ground
Bit 14 (LSB) 10.	23. Bit 1 (MSB)
Bit 13 11.	22. Bit 2
Bit 12 12.	21. Bit 3
Bit 11 13.	20. Bit 4
Bit 10 14.	19. Bit 5
Bit 9 15.	18. Bit 6
Bit 8 16.	17. Bit 7

Ordering Guide

14-Bit, 500kHz Sampling ADC;

0°C to +70°C **SP9478C**
-55C to +125°C, Mil screened **SP9478B**

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