PLESSEY Semiconductors

ADVANCE INFORMATION CMOS

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MV68SC02

8-BIT MICROPROCESSOR

The MV68SC02 is a monolithic 8-bit microprocessor fabricated with the high density, high speed ISO-CMOS process. It offers all registers and accumulators of the MC6800, **plus** on-chip oscillator and 128 bytes of static RAM located at hexadecimal addresses 0000 to 007F. The device requires only external CMOS ROM program memory (e.g. MV23SC16) to form a micropower microcomputer.

The device is fully software, function and pin-compatible with the MC6802. Operation is quasi-static in that the clock may be interrupted only with the E clock output (pin 37) in the high (logic '1') state. In this condition the low standby power dissipation is realised and all memory and register contents retained.

NB external addressed and enabled memory or peripherals must be static.

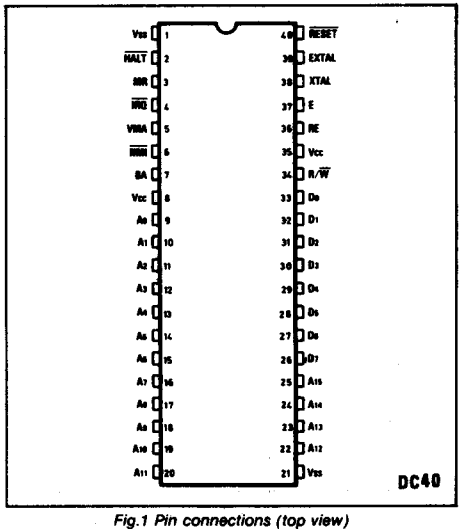

Fig.1 Pin connections (top view)

FEATURES

- Standby Power Dissipation 500µW
- Single Supply
- Operating Voltage Range 3V to 7V
- Standby Voltage Range 2V to 7V
- Software Compatible with MC6800
- Software, Function and Pin - Compatible with MC6802
- 128-Byte Static RAM and Oscillator On-Chip
- Operation DC to 2MHz (8MHz crystal)
- Operating Power Dissipation 75mW at 2MHz
- Fully TTL-Compatible
- All Memory and Registers Retainable in Standby Mode
- 16-bit Memory Addressing up to 65K Words
- Supplied in 40-pin Sidebrazed DIL (DC) package

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

Parameter	Symbol	Limit	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_I	-0.3 to V_{CC} + 0.3	V
Output current	I_O	±20	mA
Storage temperature	T_S	-65 to 150	°C
Operating temperature	T_{amb}	-40 to 85	°C
Power dissipation	P	450	mW

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{CC}	3	5	7	V
High level, output current	I_{OH}		-10		mA
Low level, output current	I_{OL}		10		mA
Operating temperature	T_{amb}	0		70	°C

Note 1. Voltages are with respect to Vss

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = +4.75V to +5.25V

Characteristic	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Operating supply voltage range	V_{CC}	3.0	5.0	7.0	V	
Standby supply voltage range	V_{CC}	2.0		7.0	V	
Standby supply current	I_{CCS}		100		µA	E = V_{OH}, V_{IN} = V_{SS} or V_{CC} EXTAL = V_{SS} or V_{CC}
Operating supply current	I_{CC}		15		mA	f = 2MHz
			3		mA	f = 1MHz
			300		µA	f = 100kHz
Read/Write protect threshold (RE - pin 36)			2.0		V	
Input high level voltage (except $\overline{RESET}$)	V_{IH}	2.0			V	
Input high level voltage $\overline{RESET}$	V_{IH}	4.0			V	
Input low level voltage	V_{IL}			0.8	V	
Input leakage current	I_L	-10		10	µA	V_{IN} = V_{SS} to V_{CC}, Note 3
Output high level voltage						
D0-D7, E	V_{OH}	2.4			V	I_{OH} = -205uA
A0-A15,R/$\overline{W}$,VMA	V_{OH}	2.4			V	I_{OH} = -145uA
BA	V_{OH}	2.4			V	I_{OH} = -100uA
Output low level voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input capacitance D0-D7	C_{IN}		10		pF	V_{IN} = 0V, f = 1MHz
Logic inputs, EXTAL	C_{IN}		6		pF	
Output capacitance A0-A15, R/$\overline{W}$, VMA	C_{OUT}		10		pF	
Frequency of operation (EXTAL Clock ÷ 4)	f	0		2.0	MHz	f = 1/t_{CYC}
Crystal frequency	f_{XTAL}	0.20		8.0	MHz	
Clock cycle time	t_{CYC}	500			ns	Fig. 2 and Fig. 3
Clock pulse width	t_{ELO}	0.25		10	µs	Fig. 2 and Fig. 3
Instruction cycle time			2		µs	f = 2MHz
EXTAL clock rise and fall time	t_{OC}			25	ns	measured between 0.8V and 2.0V

Note 2. All Typical values at T_{amb} = 25°C, V_{CC} = 5V.
Note 3. Excluding EXTAL & XTAL

SWITCHING CHARACTERISTICS(FIG.2 and FIG.3)

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = +4.75V to +5.25V, load circuit of Fig. 4

Characteristic	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Address delay	t_{AD}			160	ns	
Peripheral Read access time t_{acc} = t_{CYC} - (t_f + t_{AD} + t_{DSR})	t_{acc}			250	ns	t_{CYC} = 500ns
Data setup time (Read)	t_{DSR}	40			ns	
Input Data hold time	t_H	10			ns	
Output Data hold time	t_H	10			ns	
Address hold time (Address, R/$\overline{W}$, VMA)	t_{AH}	10			ns	
Data delay time (Write)	t_{DDW}			160	ns	
Processor controls						
Bus available delay	t_{BA}			135	ns	
Processor control setup time	t_{PCS}	125			ns	
Processor control rise and fall time	t_{PCr},t_{PCf}			100	ns	measured between 0.8V and 2.0V
Output rise and fall times	t_r,t_f			50	ns	measured between 0.4V and 2.4V

Note 4. 'Measured between 0.8V and 2.0V' applies only to t_{PCr} and t_{PCf}.

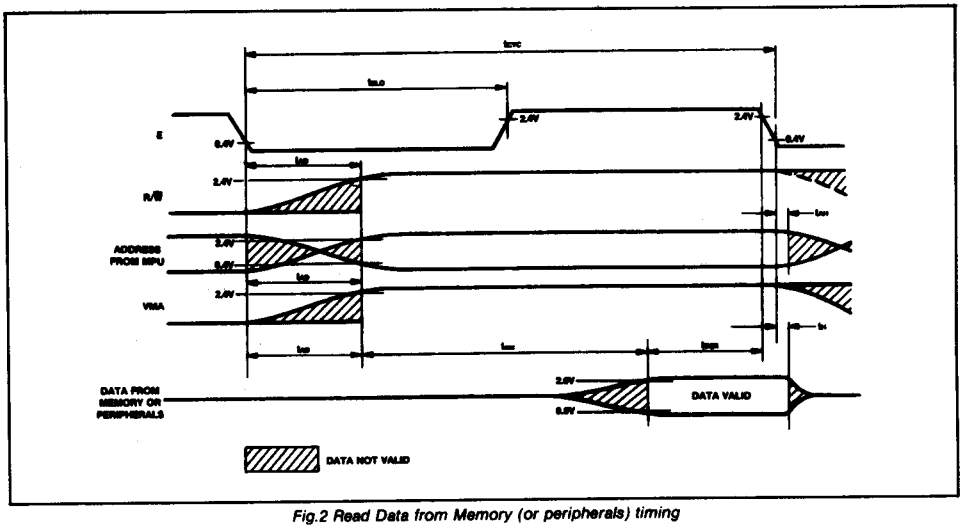

Fig.2 Read Data from Memory (or peripherals) timing

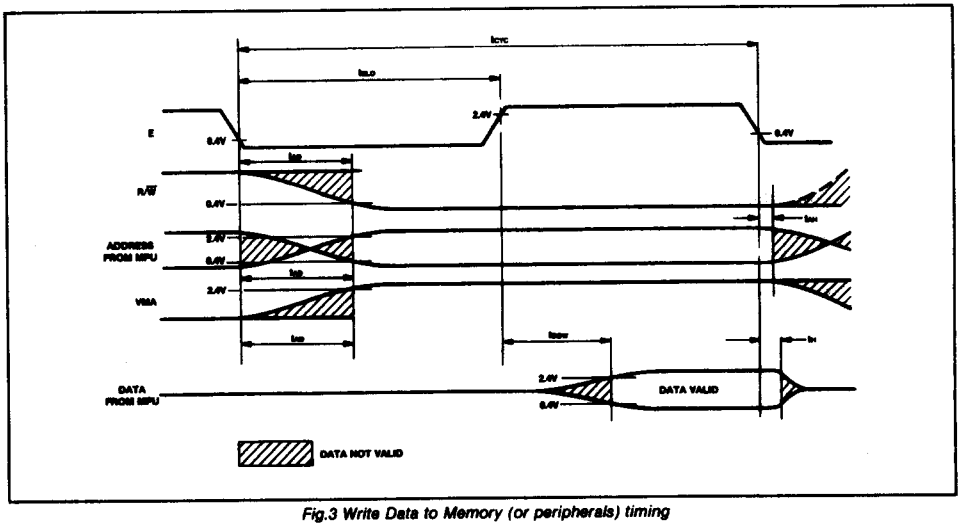

Fig.3 Write Data to Memory (or peripherals) timing

C = 130pF for D0-D7, E
= 90pF for A0-A15, R/W, and VMA
= 30pF for BA
R = 11.7kohms for D0-D7, E
= 16.5kohms for A0-A15, R/W and VMA
= 24kohms for BA

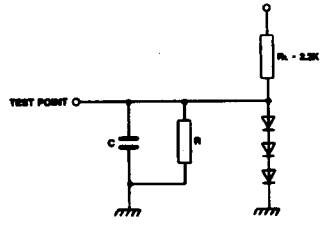

Fig.4 Load circuit for Address, Data, E, R/W, VMA and BA

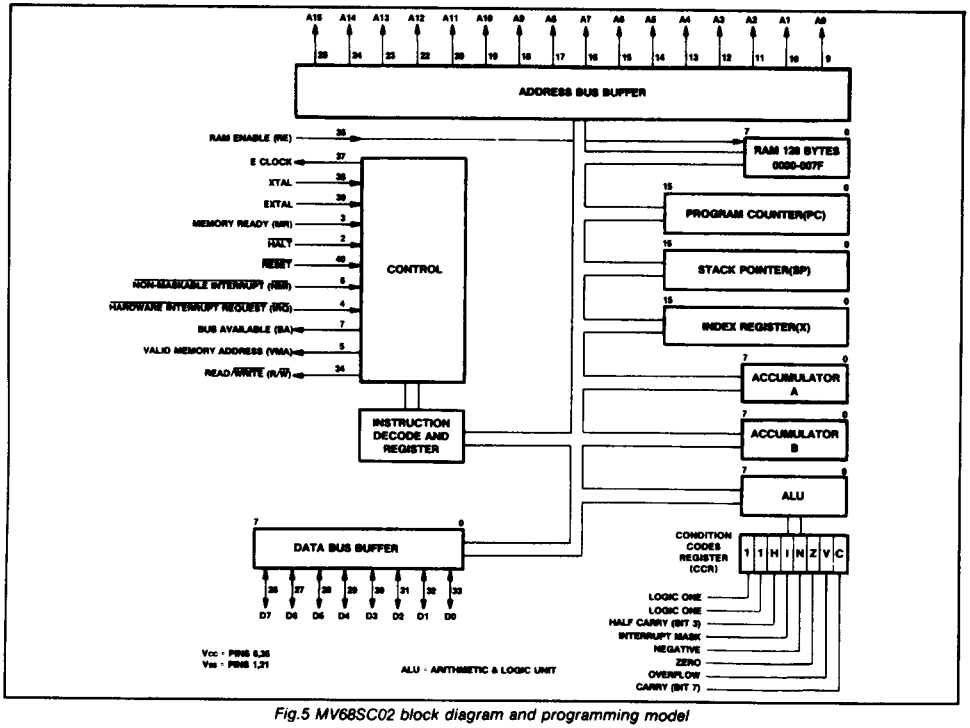

Fig.5 MV68SC02 block diagram and programming model

MV68SC02 SIGNAL DESCRIPTION

Proper operation of the MV68SC02 microprocessor requires that certain timing and control signals be provided and that other control signals be monitored to determine the state of the processor. The following is a summary of the 36 processor signals, (refer Block Diagram Fig. 5).

Address Bus (A0-A15) Sixteen pins each connected to a three-state bus driver capable of driving one standard TTL load and 90pF.

Data Bus (D0-D7) Eight pins each connected to a three-state bidirectional bus driver capable of driving one standard TTL load and 130pF.

Read/Write (R/$\overline{W}$) This output indicates to memory (or peripheral) devices that the processor is in a Read (high or Logic '1') or Write (low or Logic '0') state. The normal state of this signal, including when the processor is halted or waiting for an interrupt following a WAI instruction, is high. This output is capable of driving one standard TTL load and 90pF.

Valid Memory Address (VMA) This output indicates to memory (or peripheral) devices that there is a valid address at the address outputs, and is capable of driving one standard TTL load and 90pF. When the processor is halted, or following a WAI instruction, this signal is low ('0' state).

Bus Available (BA) This output indicates that the processor has stopped and the address and data buses are available, e.g.when halted or following a WAI instruction. This output is capable of driving one standard TTL load and 30pF.

E Clock (E) This output is equivalent to $\phi 2$ on the MC6800 and is a single phase clock to the memory (or peripheral) devices capable of driving one standard TTL load and 130pF.

EXTAL and XTAL These two connections are for a parallel resonance fundamental crystal of AT cut and frequency four times the desired operating frequency. Alternatively EXTAL may be driven from an external TTL source with XTAL left open circuit. (In either case, the t_{ELO} limits must be met.) The low to high transition at EXTAL clocks the internal divide by four and EXTAL may be stopped with E high to perform single cycle execution.

Memory Ready (MR) This TTL-compatible input signal allows stretching of any positive half-cycle of E (for interfacing with slow memories) when taken low immediately after the commencement of that half-cycle.

$\overline{HALT}$ This TTL-compatible input signal allows processor operation to be halted or single-instruction stepped. $\overline{HALT}$ transitions should occur t_{HCS} before the rising edge of E. When taken low the processor will stop at the end of the current instruction, with BA and R/$\overline{W}$ high, VMA low and the Address and Data outputs in their high impedance state. If then $\overline{HALT}$ is returned high for just one E clock cycle, the processor will execute its next instruction and stop again. Interrupts $\overline{NMI}$ and $\overline{IRQ}$, provided their pulse width exceeds t_{CYC}, will be latched if received whilst halted, and acted upon one instruction after resumption.

$\overline{RESET}$ This input is used to reset and start the processor from a power down condition, or to reinitialise the processor at any time. At power-up, $\overline{RESET}$ must be held low for a minimum of 8 E clock cycles, or 20ms, whichever is the greater. When reinitialising, $\overline{RESET}$ must be low for a minimum of 3 E clock cycles. Once these conditions have been satisified, whilst $\overline{RESET}$ remains low VMA and BA will be low with R/$\overline{W}$ high and the Data outputs in their high impedance state. The Address outputs will be set to the first Reset Vector Address FFFE, and the internal registers cleared.

When $\overline{RESET}$ is returned high, the contents of both FFFE and the second reset vector FFFF are loaded to the Program

Counter to effect indirect addressing to the programmer's initialisation routine, and the Interrupt Mask (CCR Bit 4) is set. (This bit must then be cleared under program control before the processor can be interrupted by $\overline{IRQ}$.)

Hardware Interrupt Request ($\overline{IRQ}$) This TTL-compatible input requests that an interrupt sequence be generated within the processor, which will complete the current instruction before recognising the request, and then only begin an interrupt sequence if the interrupt mask (CCR Bit 4) is clear. The interrupt sequence comprises 12 E clock cycles in which the program counter, index register, accumulators and condition code register are stacked, the interrupt mask is set, and the program counter loaded from IRQ vectors FFF8 and FFF9. The processor will thus branch to the programmer's IRQ servicing routine, which will usually conclude with an RTI instruction to unstack the interrupted program's parameters and effect resumption of that program.

Non-Maskable Interrupt ($\overline{NMI}$) This TTL-compatible input also requests that an interrupt sequence be generated within the processor, but is not subject to the interrupt mask. An interrupt sequence commences at the end of the current instruction, stacking the registers then setting the interrupt mask. In the 11th and 12th cycles the program counter is loaded from NMI vectors FFFC and FFFD.

Both $\overline{IRQ}$ and $\overline{NMI}$ inputs are sampled whilst E clock is high, and provided that t_{PCS} is met, will start their interrupt sequence when E falls at the end of the current instruction. When $\overline{IRQ}$ or $\overline{NMI}$ inputs are answering a WAI instruction, the interrupt sequence is only 4 cycles. Both inputs can accept pulse widths down to t_{CYC}, but if both occur together, or if $\overline{NMI}$ is received just before an $\overline{IRQ}$-initiated sequence reaches its vector cycles (11th and 12th cycles), vectors FFFC and FFFD will be accessed because $\overline{NMI}$ is given priority. In such an event a pulsed $\overline{IRQ}$ input will be lost because the interrupt mask will now be set.

RAM Enable (RE) This TTL-compatible input disables the internal RAM when taken low. This is necessary when external memory between addresses 0000 and 007F is to be accessed since the data bus is fixed in output mode when accessing the internal memory.

MV68SC02 INSTRUCTION SET

The MV68SC02 has a set of 72 instructions, listed alphabetically in Table 1. These instructions are executed in six different address modes - implied (inherent), immediate, direct, extended, indexed and relative. Of the 256 possible 8-bit operation codes, 197 are assigned. The instruction set is as for the MC6800/MC6802. Plessey Semiconductors' MV68SC02 Microprocessor Handbook* includes full details of the address modes, instruction descriptions, execution times and cycle by cycle operation summaries.

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

Table 1 Instruction set - alphabetical listing

*Available last quarter 1981