

M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMs with EDO(Extended Data Out : Hyper Page) mode function, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417805DXX-5,5S	50	13	25	13	90	655
M5M417805DXX-6,6S	60	15	30	15	110	540
M5M417805DXX-7,7S	70	20	35	20	130	475

XX=J,TP

- Standard 28 pin SOJ,28 pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
 - 2.75mW (Max) ----- CMOS Input level
 - 1.10mW (Max)* ----- CMOS Input level
- Operating power dissipation
 - M5M417805Dxx- 5,5S ----- 800mW (Max)
 - M5M417805Dxx- 6,6S ----- 660mW (Max)
 - M5M417805Dxx- 7,7S ----- 580mW (Max)
- Self refresh capability*
 - Self refresh current ----- 200µA(Max)
- EDO mode (1024-column random access), Read-modify- write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities.
- Early-write mode, \overline{OE} and \overline{W} to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A0 ~A10)
 - *:Applicable to self refresh version(M5M417805DJ, TP -5S, -6S,-7S :option) only

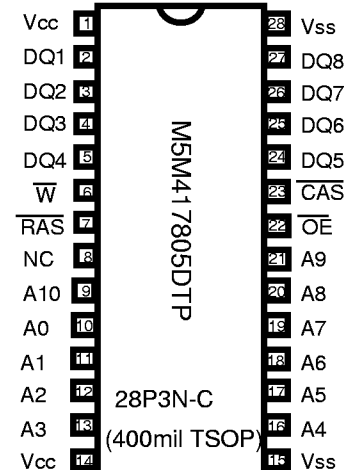
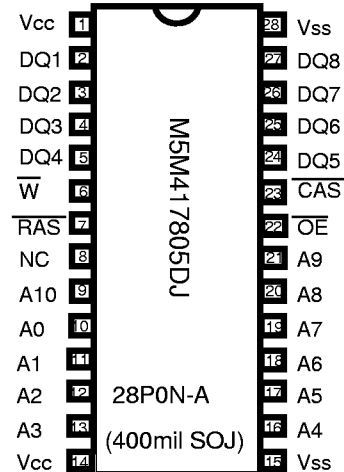
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT,

PIN DESCRIPTION

Pin Name	Function
A0~A10	Address Inputs
DQ1~DQ8	Data Inputs / Outputs
RAS	Row Address Strobe Input
CAS	Column Address Strobe Input
\overline{W}	Write Control Input
\overline{OE}	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

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FUNCTION

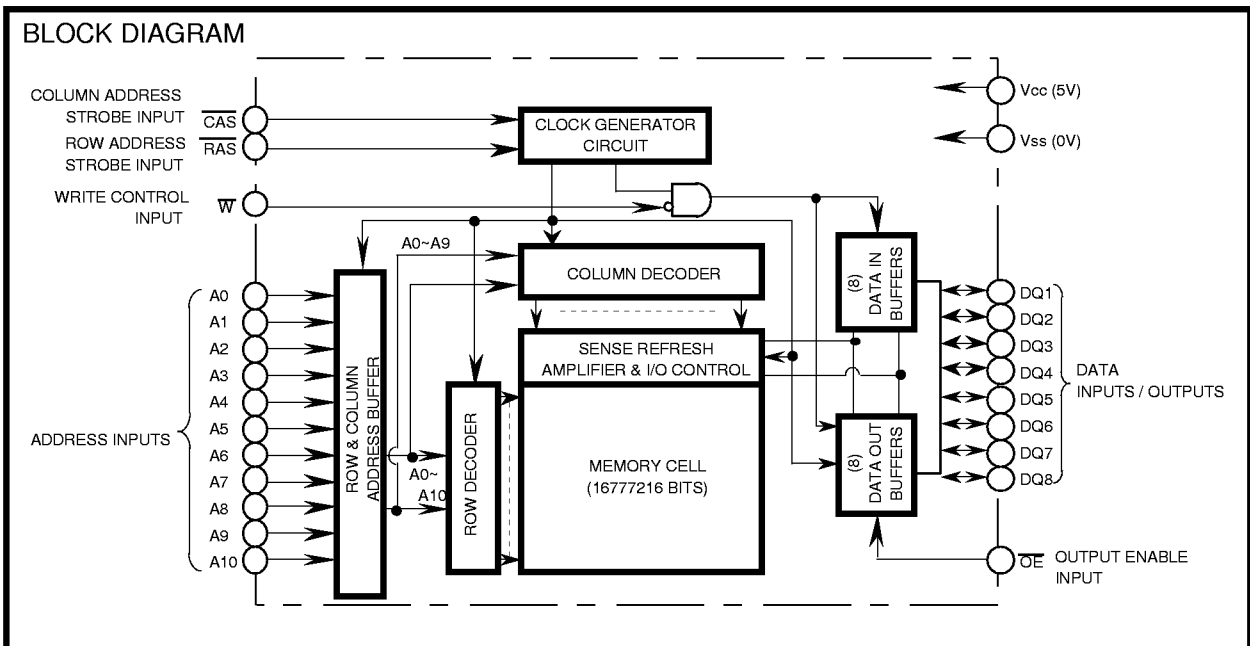
In addition to normal read, write and read-modify-write operations ,the M5M417805DJ, TP provide a number of other functions,e.g.,EDO Mode,RAS-only refresh,and delayed-write.

The input condition and output state for each mode are shown in Table 1.

Table 1 Input condition and Output state for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	EDO mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid,APD : applied, OPN : open



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to V _{ss}	-1 ~ 7	V
V _I	Input voltage		-1 ~ 7	V
V _O	Output voltage		-1 ~ 7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25 °C	1000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

(T_a=0 ~ 70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{cc}	Supply voltage	4.5	5.0	5.5	V
V _{ss}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		5.5	V
V _{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to V_{ss}** : V_{IL}(Min) is -2.0V when undershoot width is less than 25ns. (The width is defined as the period when the voltage level is below V_{ss}.)ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70 °C, V_{cc}= 5V ± 10%, V_{ss}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} = -5mA	2.4		V _{cc}	V
V _{OL}	Low-level output voltage	I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating, 0V ≤ V _{OUT} ≤ 5.5V	-10		10	μA
I _I	Input current	0V ≤ V _{IN} ≤ +5.5V, Other inputs pins=0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{cc} operating (Note 3,4,5)	M5M417805D-5,5S	R _{AS} , C _{AS} cycling t _{RC} =t _{WC} =min. output open		145	mA
		M5M417805D-6,6S			120	
		M5M417805D-7,7S			105	
I _{CC2}	Supply current from V _{cc} , stand-by (Note 6)	R _{AS} =C _{AS} =V _{IH} , output open		2	mA	
		R _{AS} =C _{AS} ≥ V _{cc} -0.2V, output open		0.5		
I _{CC3} (AV)	Average supply current from V _{cc} , R _{AS} only refresh mode (Note 3,5)	M5M417805D-5,5S	R _{AS} cycling, C _{AS} =V _{IH} t _{RC} =min. output open		145	mA
		M5M417805D-6,6S			120	
		M5M417805D-7,7S			105	
I _{CC4} (AV)	Average supply current from V _{cc} EDO Mode (Note 3,4,5)	M5M417805D-5,5S	R _{AS} =V _{IL} , C _{AS} cycling t _{HPC} =min. output open		140	mA
		M5M417805D-6,6S			115	
		M5M417805D-7,7S			90	
I _{CC6} (AV)	Average supply current from V _{cc} C _{AS} before R _{AS} refresh mode (Note 3,5)	M5M417805D-5,5S	C _{AS} before R _{AS} refresh cycling t _{RC} =min. output open		145	mA
		M5M417805D-6,6S			120	
		M5M417805D-7,7S			105	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.5: Under condition that column address is changed not more than once while R_{AS}=V_{IL} and C_{AS}=V_{IH}.CAPACITANCE (T_a=0 ~ 70 °C, V_{cc} = 5V ± 10%, V_{ss}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _I =V _{ss}			5	pF
C _{I(CLK)}	Input capacitance, clock inputs	f=1MHz			7	pF
C _{I/O}	Input/Output capacitance, data ports	V _I =25mVrms			7	pF

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SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C , Vcc = 5V ± 10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t _{CAC}	Access time from $\overline{\text{CAS}}$ (Note 7,8)		13		15		20	ns
t _{RAC}	Access time from $\overline{\text{RAS}}$ (Note 7,9)		50		60		70	ns
t _{AA}	Column address access time (Note 7,10)		25		30		35	ns
t _{CPA}	Access time from CAS precharge (Note 7,11)		30		35		40	ns
t _{OE}	Access time from OE (Note 7)		13		15		20	ns
t _{OHC}	Output hold time from CAS high (Note 13)	5		5		5		ns
t _{OHR}	Output hold time from RAS high (Note 13)	5		5		5		ns
t _{CLZ}	Output low impedance time from CAS low (Note 7)	5		5		5		ns
t _{OEZ}	Output disable time after OE high (Note 12)		13		15		20	ns
t _{WEZ}	Output disable time after $\overline{\text{WE}}$ low (Note 12)		13		15		20	ns
t _{OFF}	Output disable time after CAS high (Note 12,13)		13		15		20	ns
t _{REZ}	Output disable time after RAS high (Note 12,13)		13		15		20	ns
t _{DOH}	Output hold time from CAS low	5		5		5		ns

Note 6: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization $\overline{\text{RAS}}$ cycles. The initialization cycles should be done either by $\overline{\text{RAS}}$ -Only refresh cycles or by CAS-before- $\overline{\text{RAS}}$ refresh cycles only.

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

After the initialization cycles, $\overline{\text{RAS}}$ should be kept either higher than V_{IHmin} or lower than V_{ILmax} except $\overline{\text{RAS}}$ transition time.

7: Measured with a load circuit equivalent to 100pF.

The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{out} \leq I \pm 10 \mu A$) with no reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ go to high.

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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and EDO Mode Cycles)

(Ta=0 ~ 70 °C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		32		32		32	ms
tREF*	Refresh cycle time		128		128		128	ms
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note16)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	5		5		5		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	8		10		13		ns
tRAD	Column address delay time from RAS low (Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	8		10		10		ns
tDZC	Delay time, data to CAS low (Note19)	0		0		0		ns
tDZO	Delay time, data to OE low (Note19)	0		0		0		ns
tRDD	Delay time, RAS high to data	13		15		20		ns
tCDD	Delay time, CAS high to data	13		15		20		ns
tODD	Delay time, OE high to data	13		15		20		ns
tWED	Delay time, W low to data	13		15		20		ns
tT	Transition time (Note20)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed $t_T = 2ns$.15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.16: $t_{RCD(max)}$ is specified as a reference value only to guarantee the valid operation. If t_{RCD} is less than $t_{RCD(max)}$, access time is controlled by t_{RAC} . If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled by t_{CAC} or t_{AA} .17: $t_{RAD(max)}$ is specified as a reference value only to guarantee the valid operation. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled by t_{AA} .18: $t_{ASC(max)}$ is specified as a reference value only to guarantee the valid operation. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled by t_{CAC} .19: Either t_{DZC} or t_{DZO} must be satisfied.20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.**Read and Refresh Cycles**

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tRCS	Read Setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 21)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 21)	0		0		0		ns
tRAL	Column address to RAS hold time	25		30		35		ns
tCAL	Column address to CAS hold time	15		18		20		ns
tORH	RAS hold time after OE low	13		15		20		ns
tOCH	CAS hold time after OE low	13		15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t _{WC}	Write cycle time	90		110		130		ns
t _{RAS}	RAS low pulse width	50	10000	60	10000	70	10000	ns
t _{CAS}	CAS low pulse width	8	10000	10	10000	13	10000	ns
t _{CSH}	CAS hold time after RAS low	40		48		55		ns
t _{RSH}	RAS hold time after CAS low	13		15		20		ns
t _{WCS}	Write setup time before CAS low (Note 23)	0		0		0		ns
t _{WCH}	Write hold time after CAS low	8		10		13		ns
t _{CWL}	CAS hold time after \bar{W} low	8		10		13		ns
t _{RWL}	RAS hold time after \bar{W} low	8		10		13		ns
t _{WP}	Write pulse width	8		10		13		ns
t _{DS}	Data setup time before CAS low or \bar{W} low	0		0		0		ns
t _{DH}	Data hold time after CAS low or \bar{W} low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t _{RWC}	Read write/read modify write cycle time (Note22)	109		133		161		ns
t _{RAS}	RAS low pulse width	75	10000	89	10000	107	10000	ns
t _{CAS}	CAS low pulse width	38	10000	44	10000	57	10000	ns
t _{CSH}	CAS hold time after RAS low	70		82		99		ns
t _{RSH}	RAS hold time after CAS low	38		44		57		ns
t _{RCS}	Read setup time before CAS low	0		0		0		ns
t _{CWD}	Delay time, CAS low to \bar{W} low (Note23)	28		32		42		ns
t _{RWD}	Delay time, RAS low to \bar{W} low (Note23)	65		77		92		ns
t _{AWD}	Delay time, address to \bar{W} low (Note23)	40		47		57		ns
t _{OEH}	\bar{OE} hold time after \bar{W} low	13		15		20		ns

Note 22: t_{RWC} is defined $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_r$.

23: t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference values only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for EDO mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. Under conditions other than those specified above (for delayed write) of the DQ output (at access time and until CAS or OE goes back to V_{IH}) is invalid.

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EDO Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle,
Read Write Mix Cycle, Hi-Z control by \overline{OE} or \overline{W}) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	EDO mode read/write cycle time (Note25)	20		25		30		ns
tHPRWC	EDO Mode read write / read modify write cycle time	57		66		79		ns
tRAS	RAS low pulse width for read or write cycle (Note26)	65	100000	77	100000	92	100000	ns
tCP	CAS high pulse width (Note27)	8	13	10	16	13	16	ns
tCPRH	RAS hold time after CAS precharge	28		33		38		ns
tCPWD	Delay time, \overline{CAS} precharge to \overline{W} low (Note23)	43		50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until CAS access	7		7		7		ns
tOEPE	OE Pulse Width (Hi-Z control)	7		7		7		ns
tWPE	\overline{W} Pulse Width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, CAS low to \overline{W} low after read	28		32		42		ns
tHAWD	Delay time, Address to \overline{W} low after read	40		47		57		ns
tHPWD	Delay time, CAS precharge to \overline{W} low after read	43		50		60		ns
tHCOD	Delay time, CAS low to OE high after read	13		15		20		ns
tHAOD	Delay time, Address to OE high after read	25		30		35		ns
tHPOD	Delay time, CAS precharge to OE high after read	28		33		38		ns

Note 24: For those timing requirements which are not listed above parameters of cycles are applicable.

25: tHPC(min) is specified in the case of read-only and early write-only in EDO Mode.

26: tRAS(min) is specified as two cycles of \overline{CAS} input are performed. It is defined as tRAS(min)=tCSH(min)+tPC(min)

27: tCP(max) is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 28)

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	5		5		5		ns
tCHR	CAS hold time after RAS low	10		10		15		ns
tCAS	CAS low pulse width	17		17		22		ns
tRSR	Read setup time before RAS low	5		5		5		ns
tRHR	Read hold time after RAS low	10		10		15		ns

Note 28: Eight or more \overline{CAS} before \overline{RAS} cycles instead of eight RAS cycles are necessary for proper operation of CAS before \overline{RAS} refresh mode.**Hidden Refresh Cycle** (Note 30)

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRSR	Read setup time before RAS low	5		5		5		ns
tRHR	Read hold time after RAS low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases tRSR and tRHR should be satisfied.

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SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70 °C , Vcc=5V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I _{CC8} (AV)	Average supply current from Vcc Slow - Refresh cycle (note 6)	M5M417805D (S) CAS before RAS refresh cycling ,or, RAS cycling & CAS ≤ 0.2V OE&W ≤ 0.2V ,or, OE&W ≥ Vcc- 0.2V A0 ~ A10 ≥ 0.2V ,or, A0 ~ A10 ≥ Vcc- 0.2V tREF =128mS (2048cycles) output = OPEN tRAS=tRASmin. ~ 1μs			500	μA
I _{CC9} (AV)*	Average supply current from Vcc Self - Refresh cycle (note 6)	M5M417805D (S) RAS = CAS ≤ 0.2V output = OPEN			200	μA

TIMING REQUIREMENTS (Ta=0 ~ 70 °C , Vcc=5V ± 10%, Vss=0V, unless otherwise noted) (Noted 14,15)

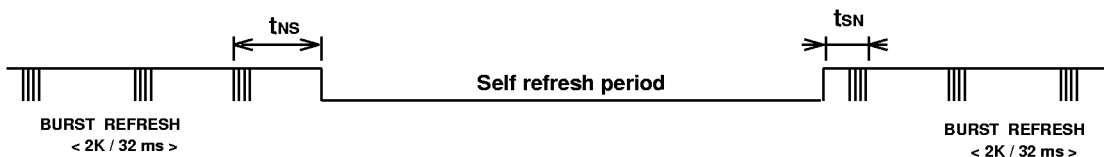
Symbol	Parameter	Limits						Unit
		M5M417805D-5S		M5M417805D-6S		M5M417805D-7S		
		Min	Max	Min	Max	Min	Max	
t _{RASS}	Self Refresh RAS low pulse width	100		100		100		μs
t _{RPS}	Self Refresh RAS high precharge time	90		110		130		ns
t _{CHS}	Self Refresh RAS hold time	- 50		- 50		- 50		ns
t _{RSR}	Read setup time before RAS low	10		10		10		ns
t _{RHR}	Read hold time after RAS low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS**(1) In the case of distributed refresh**

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} ≤ 32 ms and t_{SN} ≤ 32 ms.

**(2) In the case of burst refresh**

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} + t_{SN} ≤ 32 ms.



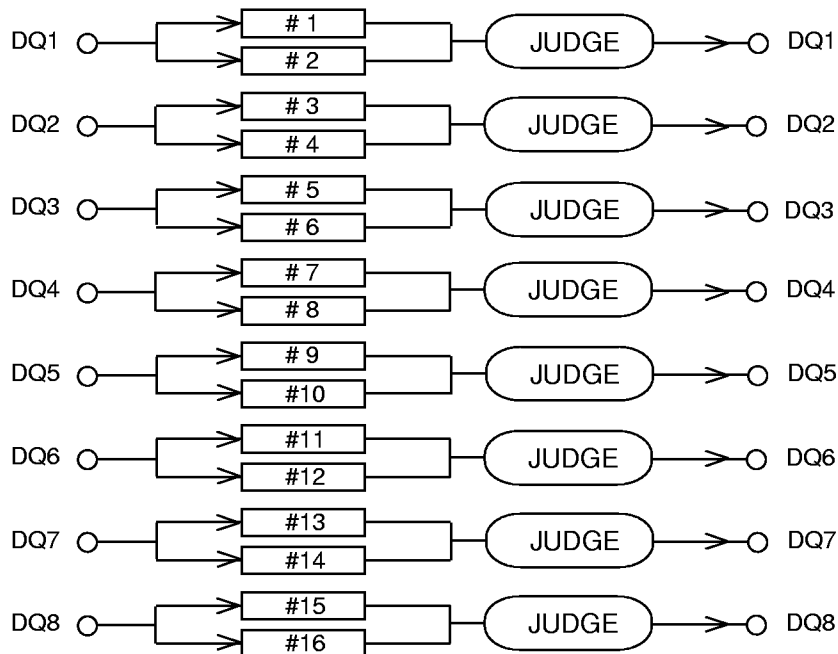
M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

TEST Mode SET Cycle (Note 31)

Symbol	Parameter	Limits						Unit
		M5M417805D-5,-5S		M5M417805D-6,-6S		M5M417805D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	W setup time before RAS low	10		10		10		ns
tWHR	W hold time after RAS low	10		10		15		ns

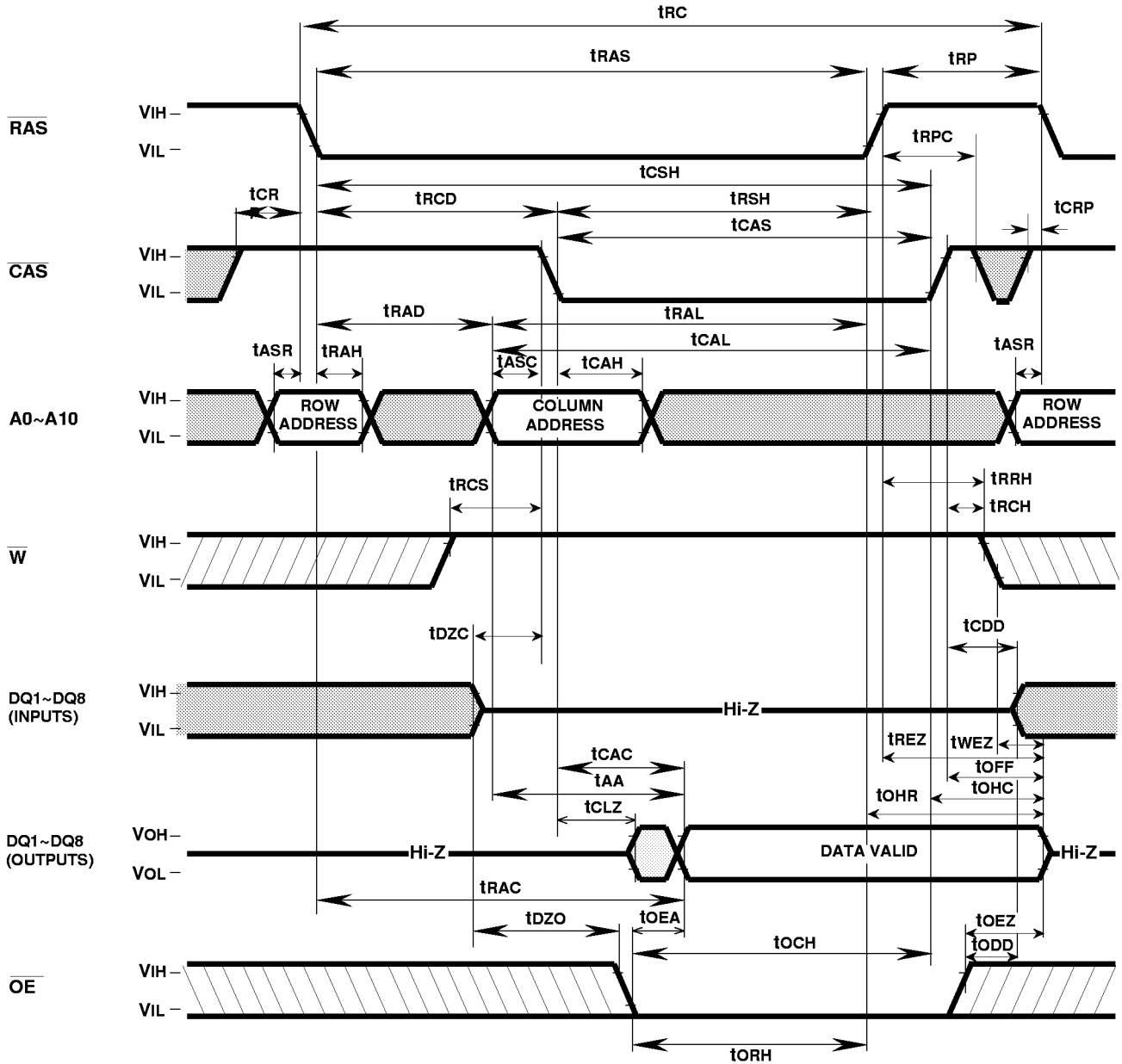
Note 31 : The test mode function is initiated by a \overline{W} and \overline{CAS} before \overline{RAS} cycle (WCBR cycle) as specified in timing diagram. The test mode function is terminated by either a \overline{CAS} before \overline{RAS} refresh cycle (CBR refresh cycle) or a \overline{RAS} only refresh cycle. During the test mode, the device is internally organized as 16 bits wide (1M bytes depth). Address of CA0,CA1 is no required. During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2 bits, respectively. High state indicates that they are same. Low state indicates that they are not same. These high and low outputs are used to determine Pass and Fail respectively. During the test mode operation, only WCBR cycle can be used to perform refresh.



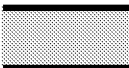
M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S


EDO (HYPER PAGE) MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

Timing Diagrams (Note 29) Read Cycle



Note 29

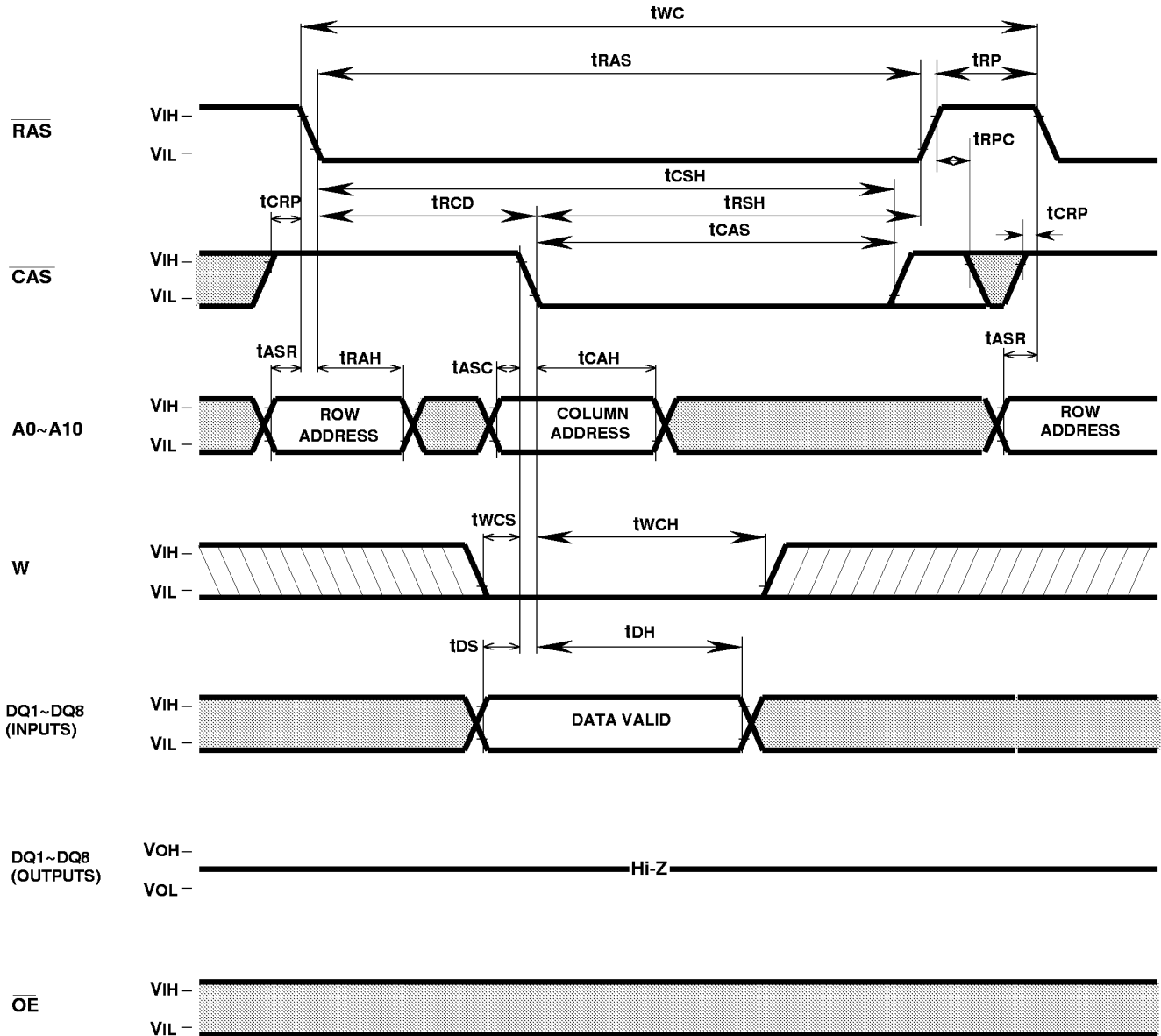
 Indicates the don't care input.
 $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$ or $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$

 Indicates the invalid output.

M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

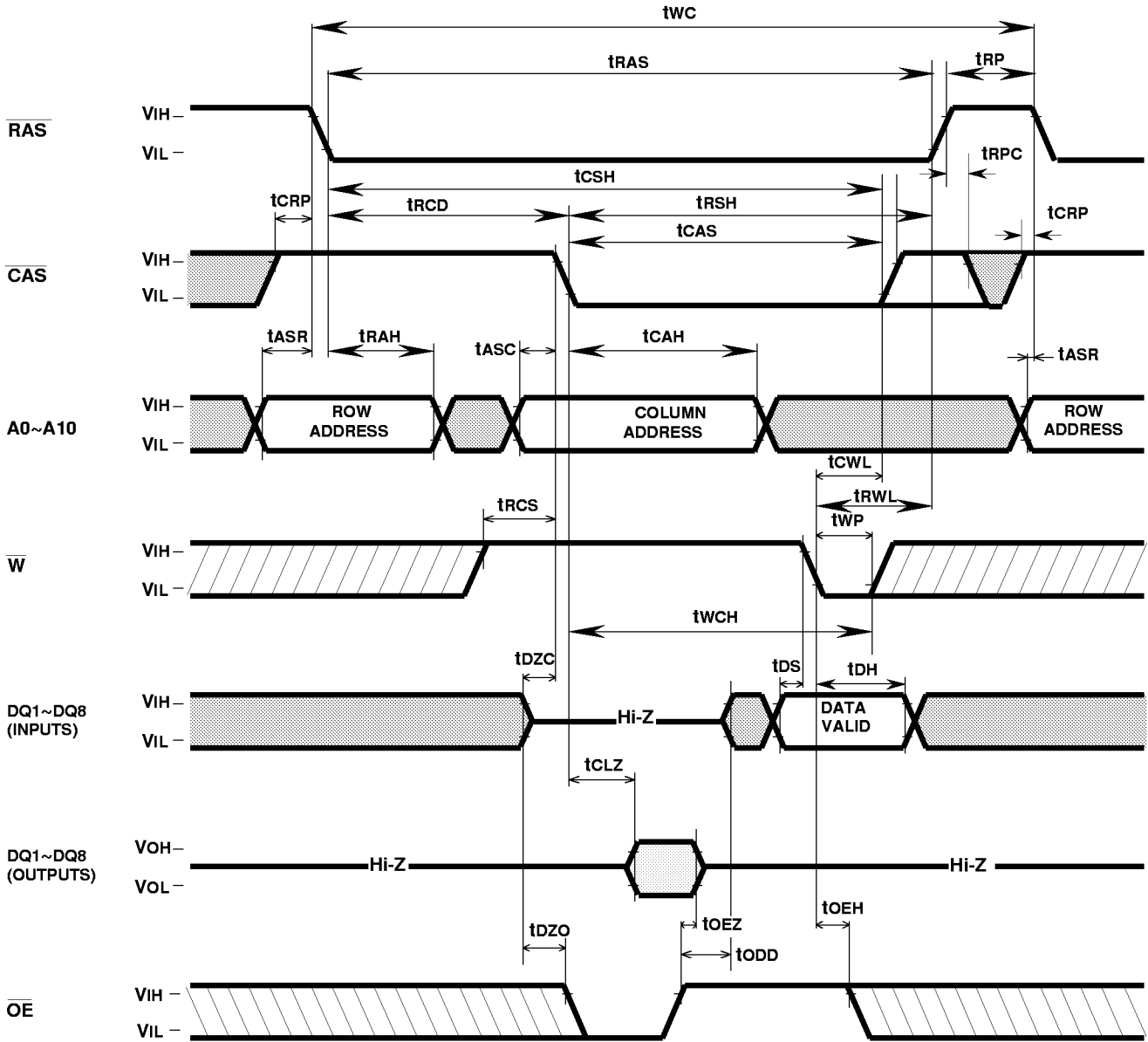
Early Write Cycle



M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

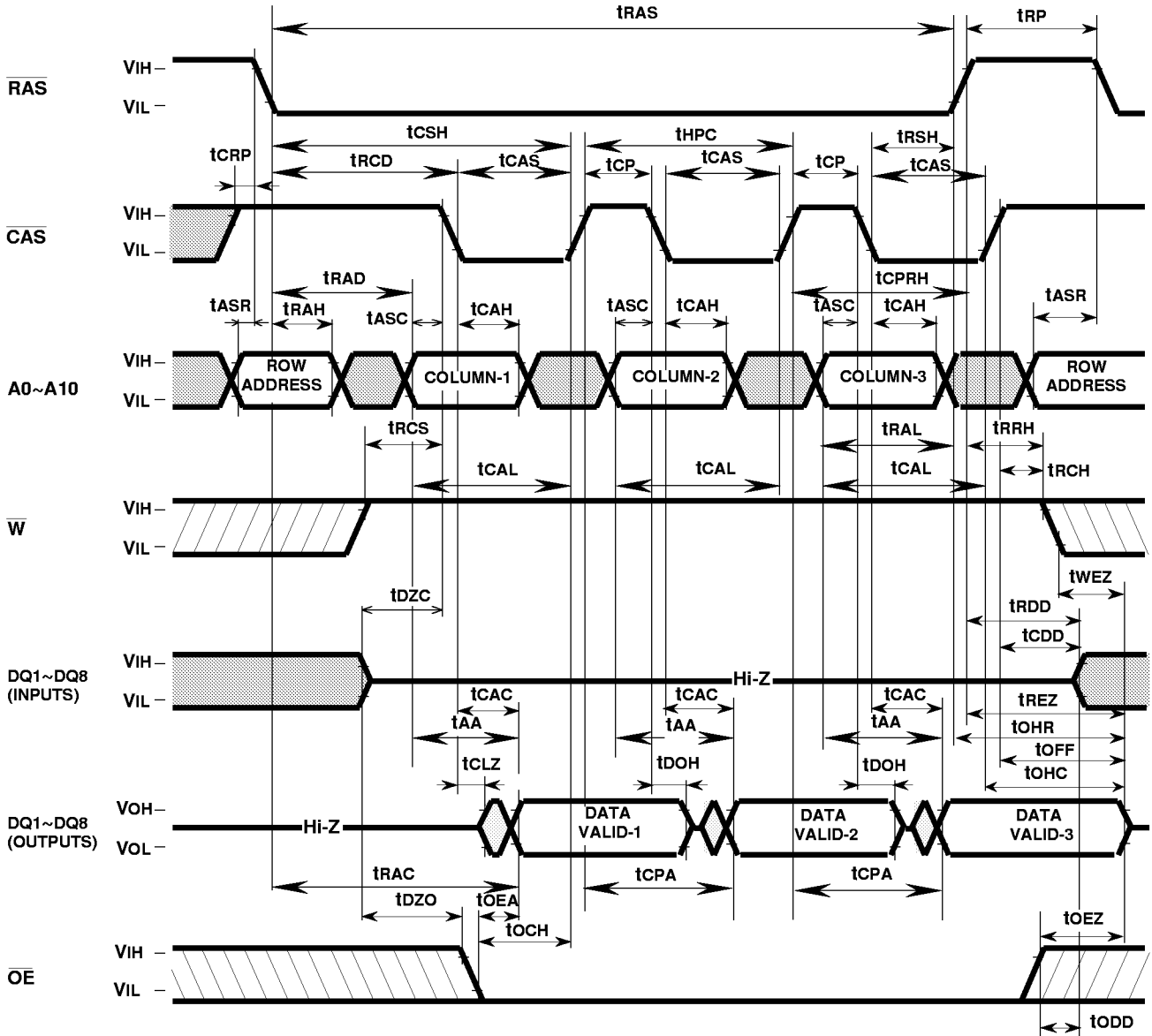
Delayed Write Cycle



M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

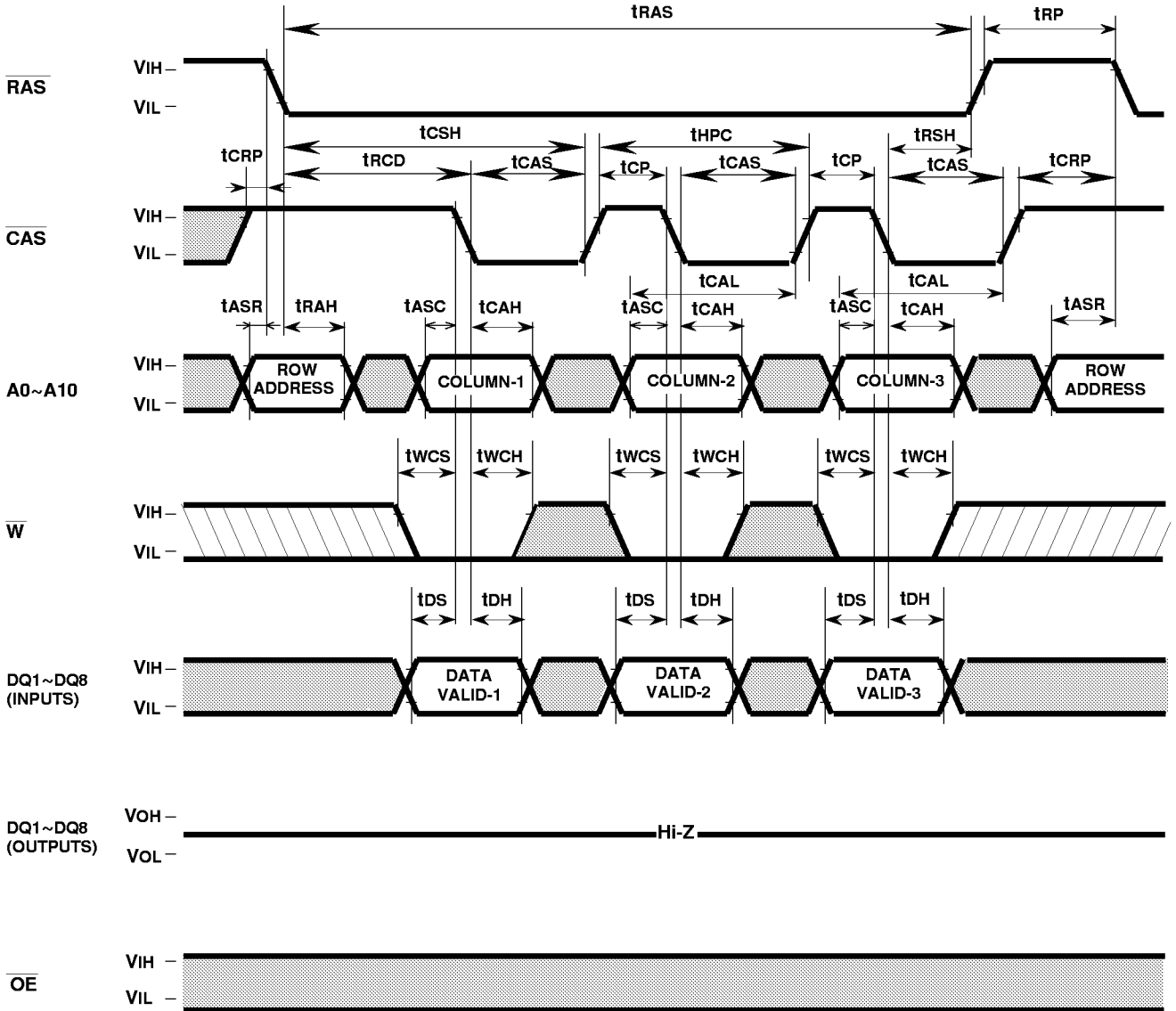
EDO Mode Read Cycle



M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

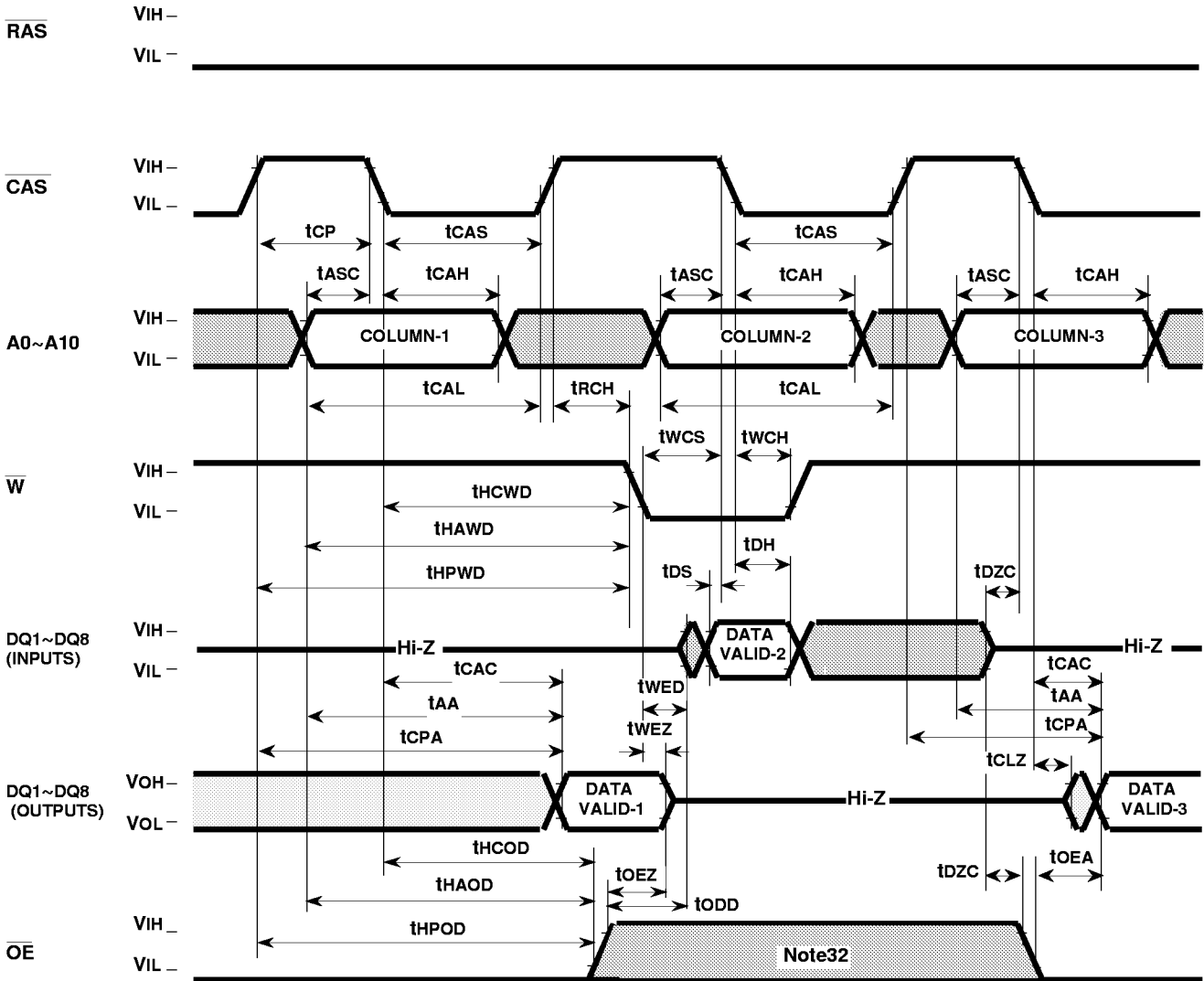
EDO Mode Early Write Cycle



M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

EDO Mode Mix Cycle (2) (Note32)

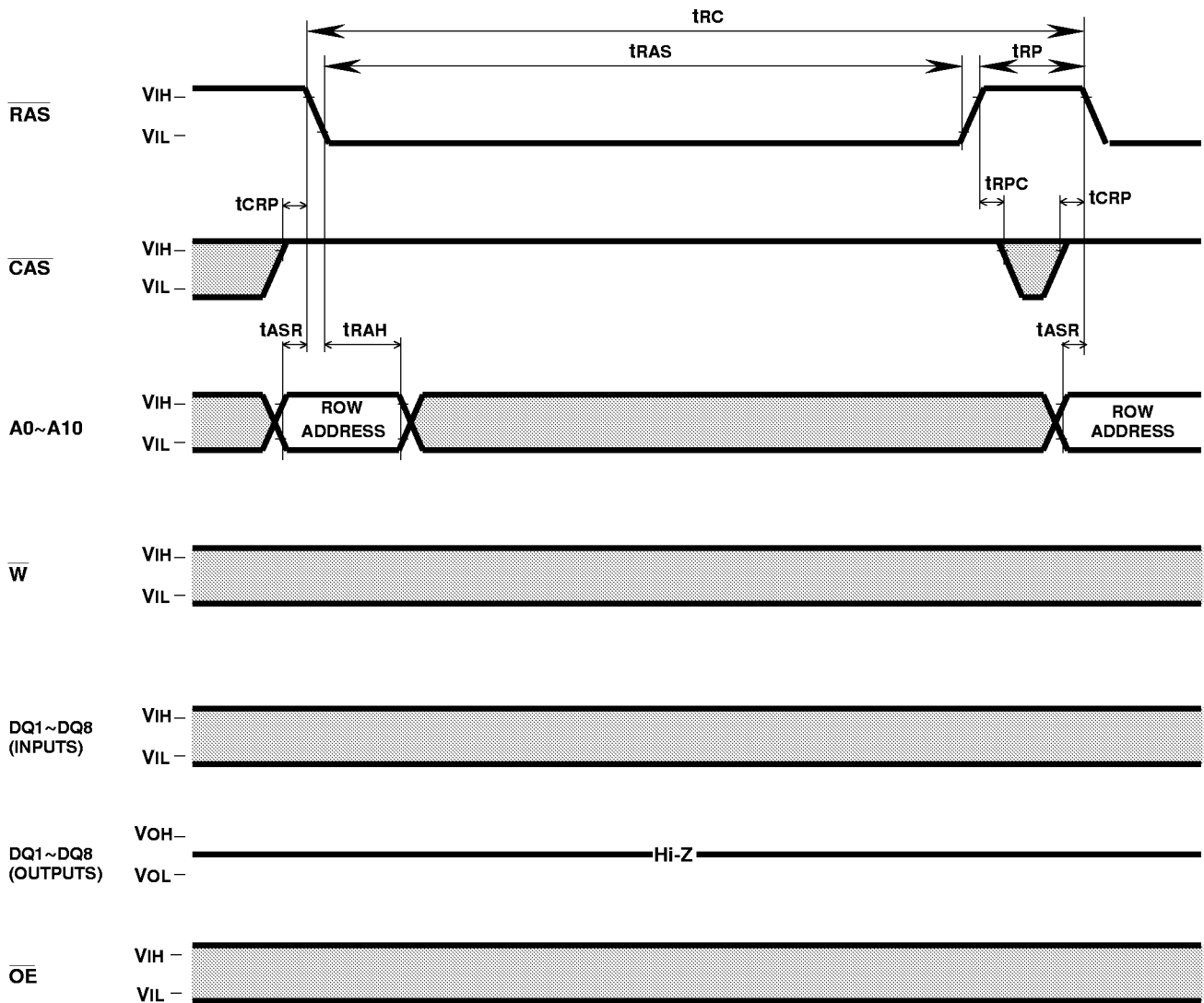


Note 32 : \overline{OE} low ; Hi-Z control by \overline{W}
 \overline{OE} high ; Hi-Z control by \overline{OE}

M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

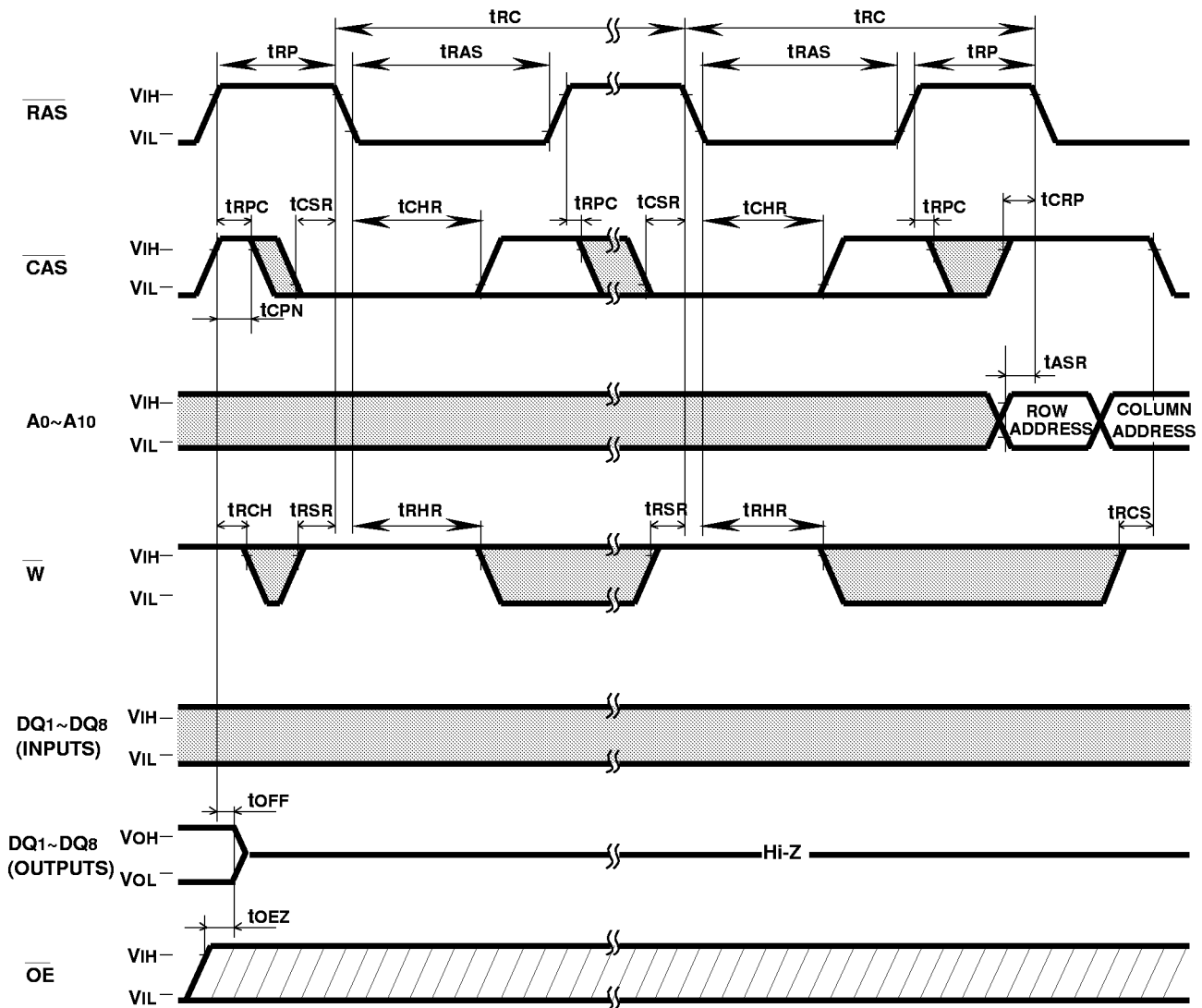
RAS-only Refresh Cycle



M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

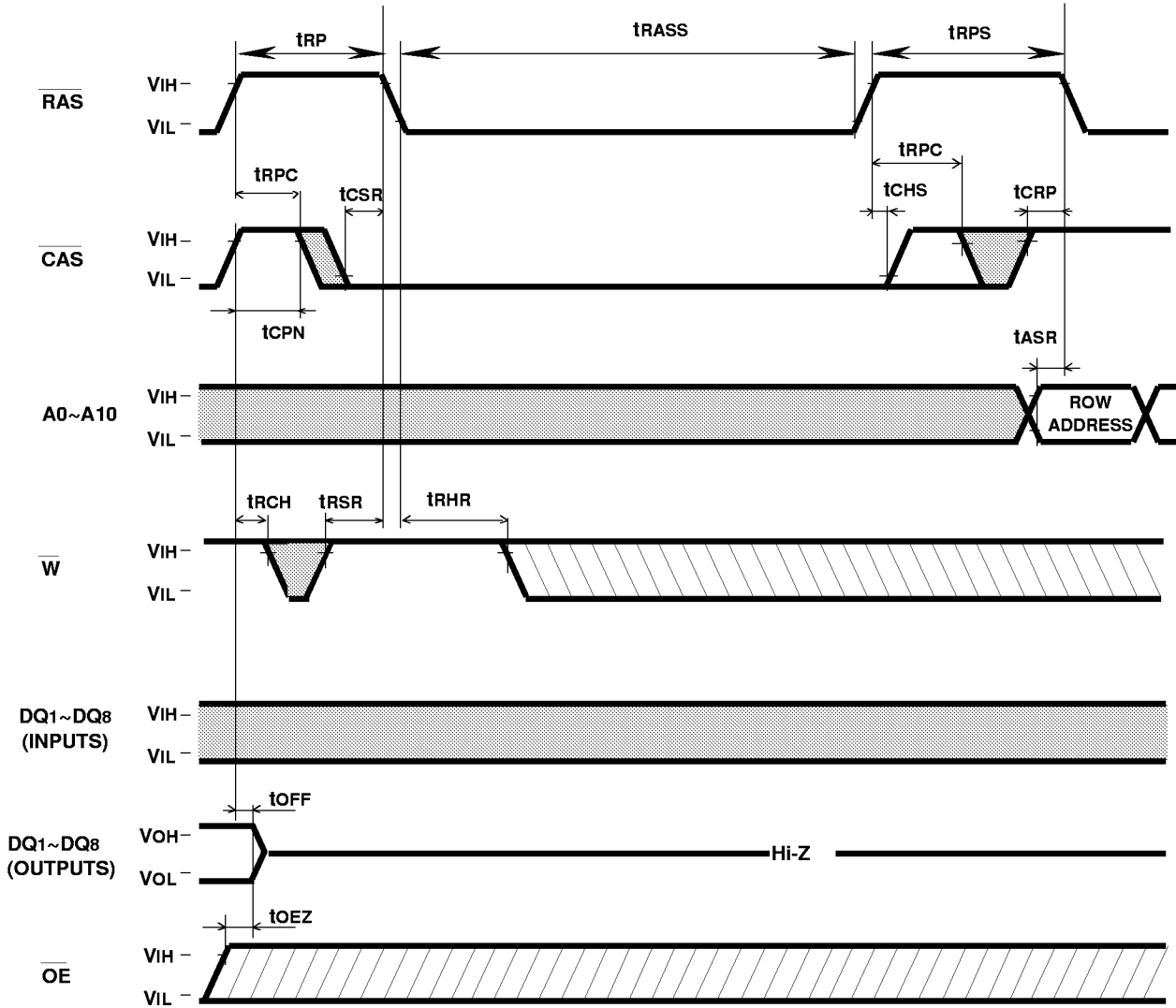
CAS before RAS Refresh Cycle, Slow Refresh Cycle



M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

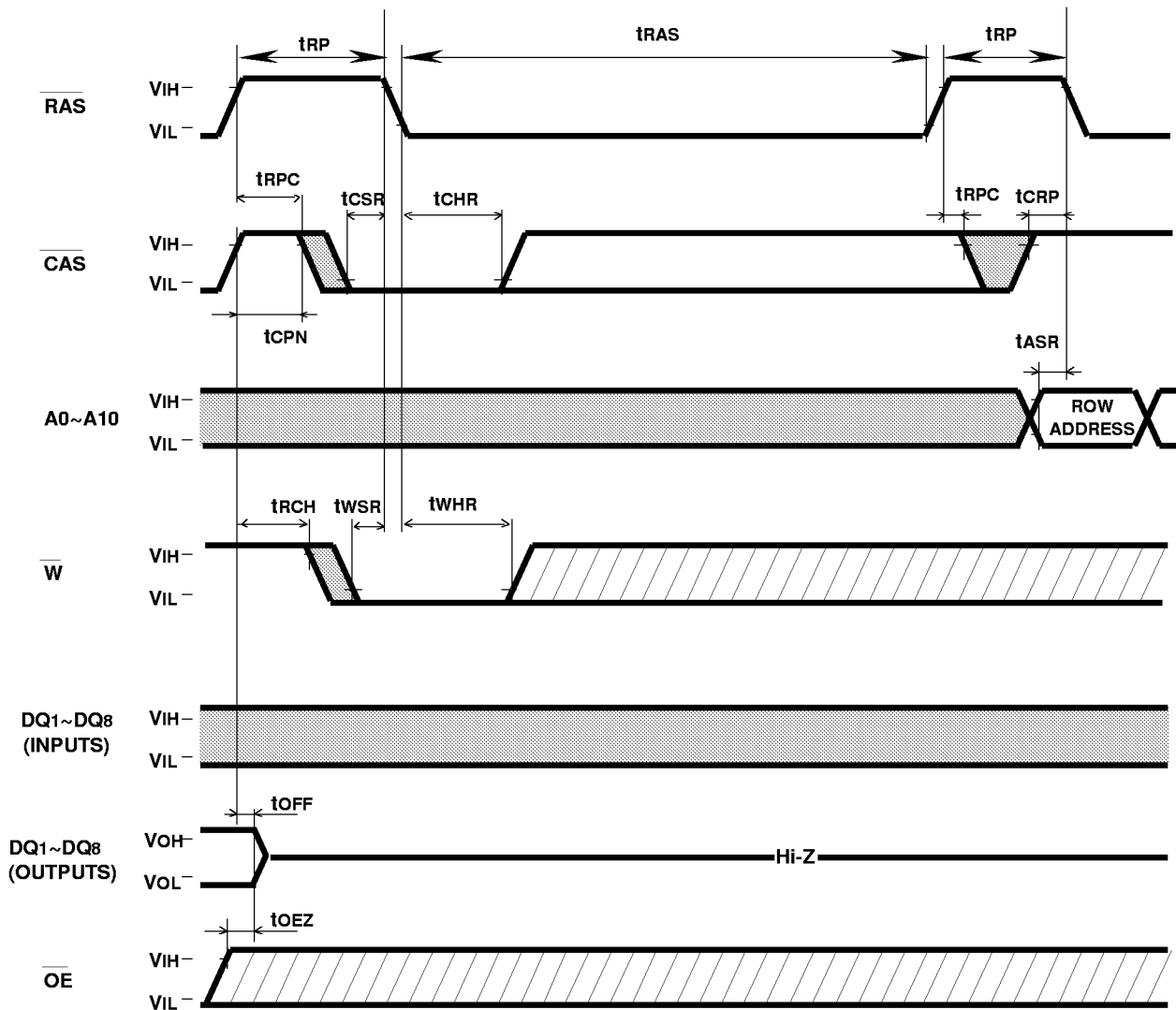
Self Refresh Cycle



M5M417805DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

TEST Mode SET Cycle (Note31)



Note31 : This cycle can be used for initialized cycle after power-up , however entried into Test Mode.