LOW-VOLTAGE DIFFERENTIAL SCSI (LVD) 27-LINE REGULATOR SET

FEATURES

- **SCSI SPI-2, SPI-3 and SPI-4 LVD SCSI 27-Line, Low-Voltage Differential Regulator**
- **2.7-V to 5.25-V Operation**
- **Integrated Regulator Set for LVD SCSI**
- **Differential Failsafe Bias**

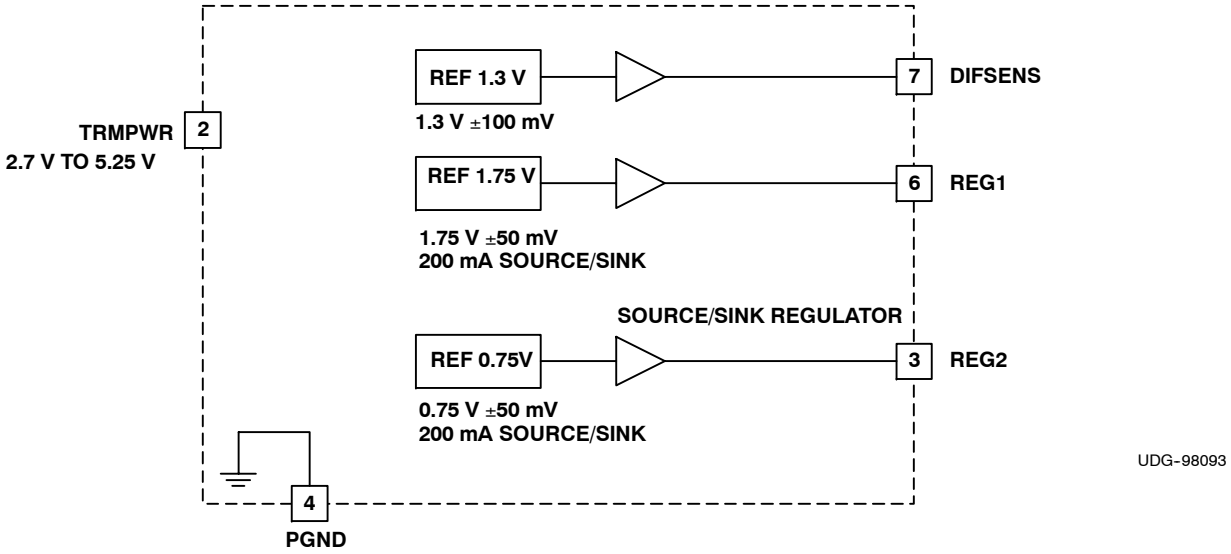
APPLICATIONS

- **Servers**
- **Workstations**
- **RAID Boxes**

DESCRIPTION

The UCC561 low-voltage differential (LVD) regulator set is designed to provide the correct references voltages and bias currents for LVD termination resistor networks (475 Ω, 121 Ω, and 475 Ω). The device also provides a 1.3-V output for “diff sense” signaling. With the proper resistor network, the UCC561 solution meets the common mode bias impedance, differential bias, and termination impedance requirements of SPI-2 (Ultra2), SPI-3 (Ultra3/Ultra160) and SPI-4 (Ultra320). The UCC561 is not intended for SPI-5 applications.

This device incorporates into a single monolith, two sink/source reference voltage regulators, a 1.3-V buffered output and protection features. The protection features include thermal shutdown and active current-limiting circuitry. The UCC561 is offered in 16-pin SOIC (DP) package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
UCC561	SOIC-16	DP	0°C to 70°C	UCC561DP	Rail, 70

(1) For the most current specification and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

	UCC561	UNIT
TERMPWR	6	V
Package dissipation	1.2	W
Junction temperature, T_J	-55 to 150	°C
Storage temperature, T_{stg}	-65 to 150	°C

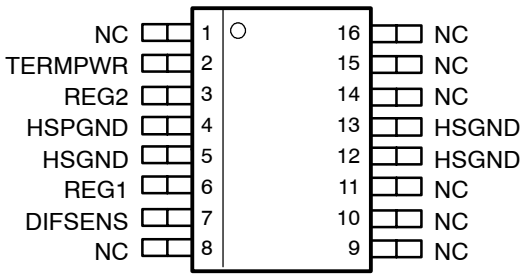
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Currents are positive into and negative out of the specified terminals.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
$V_{TERMPWR}$, TermPower voltage	2.70		5.25	V

DP PACKAGE
(TOP VIEW)



NC = No connection

ELECTRICAL CHARACTERISTICS

T_J = 0°C to 70°C, $V_{TERMPWR}$ = 3.3 V unless otherwise noted(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TERMPWR Supply Current					
TERMPWR supply current	No load			40	mA
TERMPWR voltage		2.70		5.25	V
Regulator					
1.75-V regulator	REG1 (±125 mA)	1.70	1.75	1.80	V
1.3-V regulator	-5 mA ≤ $I_{DIFSENS}$ ≤ 50 μA	1.2	1.3	1.4	V
0.75-V regulator	REG2 (±125 mA)	0.70	0.75	0.80	V
1.75-V regulator source current	V_O = 1.25 V	-200			mA
1.75-V regulator sink current	V_O = 2.25 V	200			mA
1.75-V regulator source current limit(1)		-200		-700	mA
1.75-V regulator sink current limit(1)		200		700	mA
1.3-V regulator source current	$V_{DIFSENS}$ = 0 V	-5		-15	mA
1.3-V regulator sink current	$V_{DIFSENS}$ = 2.4 V	50		200	μA
0.75-V regulator source current	V_O = 0.25 V	-200			mA
0.75-V regulator sink current	V_O = 1.25 V	200			mA
0.75-V regulator source current limit(1)		-200		-700	mA
0.75-V regulator sink current limit(1)		200		700	mA

(1) Ensured by design. Not production tested.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HSPGND	4	-	Heat sink power ground pin.
HSGND	5, 12, 13	-	Heat sink ground pin which should be attached to the ground plane on a multilayer board or large copper area on a 2 layer board.
REG1	6	O	1.75-V source/sink regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. For best performance, a 4.7-μF low-ESR capacitor is recommended. Lead lengths should be kept to a minimum.
REG2	3	O	0.75-V source/sink regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. For best performance, a 4.7-μF low-ESR capacitor is recommended. Lead lengths should be kept to a minimum.
DIFSENS	7	O	1.3-V source/sink regulated output voltage pin. The part is internally current limited to the SCSI SPI-2 through SPI-4 standards for both sinking and sourcing current to prevent damage.
TERMPWR	2	I	Supply voltage pin. The pin should be decoupled with at least a 2.2-μF low-ESR capacitor. For best performance, a 4.7-μF low-ESR capacitor is recommended. Lead lengths should be kept to a minimum.

APPLICATION INFORMATION

The resistor stack with the 1.75-V and 0.75-V reference gives the correct differential impedance, bias voltage, common mode differential impedance, and common mode voltage as show in Table 1.

Table 1. UCC561 Resistor Stack vs. Standard (SPI–2 through SPI–4)

PARAMETER	UCC561	STANDARD	UNITS
Differential Impedance	107.3	100 to 110	Ω
Differential bias voltage	112.9	100 to 125	mV
Common-mode differential impedance	237	100 to 300	Ω
Common-mode voltage	1.25	1.2 to 1.3	V

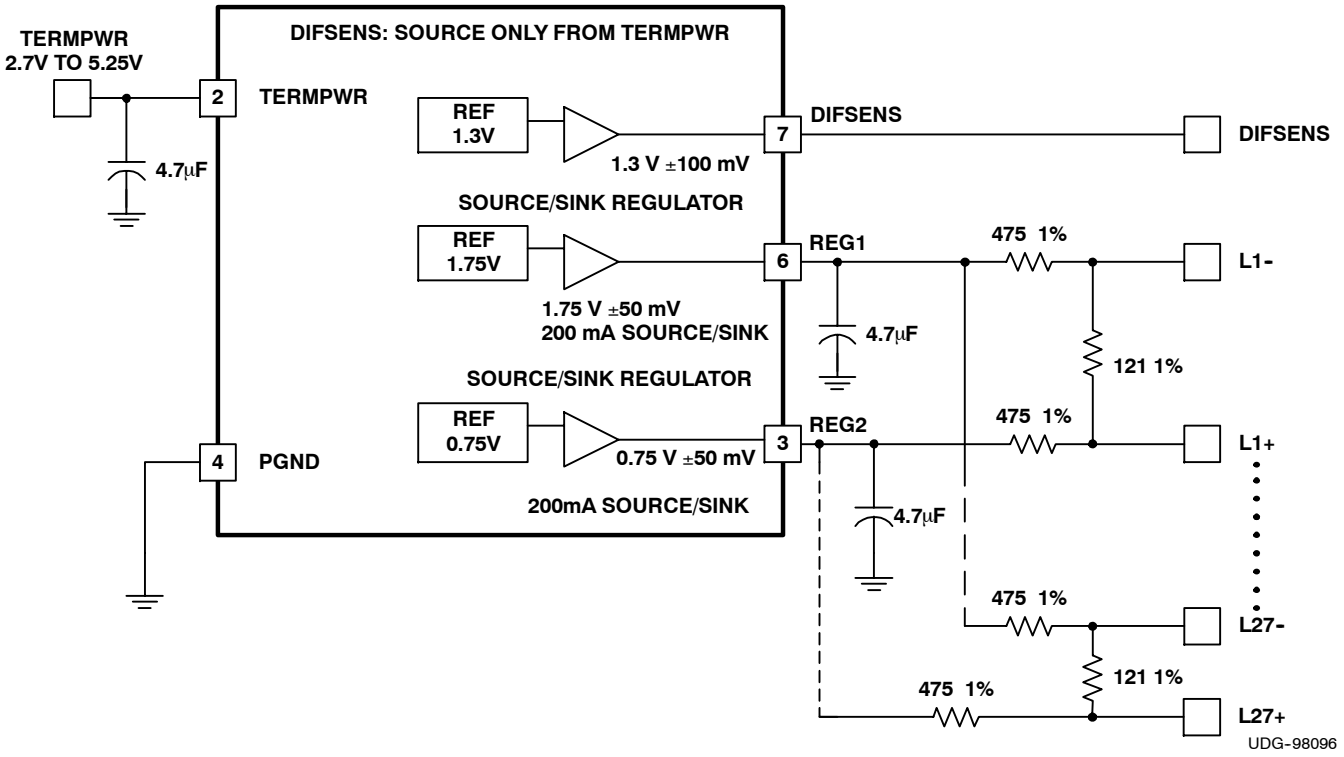


Figure 1. Low-Voltage Differential Discrete Resistor Stack

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC561DP	LIFEBUY	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		UCC561DP	
UCC561DPG4	LIFEBUY	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		UCC561DP	
UCC561DPTR	LIFEBUY	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		UCC561DP	
UCC561DPTRG4	LIFEBUY	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		UCC561DP	
UCC561TD	OBSOLETE	TO-220	KC	5		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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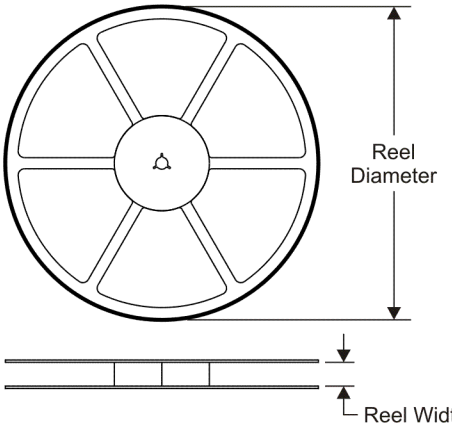
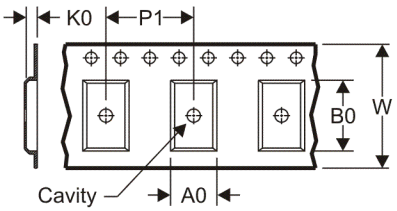
TAPE AND REEL INFORMATION

REEL DIMENSIONS

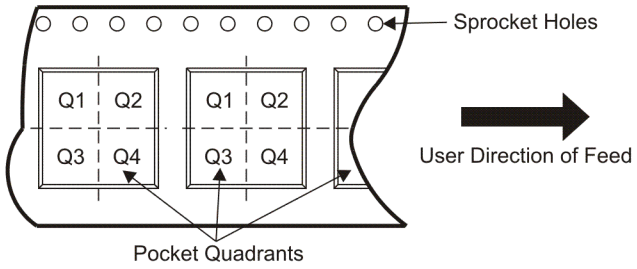


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

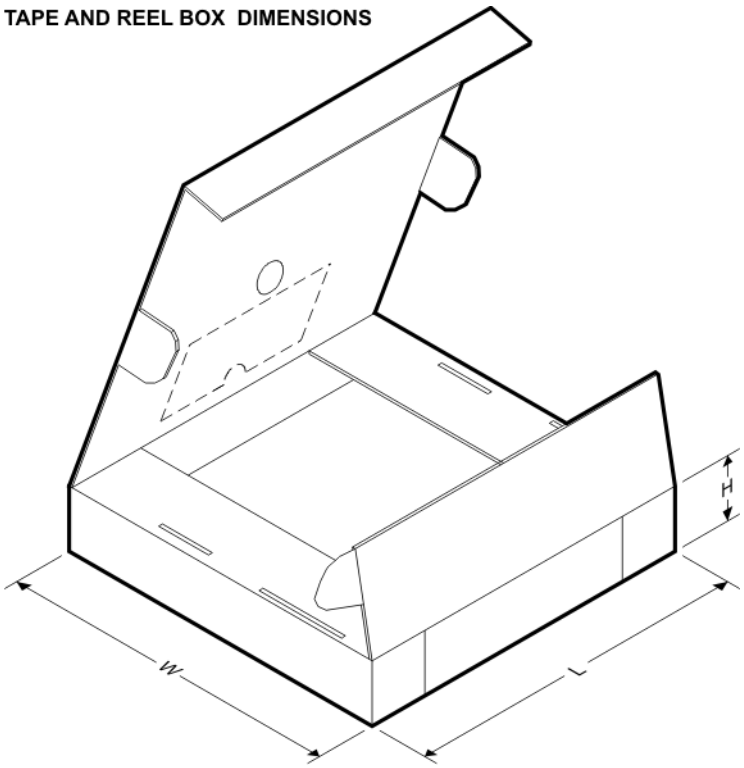
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC561DPTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

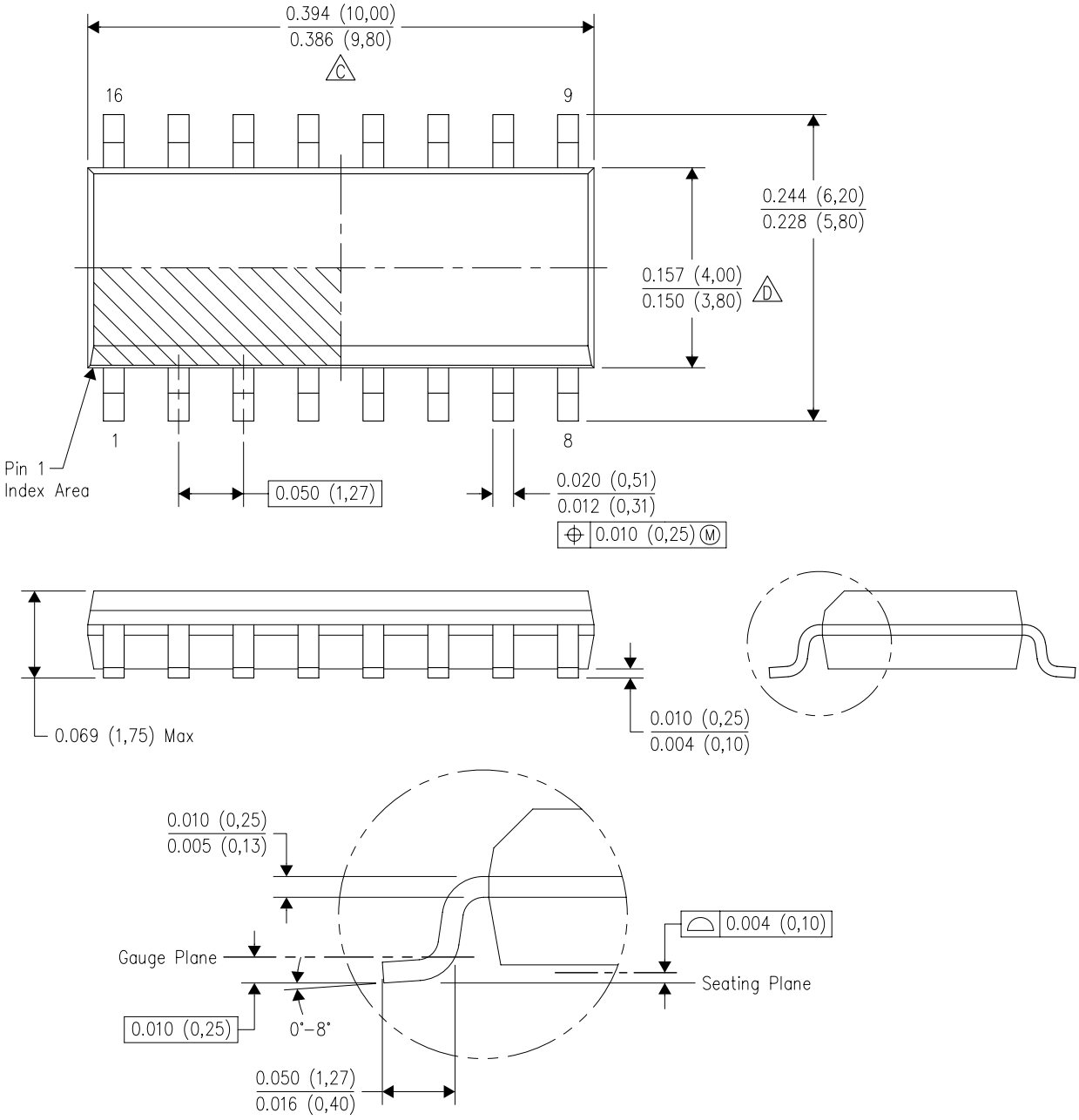
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

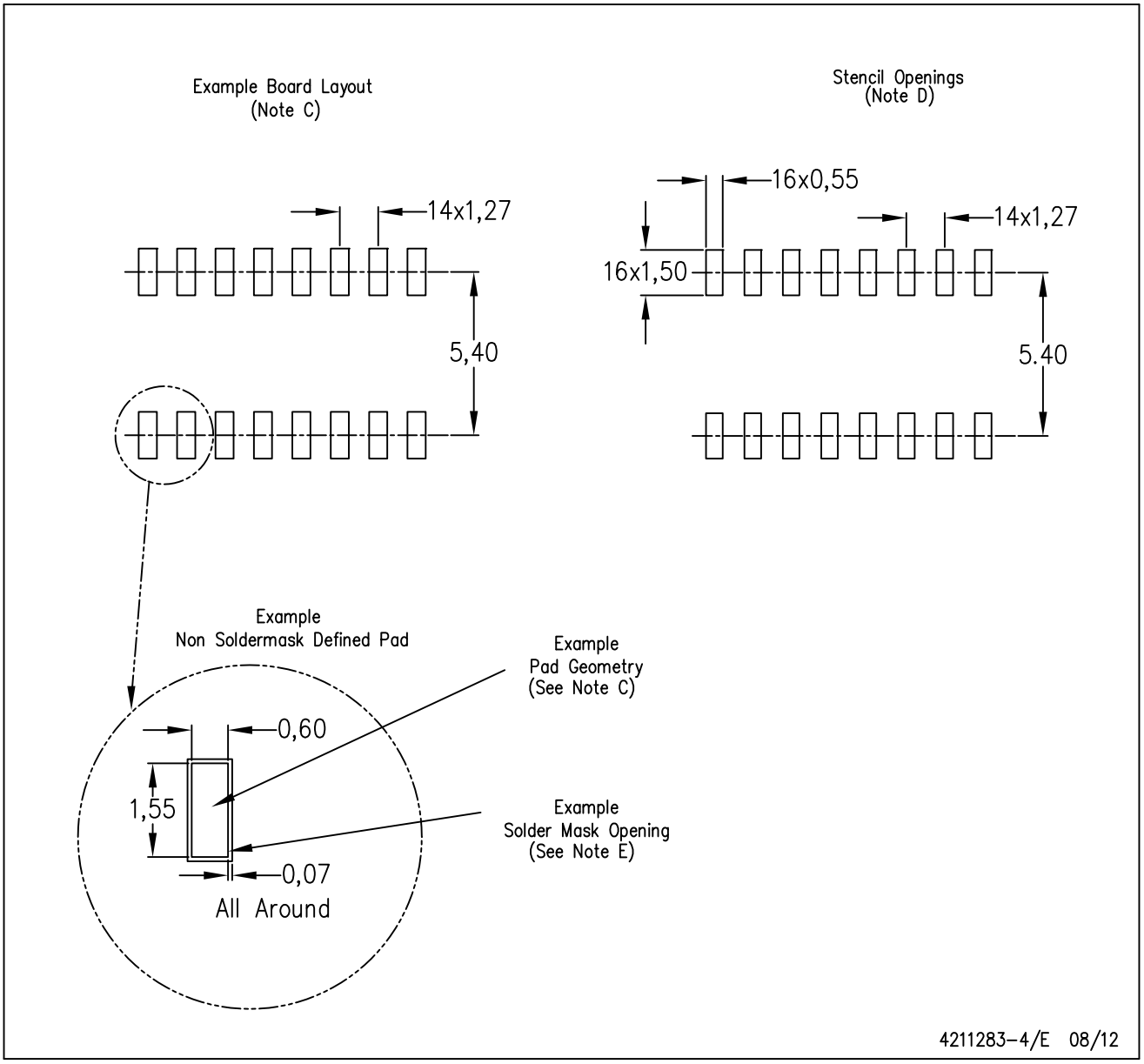
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC561DPTR	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



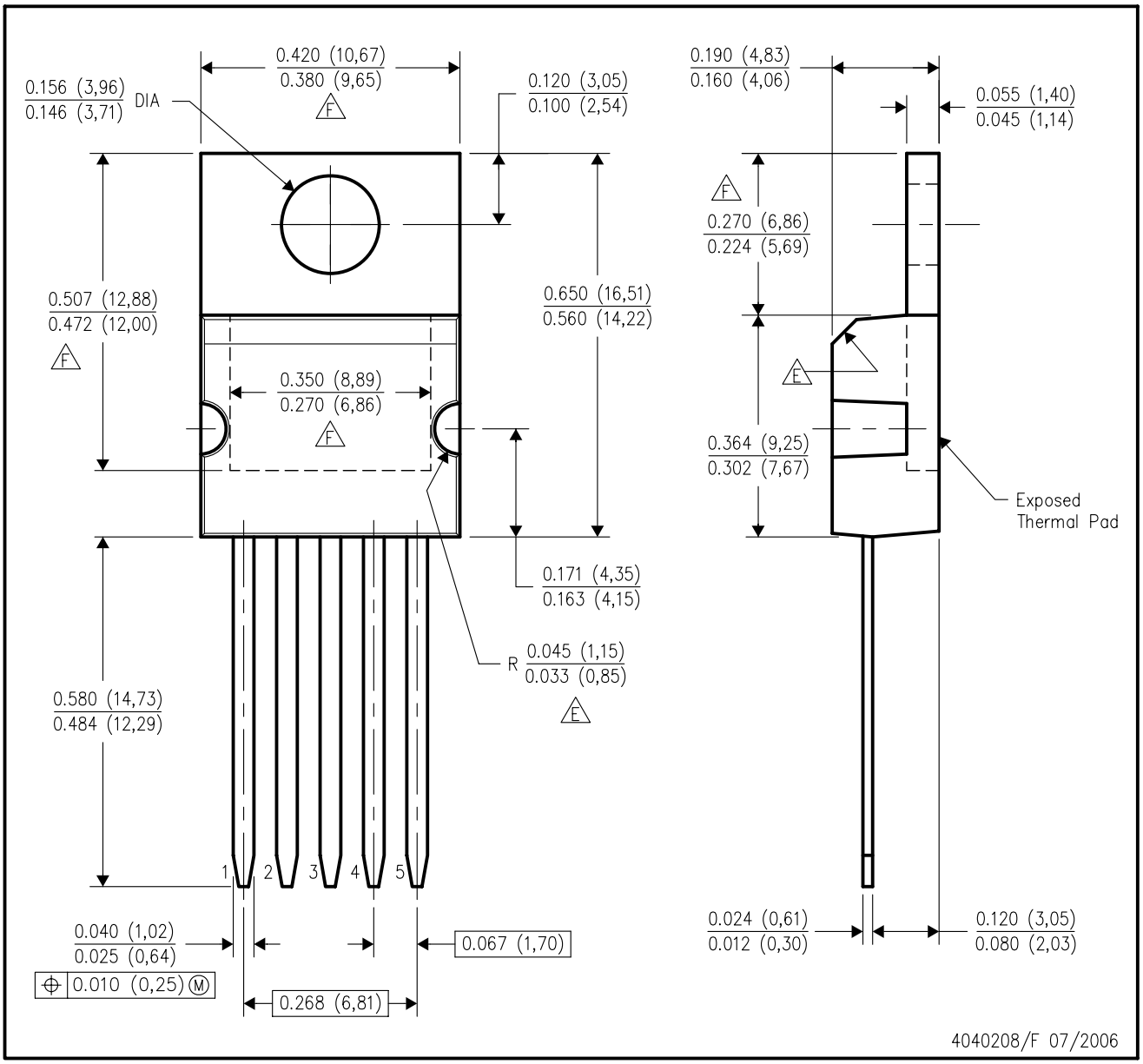
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

KC (R–PSFM–T5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. All lead dimensions apply before solder dip.
D. The center lead is in electrical contact with the mounting tab.
E. These features are optional.
F. Thermal pad contour optional within these dimensions.

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