AH103

High Gain, High Linearity ½ Watt Amplifier

The Communications Edge ™

Product Information

Product Features

- 60 – 2700 MHz
- +27 dBm P1dB
- +46 dBm Output IP3
- 28.5 dB Gain @ 900 MHz
- Excellent ACPR
- MTTF > 100 Years
- SOIC-8 Pkg w/ heat slug

Applications

- Mobile Infrastructure
- W-LAN / ISM / RFID
- MDS / MMDS Infrastructure

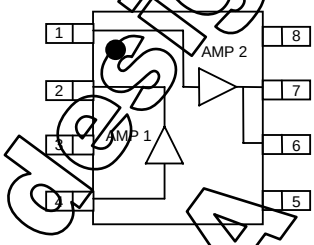
Product Description

The AH103 is a high gain, high linearity ½-Watt amplifier. This device is comprised of two individual MMIC amplifiers internally and can be used with an external interstage match for any of the mobile infrastructure frequency bands. The dual-stage amplifier achieves up to +46 dBm IP3 performance with 28.5 dB gain.

The device conforms to WJ Communications' long history of producing high reliability and quality components. The AH103 has an associated MTTF of a minimum of 100 years at a mounting temperature of 85°C. All devices are 100% RF & DC tested.

The product is targeted for use as driver amplifiers for wireless infrastructure where high performance and high linearity are required.

Functional Diagram



Function	Pin No.
Amp2 in	1
Amp1 out / Bias 1	2
Ground	3, 5, 8, Backside copper
RF in (Amp1 in)	4
RF out (Amp2 out)	6
Bias 2	7

Specifications

Parameter	Units	Min	Typ	Max
Frequency Range (2)	MHz	60	800	2700
Gain	dB	26.5	28.5	
Input Return Loss	dB		20	
Output Return Loss	dB		11	
Output P1dB	dBm	+26	+27	
Output IP3 (3)	dBm	+43	+46	
IS-95 Channel Power (4) @ -45 dBc ACPR	dBm		+21	
Noise Figure	dB		2.9	
Supply Voltage (Amp1)	V		+4.5	
Supply Voltage (Amp2)	V		+9	
Operating Current (Amp1)	mA	55	75	100
Operating Current (Amp2)	mA	170	200	230
Thermal Resistance (5)	°C / W			20.6
Junction Temperature (6)	°C			200

Test conditions unless otherwise noted.

1. T = 25ºC, Vdd1 = +4.5 V, Vdd2 = +9 V, Frequency = 800 MHz in a tuned application circuit.
2. The frequency of operation & bandwidth is determined by the external interstage match.
3. 3OIP measured with two tones at an output power of +10 dBm/tone separated by 10 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
4. IS-95, 9 Channels Forward, Pk/Avg Ratio = 11.5 dB at a .001% probability, ±750 kHz offset, 30 kHz BW, Channel BW = 1.23 MHz, frequency = 880 MHz.
5. The worst-case junction temperature for a given ground tab temperature can be calculated by multiplying the thermal resistance with the total package power dissipation and adding it to the tab temperature. ie. At 85°C case temperature for a typical device, the worst-case junction temperature would be = 85°C + (9 V * 0.2 A + 4.5 V * 0.075 A) = 129°C.
6. The junction temperature sustains a minimum MTTF rating of 1 million hours of usage.

Typical Performance

Parameter	Units	Typical			
Frequency	MHz	900	1900	2140	2400
S21	dB	28.5	26	25	24.7
S11	dB	-15	-12	-11	-12
S22	dB	-11	-11	-14	-17
Output P1dB	dBm	+27	+26.5	+26.5	+26
Output IP3	dBm	+46	+45	+45	+43.3
Channel Power @ -45 dBc ACPR / ACLR	dBm	+21	+20	+17.2	
Noise Figure	dB	2.9	3.7	3.5	3.6
Supply Bias 1		+4.5 V @ 75 mA			
Supply Bias 2		+9 V @ 200 mA			

7. Typical parameters reflect performance in an application circuit.
8. An IS-95 signal is used for 915 / 1960 MHz. A 3GPP W-CDMA signal is used for 2140 MHz.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +125 °C
DC Voltage (pin 2)	+6 V
DC Voltage (pin 6, 7)	+11 V
RF Input Power (continuous)	4 dB above Input P1dB
Junction Temperature	+220°C

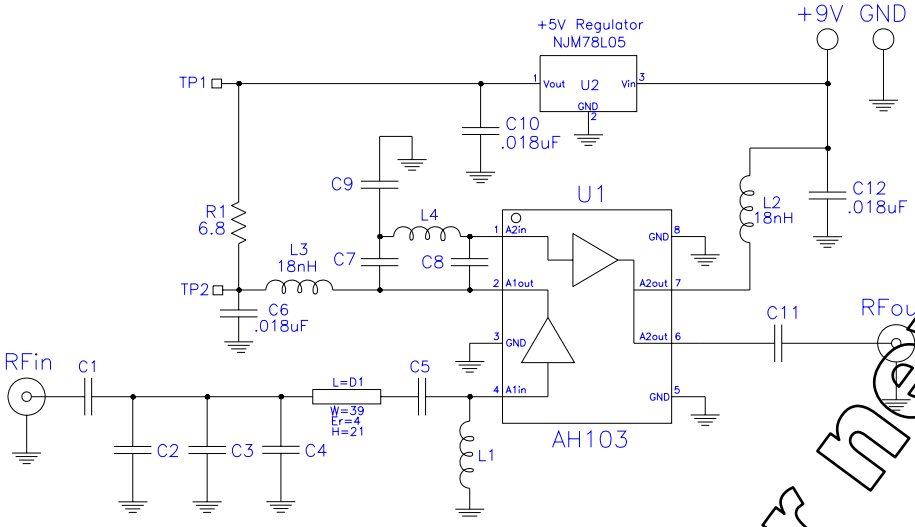
Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

Part No.	Description
AH103	High Gain ½ Watt Amplifier (available in tape and reel)

Specifications and information are subject to change without notice

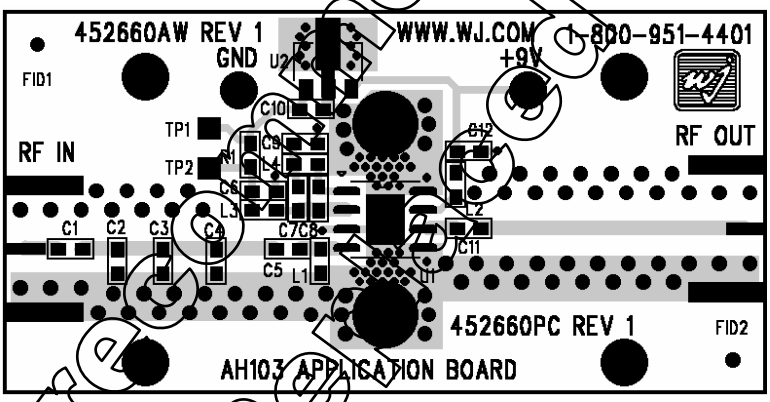
Application Circuit



Notes:

1. DNP = Do not place this component.
2. Distance "D1" measured from U1, pin 4 to edge of Cx (where x = 2, 3, or 4).
   a. D1 = 0.620" to C2 (for use with AH103-PCB1750)
      The 2.0 pF input tuning capacitor is placed .045" to the left of "C2" shown on the silk screen. The shunt capacitor is placed directly on the right and adjacent to the input blocking capacitor C1.
   b. D1 = 0.450" to C3 (for use with AH103-PCB1900)
   c. D1 = 0.310" to C4 (for use with AH103-PCB2140)
3. A voltage regulator is used in this circuit (U2) to drop the +9 V to a +5 V usable supply for the first internal amplifier. It is permissible to remove the regulator and operate the 1st amplifier stage directly off of +5 V supply onto Test Point 1 (TP1). The use of a +5 V supply on the 1st amplifier stage requires a dropping resistor of 6.8 Ω.
4. A +4.5 V supply can also be used to bypass the 6.8 Ω and can be applied to Test Point 2 (TP2).

Evaluation Board PCB Layout



Circuit Board Material: .014" FR-4, 4 layers, .062" total thickness

Bill of Materials
All Application Circuits

Ref. Desig.	Component
R1	6.8 Ω chip resistor
L2, L3	18nH chip inductor
C6, C10, C12	.018 µF chip capacitor
U1	WJ AH103 Amplifier
U2	+5V Regulator, National Semiconductor NJM78L05

5. All components are of size 0603.
6. Other components not shown above are specific for the frequency band of interest.

AH103-PCB900
700 – 1000 MHz App. Circuit

Ref. Desig.	Component
L1	10 nH chip inductor
L4	5.6 nH chip inductor
C1	0 Ω chip resistor
C5, C11	5.6 pF chip capacitor
C7	10 pF chip capacitor
C9	1.5 pF chip capacitor
C2, C3, C4, C8	DNP

AH103-PCB1750
1700 – 1800 MHz App. Circuit

Ref. Desig.	Component
C1, C11	47 pF chip capacitor
C2	2.0 pF chip capacitor
C5	0 Ω chip resistor
C8	10 pF chip capacitor
C3, C4, C7 C9, L1, L4	DNP

See note (2a) for the proper placement of C2.

AH103-PCB1900
1800 – 2000 MHz App. Circuit

Ref. Desig.	Component
C1, C11	47 pF chip capacitor
C3	1.5 pF chip capacitor
C5	0 Ω chip resistor
C8	10 pF chip capacitor
C2, C4, C7 C9, L1, L4	DNP

AH103-PCB2140
2110 – 2140 MHz App. Circuit

Ref. Desig.	Component
C1, C11	47 pF chip capacitor
C4	1.2 pF chip capacitor
C5	0 Ω chip resistor
C8	10 pF chip capacitor
C2, C3. C7 C9, L1, L4	DNP

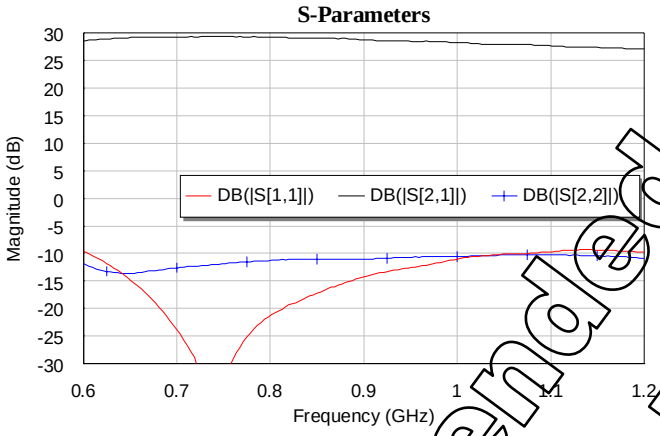
2.4 – 2.7 GHz Reference Circuit

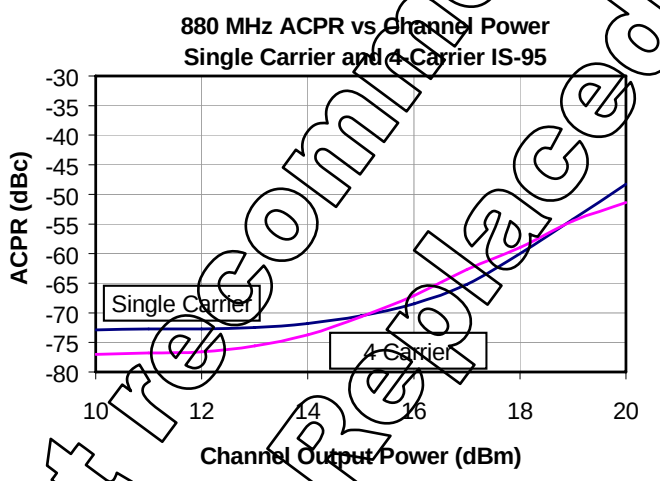
Ref. Desig.	Component
L1	1 pF chip capacitor
C1	0 Ω chip resistor
C5	22 pF chip capacitor
C8	10 pF chip capacitor
C11	47 pF chip capacitor
C2, C3. C4 C7, C9, L4	DNP

Application Circuit: 700 – 1000 MHz (AH103-PCB900)

Typical RF Performance

Frequency	880 MHz
S21 – Gain	28.5 dB
S11 – Input Return Loss	-15 dB
S22 – Output Return Loss	-11 dB
Output P1dB	+27 dBm
Output IP3 (+10 dBm / tone, 1 MHz spacing)	+45 dBm
IS-95 Channel Power @ -45 dBc ACPR	+21 dBm
Noise Figure	2.9 dB
Supply Bias (Amp 1)	+4.5 V @ 75 mA
Supply Bias (Amp 2)	+9 V @ 200 mA





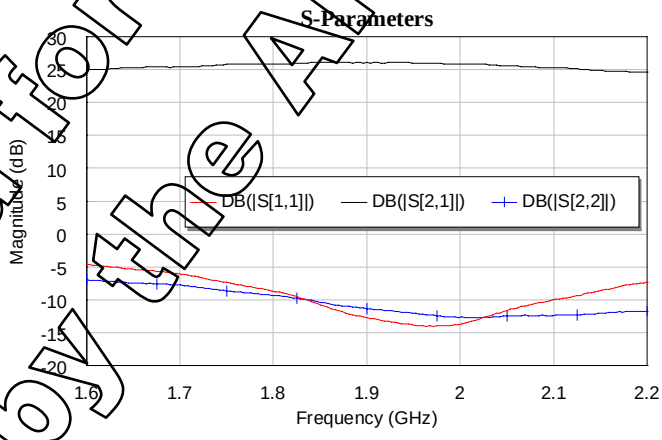
Single Carrier Signal:
IS-95, 9 Channels Forward, Pk/Avg Ratio = 11.5 dB at a .001% probability
±750 kHz offset, 30 kHz bandwidth, Channel BW = 1.23 MHz

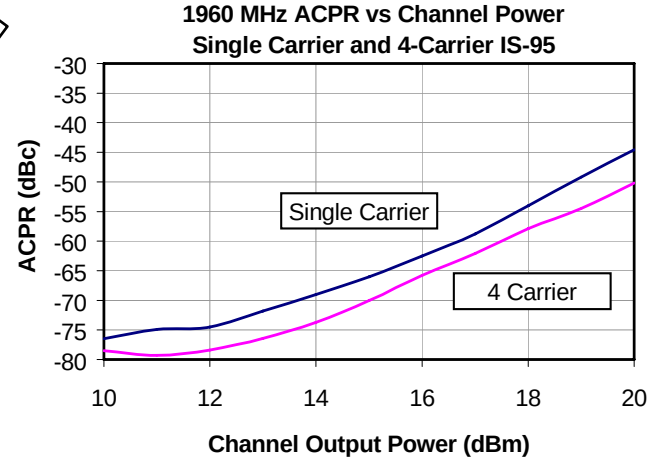
Four-Carrier Signal:
IS-95, 9 Channels Forward, Pk/Avg Ratio = 10.2 dB at a .001% probability
±2.60 MHz offset, 30 kHz bandwidth, Channel BW = 4.92 MHz

Application Circuit: 1.8 – 2.0 GHz (AH103-PCB1900)

Typical RF Performance

Frequency	1960 MHz
S21 – Gain	26 dB
S11 – Input Return Loss	-12 dB
S22 – Output Return Loss	-11 dB
Output P1dB	+26.5 dBm
Output IP3 (+10 dBm / tone, 1 MHz spacing)	+45 dBm
IS-95 Channel Power @ -45 dBc ACPR	+20 dBm
Noise Figure	3.7 dB
Supply Bias (Amp 1)	+4.5 V @ 75 mA
Supply Bias (Amp 2)	+9 V @ 200 mA





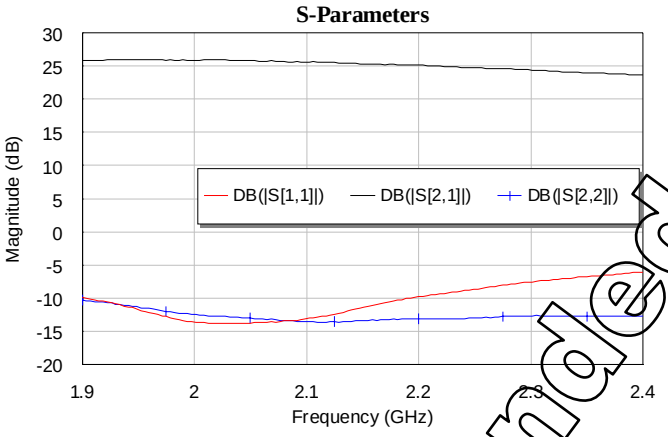
Single Carrier Signal:
IS-95, 9 Channels Forward, Pk/Avg Ratio = 11.5 dB at a .001% probability
±885 kHz offset, 30 kHz bandwidth, Channel BW = 1.23 MHz

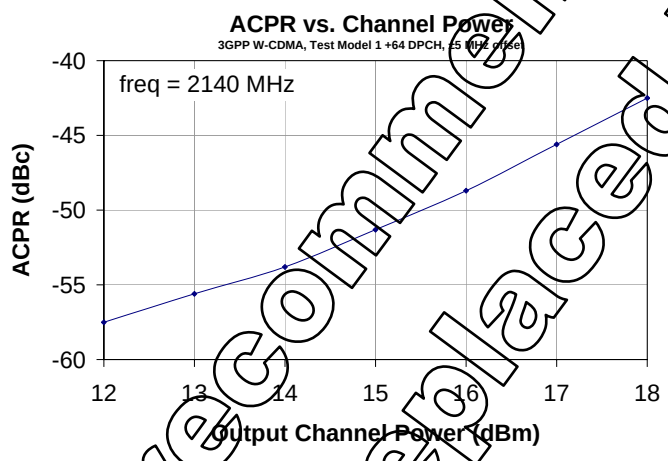
Four-Carrier Signal:
IS-95, 9 Channels Forward, Pk/Avg Ratio = 10.2 dB at a .001% probability
±2.76 MHz offset, 30 kHz bandwidth, Channel BW = 4.98 MHz

Application Circuit: 2110 – 2170 MHz (AH103-PCB2140)

Typical RF Performance

Frequency	2140 MHz
S21 – Gain	25 dB
S11 – Input Return Loss	-11 dB
S22 – Output Return Loss	-14 dB
Output P1dB	+26.5 dBm
Output IP3 (+10 dBm / tone, 1 MHz spacing)	+45 dBm
Noise Figure	3.5 dB
Supply Bias (Amp 1)	+4.5 V @ 75 mA
Supply Bias (Amp 2)	+9 V @ 200 mA

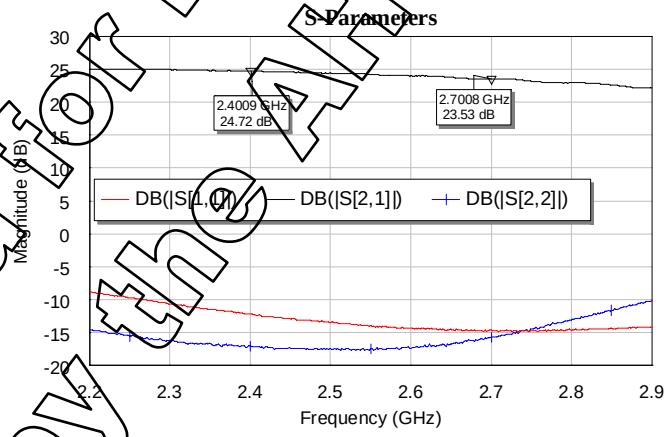




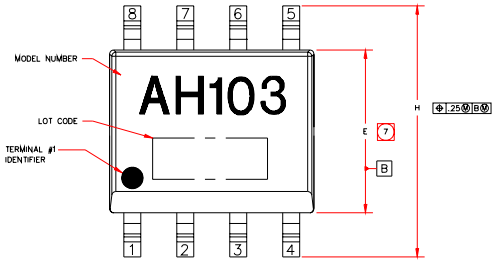
Reference Design: 2.4 – 2.7 GHz

Typical RF Performance

Frequency	MHz	2400	2700
S21 – Gain	dB	24.7	23.5
S11 – Input Return Loss	dB	-12	-15
S22 – Output Return Loss	dB	-17	-16
Output P1dB	dBm	+26	+25.2
Output IP3 (+10 dBm / tone, 1 MHz spacing)	dBm	+43.3	+41.9
Noise Figure	dB	3.6	3.6
Supply Bias (Amp 1)		4.5 V @ 75 mA	
Supply Bias (Amp 2)		9 V @ 200 mA	

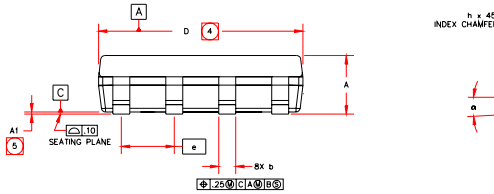


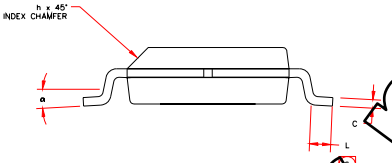
Outline Drawing

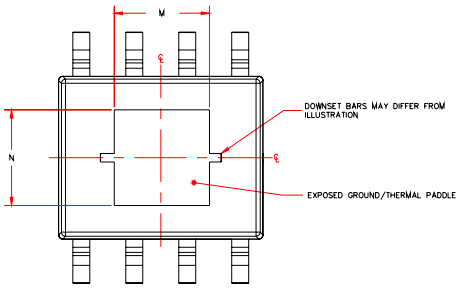


NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.







SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.30	1.52	.051	.064
A1	0	.10	0	.003
b	.38	.46	.015	.017
C	.18	.25	.007	.010
D	4.80	5.00	.189	.197
E	3.80	4.00	.150	.157
e	1.27 BSC		.050 BSC	
H	5.80	6.20	.228	.244
h	.25	.50	.01	.02
L	.40	1.27	.016	.050
M	2.95	3.30	.080	.130
N	2.95	3.05	.080	.120
α	0°	8°	0°	8°

Product Marking

The component will be marked with an "AH103" designator followed by a four- or five-digit alpha-numeric lot code on the top surface of the package. Tape and reel specifications for this part is located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD-sensitive device.

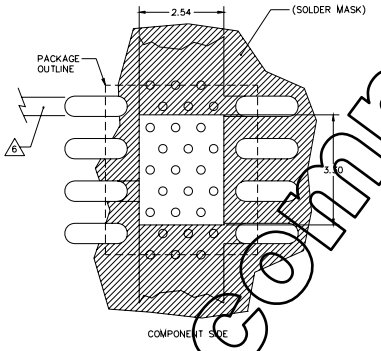
ESD Classification:	Class 1B
Value:	Passes ≥ 500 V to <1000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
ESD Classification:	Class III
Value:	Passes ≥ 500 V to <1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101
MSL Rating:	Level 1 at +235 °C convection reflow
Standard:	JEDEC Standard J-STD-020B

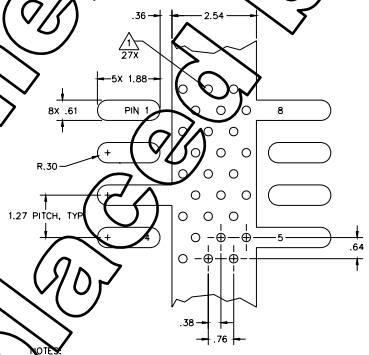
Functional Pin Layout

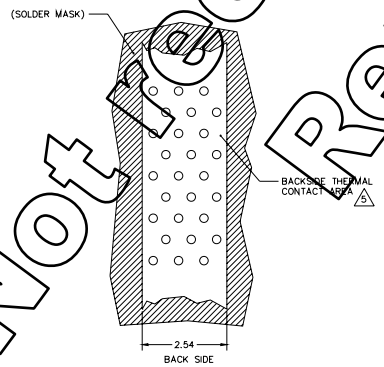
Pin	Function
1	Amp2 input
2	Amp1 output / Bias Amp1
3	Ground
4	RF input (Amp1 input)
5	Ground
6	RF output (Amp2 output)
7	Bias Amp2
8	Ground

The backside paddle is the Source and should be grounded for thermal and electrical purposes. All other pins should be grounded on the PCB.

Mounting Configuration / Land Pattern



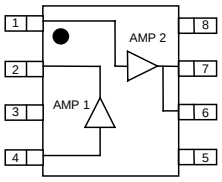




NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. FOR OPTIMAL THERMAL PERFORMANCE, EXPOSE SOLDERMASK ON BACKSIDE WHERE IT CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Typical Device Data



Typical AH103 Performance Chain Analysis at 900 MHz

Stage	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)	Voltage (V)	Current (mA)	Cumulative Performance			
							Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)
Amplifier 1	14.5	18	39	2.7	+4.5	75	14.5	18	39	2.7
Amplifier 2	14	27	46	3.1	+9	200	28.5	25.8	45.2	2.8
AH103	**Cumulative Performance**					**275**	**28.5**	**+25.8**	**+45.2**	**2.8**

S-Parameters (Amplifier #1, V_D = +4.5 V, I_D = 75 mA, T = 25°C, calibrated to device leads, pin 4 = port 1, pin 2 = port 2)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-4.86	-26.48	15.26	166.07	-21.98	27.52	-9.70	-36.91
200	-7.73	-22.56	14.09	165.44	-20.82	4.55	-15.06	-23.28
400	-6.98	-31.07	13.81	158.26	-20.79	-1.20	-13.38	-23.85
600	-7.02	-42.34	13.67	149.51	-20.87	-5.43	-13.47	-28.27
800	-7.16	-54.83	13.52	140.22	-20.74	-9.01	-13.71	-34.42
1000	-7.19	-67.46	13.36	131.15	-20.75	-12.46	-13.81	-40.37
1200	-7.17	-79.27	13.18	122.10	-20.61	-15.68	-14.16	-45.64
1400	-7.41	-91.82	13.04	113.28	-20.49	-19.43	-14.82	-50.24
1600	-7.64	-105.01	12.84	104.13	-20.43	-23.02	-15.82	-55.50
1800	-7.89	-118.56	12.65	95.51	-20.23	-27.00	-17.15	-60.75
2000	-8.01	-125.93	12.51	87.63	-20.10	-29.55	-17.66	-53.33
2200	-8.49	-142.46	12.36	78.62	-19.93	-34.96	-20.96	-54.42
2400	-8.67	-160.24	12.13	69.65	-19.89	-38.99	-26.00	-54.24
2600	-8.68	-172.38	11.93	63.44	-19.88	-43.41	-33.58	-50.38
2800	-8.41	169.78	11.67	54.46	-19.87	-47.77	-34.93	72.34
3000	-7.99	153.13	11.27	44.65	-19.92	-53.05	-25.07	91.10

S-Parameters (Amplifier #2, V_D = +9 V, I_D = 200 mA, T = 25°C, calibrated to device leads, pin 1 = port 1, pin 7 = port 2)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-14.89	-61.31	15.70	167.65	-19.34	7.31	-20.46	-69.94
200	-18.44	-66.85	15.25	161.10	-19.19	-8.11	-27.00	35.96
400	-13.76	-79.48	14.98	146.18	-18.48	-18.63	-18.71	6.17
600	-12.08	-100.14	14.63	131.18	-19.72	-29.44	-16.02	-1.40
800	-10.77	-119.25	14.23	116.54	-20.04	-39.85	-14.15	-10.84
1000	-9.63	-134.77	13.84	102.40	-20.41	-49.54	-12.62	-22.52
1200	-8.84	-148.91	13.45	88.71	-20.82	-58.10	-11.52	-32.78
1400	-8.26	-168.49	13.12	75.19	-21.26	-67.89	-10.66	-42.36
1600	-7.70	-177.35	12.79	61.97	-21.81	-76.50	-10.11	-52.56
1800	-7.18	-169.87	12.46	48.61	-22.20	-86.90	-9.60	-63.61
2000	-7.12	156.94	12.32	35.83	-22.71	-93.31	-9.46	-69.21
2200	-6.52	142.96	12.06	21.94	-23.51	-103.96	-9.28	-79.85
2400	-5.85	131.77	11.71	8.30	-24.26	-113.83	-8.99	-93.56
2600	-5.38	124.67	11.47	-1.71	-24.94	-120.76	-8.74	-104.09
2800	-4.72	115.12	11.10	-15.80	-25.66	-129.36	-8.43	-118.28
3000	-4.13	106.69	10.56	-30.06	-27.18	-137.91	-8.04	-135.08