SAMSUNG ELECTRONICS INC 42E D 7964142 0010616 1 SMGK

T-46-23-15

256KX4 Bit CMOS Video RAM

FEATURES

- Dual port Architecture
  256K × 4 bits RAM port
  512 × 4 bits SAM port
- Performance

Parameter \ Speed	−8	−10	−12
RAM access time (t_{RAC})	80ns	100ns	120ns
RAM access time (t_{CAO})	20ns	25ns	30ns
RAM cycle time (t_{RC})	150ns	180ns	220ns
RAM page mode cycle (t_{PC})	50ns	60ns	75ns
SAM access time (t_{SCA})	20ns	25ns	35ns
SAM cycle time (t_{SCC})	30ns	30ns	40ns
RAM active current	80mA	70mA	60mA
SAM active current	40mA	40mA	40mA

- Fast Page Mode
- RAM Read, Write, Read-Modify-Write
- Serial Read and Serial Write
- Read, Real Time Read and Split Read Transfer (RAM→SAM)
- Write, Split Write Transfer with Masking operation
- Block Write, Flash Write and Write per bit with Masking operation
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh
- Common Data I/O Using three state RAM Output Control
- All Inputs and Outputs TTL and CMOS Compatible
- Refresh: 512 Cycle/8ms
- Single +5V±10% Supply Voltage
- Plastic 28-PIN 400 mil SOJ and ZIP

Pin Name	Pin Function
SC	Serial Clock
SDQ_0-SDQ_3	Serial Data Input/Output
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write Per Bit/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
W_0/DQ_0-W_3/DQ_3	Data Write Mask/Input/Output
$\overline{SE}$	Serial Enable
A_0-A_8	Address Inputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
DSF	Special Function Control
QSF	Special Flag Output

GENERAL DESCRIPTION

The Samsung KM424C257 is a CMOS 256K×4 bit Dual Port DRAM. It consists of a 256K×4 dynamic random access memory (RAM) port and 512×4 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 2048 bits. It operates like a conventional 256K×4 CMOS DRAM. The RAM port has a write per bit mask capability.

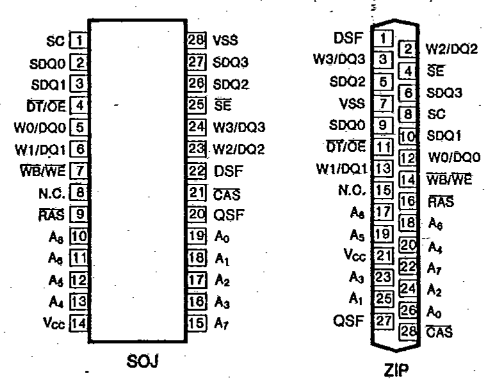
The SAM port consists of four 512 bit high speed shift registers that are connected to the RAM array through a 2048 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read or write transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM424C257 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All Inputs and I/O's are TTL and CMOS level compartible. All address lines and Data Inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN CONFIGURATION (Top Views)



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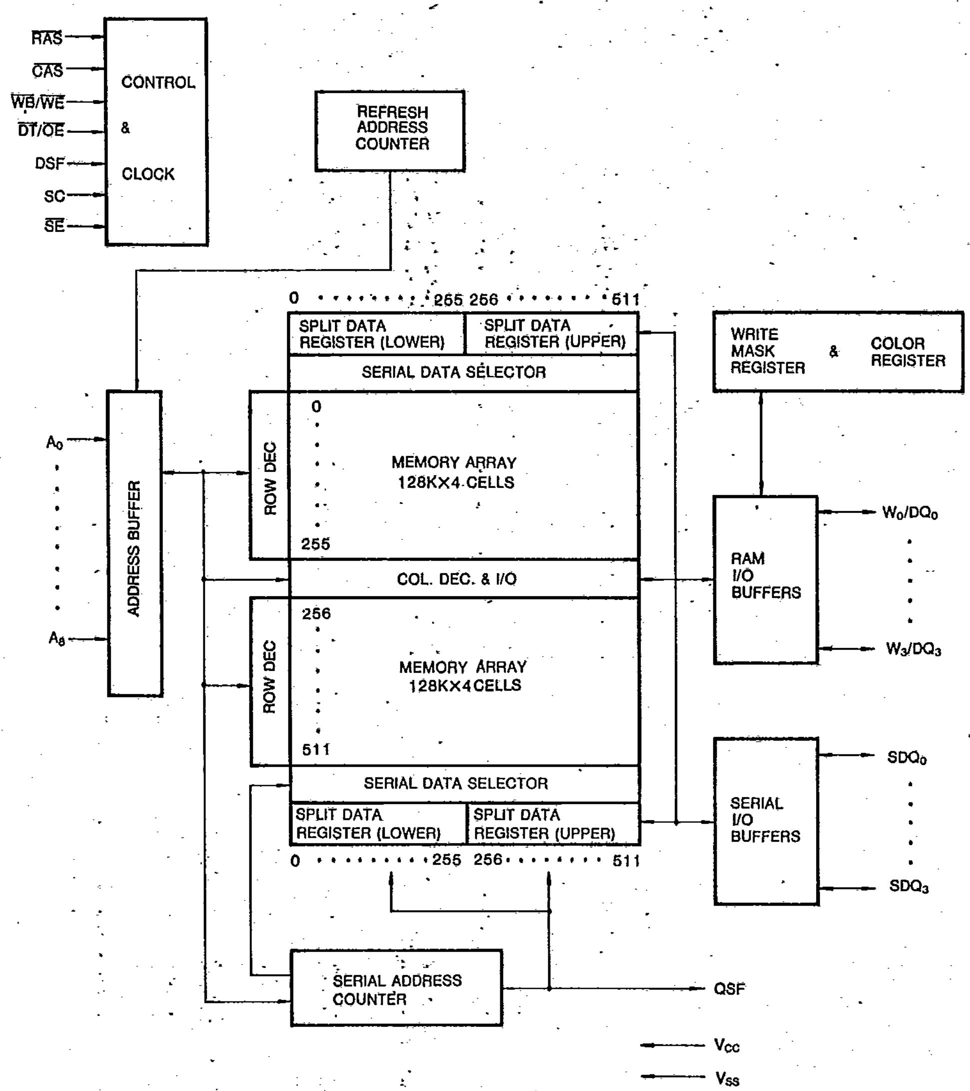
FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

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DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (Ram Port)	Sam port	Symbol	KM424C257			Unit
			−8	−10	−12	
Operating Current* (RAS and CAS Cycling @ t_{RC}=min)	Standby	I_{CC1}	80	70	60	mA
	Active	I_{CC1} A	120	110	100	mA
Standby Current (RAS=CAS=V_{IH})	Standby	I_{CC2}	10	10	10	mA
	Active	I_{CC2} A	40	40	40	mA
RAS Only Refresh Current* (CAS=V_{IH}, RAS Cycling @ t_{RC}=min)	Standby	I_{CC3}	80	70	60	mA
	Active	I_{CC3} A	120	110	100	mA
Fast Page Mode Current* (RAS=V_{IL}, CAS Cycling t_{PC}=min)	Standby	I_{CC4}	60	50	40	mA
	Active	I_{CC4} A	100	90	80	mA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @ t_{RC}=min)	Standby	I_{CC5}	80	70	60	mA
	Active	I_{CC5} A	120	110	100	mA
Data Transfer Current* (RAS and CAS Cycling @ t_{RC}=min)	Standby	I_{CC6}	110	100	90	mA
	Active	I_{CC6} A	150	140	130	mA
Flash Write Cycle (RAS and CAS Cycling @ t_{RC}=min)	Standby	I_{CC7}	80	70	60	mA
	Active	I_{CC7} A	120	110	100	mA
Block Write Cycle (RAS and CAS Cycling @ t_{RC}=min)	Standby	I_{CC8}	90	80	70	mA
	Active	I_{CC8} A	130	120	110	mA
Color Register Load or Read Cycle (RAS and CAS Cycling @t_{RC}=min)	Standby	I_{CC9}	80	70	60	mA
	Active	I_{CC9} A	120	110	100	mA

*NOTE: Real values are dependent on output loading and cycle rates. Specified values are obtained with the output open, I_{CC} is specified as average current.

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts.)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level (RAM $I_{OH}=-5mA$, SAM $I_{OH}=-2mA$)	V_{OH}	2.4	—	V
Output Low Voltage Level (RAM $I_{OL}=4.2mA$, SAM $I_{OL}=2mA$)	V_{OL}	—	0.4	V

CAPACITANCE ($t_A=25°C$)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	—	7	pF
Input/Output Capacitance (W_0/DQ_0-W_3/DQ_3)	C_{DQ}	—	7	pF
Input/Output Capacitance (SDQ_0-SDQ_3)	C_{SDQ}	—	7	pF
Output Capacitance (QSF)	C_{QSF}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

Parameter	Symbol	KM424C257-8		KM424C257-10		KM424C257-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		220		ns	
Read-modify-write cycle time	t_{RWC}	205		245		295		ns	
Fast page mode cycle time	t_{PC}	50		60		75		ns	
Fast page mode read-modify-write	t_{PRWC}	105		125		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	4
Access time from column address	t_{AA}		40		50		60	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	35	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20		25		30		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	5,6
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	20	60	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM424C257-8		KM424C257-10		KM424C257-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		15		20		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		15		20		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		20		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	65		75		85		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	9
Write command hold time	t_{WCH}	15		20		25		ns	
Write command holod referenced to $\overline{RAS}$	t_{WCR}	65		75		85		ns	
Write command pulse width	t_{WP}	20		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		30		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		20		25		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	65		75		85		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	50		60		70		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	110		135		160		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	70		85		100		ns	8
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	15		20		25		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from output enable	t_{OEA}		20		25		30	ns	
Output enable to data input delay	t_{OED}	15		20		25		ns	
Output buffer turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	7
Output enable command hold time	t_{OEH}	20		25		30		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	15		20		25		ns	
DSF set-up time referenced to $\overline{RAS}$ (I)	t_{FSR}	0		0		0		ns	

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM424C257-8		KM424C257-10		KM424C257-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DSF hold time referenced to $\overline{RAS}$ (I)	t_{FHR}	65		75		85		ns	
DSF hold time referenced to $\overline{RAS}$ (II)	t_{RFH}	15		15		20		ns	
DSF set-up time referenced to $\overline{CAS}$	t_{FSC}	10		10		10		ns	
DSF hold time referenced to $\overline{CAS}$	t_{CFH}	15		15		20		ns	
Write per bit mask data set-up	t_{MS}	0		0		0		ns	
Write per bit mask data hold	t_{MH}	15		20		25		ns	
$\overline{DT}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	15		15		20		ns	
$\overline{DT}$ low set-up time	t_{TLS}	0		0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	15		15		20		ns	
$\overline{DT}$ low hold ref to $\overline{RAS}$ (real time read transfer)	t_{RTH}	70		80		95		ns	
$\overline{DT}$ low hold ref to $\overline{CAS}$ (real time read transfer)	t_{CTH}	25		30		35		ns	
$\overline{DT}$ low hold ref to Col. Address (Real time read transfer)	t_{ATH}	30		35		40		ns	
$\overline{SE}$ set-up referenced to $\overline{RAS}$	t_{ESR}	0		0		0		ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{REH}	10		15		20		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay time	t_{TRD}	10		10		15		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay time	t_{TCD}	10		10		15		ns	
$\overline{DT}$ precharge time	t_{TP}	25		30		35		ns	
$\overline{RAS}$ to first SC delay (read transfer)	t_{RSD}	80		100		120		ns	
$\overline{CAS}$ to first SC delay (read transfer)	t_{CSD}	40		50		60		ns	
Col. Addr. to first SC delay (read transfer)	t_{ASD}	45		55		65		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		10		ns	
$\overline{DT}$ to first SC delay (read transfer)	t_{TSD}	10		15		20		ns	
Last SC to $\overline{RAS}$ set-up (serial input)	t_{SRS}	25		30		40		ns	
$\overline{RAS}$ to first SC delay time (serial input)	t_{SRD}	25		30		40			
$\overline{RAS}$ to serial input delay	t_{SDD}	40		50		60		ns	
Serial out buffer turn-off delay from $\overline{RAS}$ (pseudo write transfer)	t_{SDZ}	10	40	10	50	10	60	ns	7
Serial input to first SC delay	t_{SZS}	0		0		0		ns	
SC cycle time	t_{SCC}	25		30		40		ns	
SC pulse width (SC high time)	t_{SC}	10		10		15		ns	
SC precharge (SC low time)	t_{SCP}	10		10		15		ns	
Access time from SC	t_{SCA}		20		25		35	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Serial input set-up time	t_{SDS}	0		0		0		ns	
Serial input hold time	t_{SDH}	15		20		25		ns	
Access time from $\overline{SE}$	t_{SEA}	20		25		35		ns	4

AC CHARACTERISTICS (Continued)

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Parameter	Symbol	KM424C257-8		KM424C257-10		KM424C257-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{SE}$ pulse width	t_{SE}	20		25		35		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		25		35		ns	
Serial out buffer turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	20	0	30	ns	7
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		0		ns	
Serial write enable set-up time	t_{SWS}	5		5		10		ns	
Serial write enable hold time	t_{SWH}	15		15		20		ns	
Serial write disable set-up time	t_{SWIS}	5		5		10		ns	
Serial write disable hold time	t_{SWIH}	15		15		20		ns	
Split transfer set-up time	t_{STS}	30		30		40		ns	
Split transfer hold time	t_{STH}	30		30		40		ns	
SC-QSF delay time	t_{SQD}		20		25		35	ns	
$\overline{DT}$-QSF delay time	t_{TQD}		40		50		60	ns	
$\overline{CAS}$-QSF delay time	t_{CQD}		40		50		60	ns	
$\overline{RAS}$-QSF delay time	t_{RQD}		80		100		120	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved ($\overline{DT}/\overline{OE}$=HIGH). If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. RAM port outputs are measured with a load equivalent to 2 TTL loads and 100pF.
4. SAM port outputs are measured with a load equivalent to 2 TTL loads and 50pF. Dout comparator level: V_{OH}/V_{OL}=2.0/0.8V.
5. Operation within the $t_{RCD(max)}$ limit insures the $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
7. The parameters, $t_{OFF(max)}$, $t_{OEZ(max)}$, $t_{SDZ(max)}$ and $t_{SEZ(max)}$, define the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RCD(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

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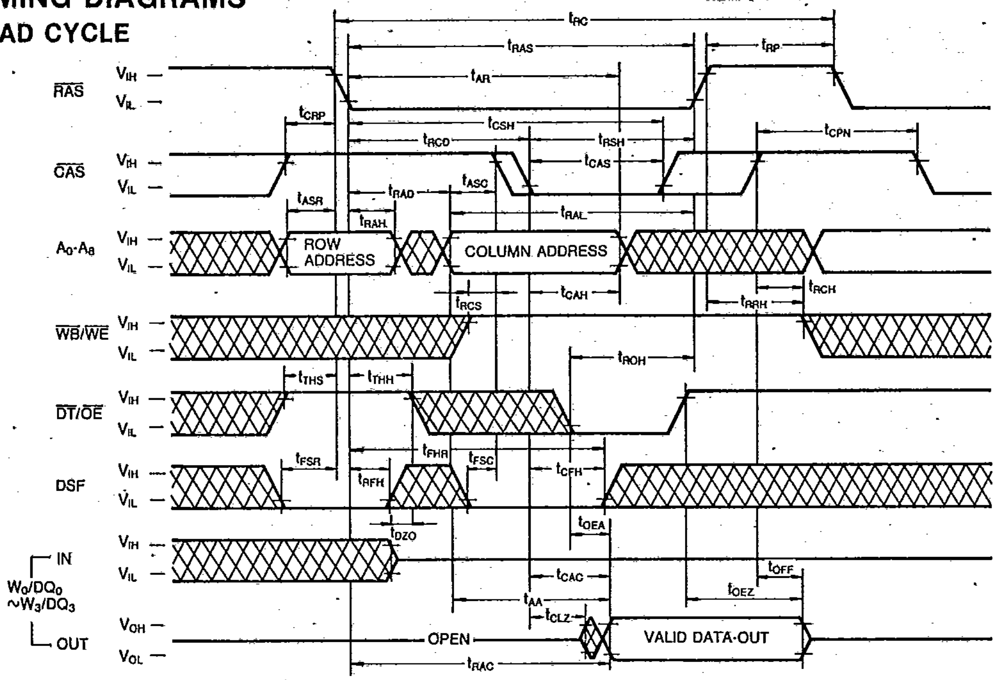
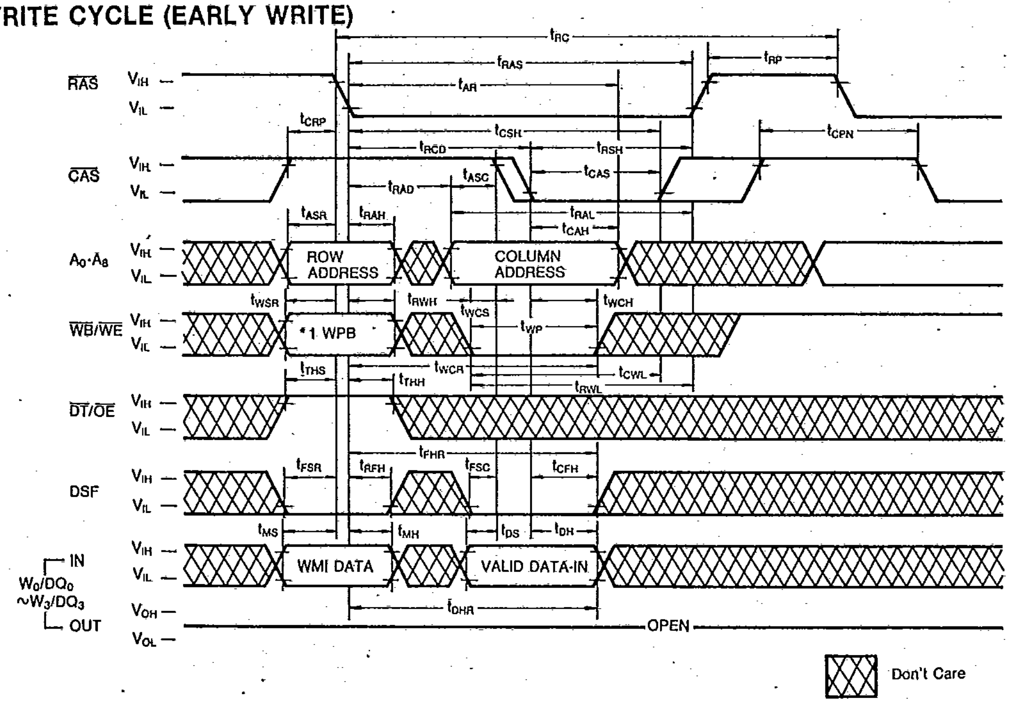
TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)



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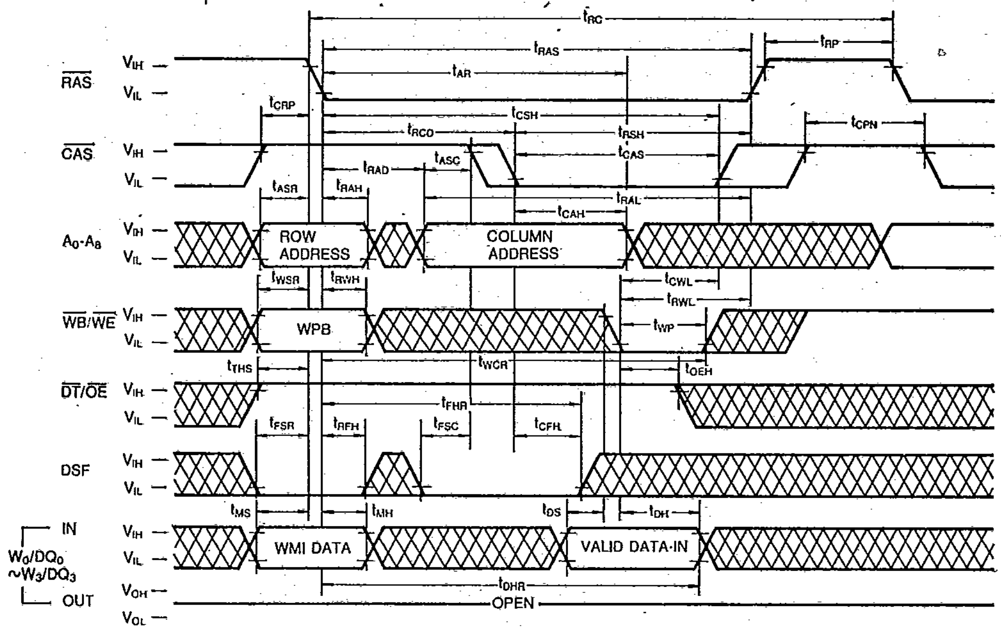
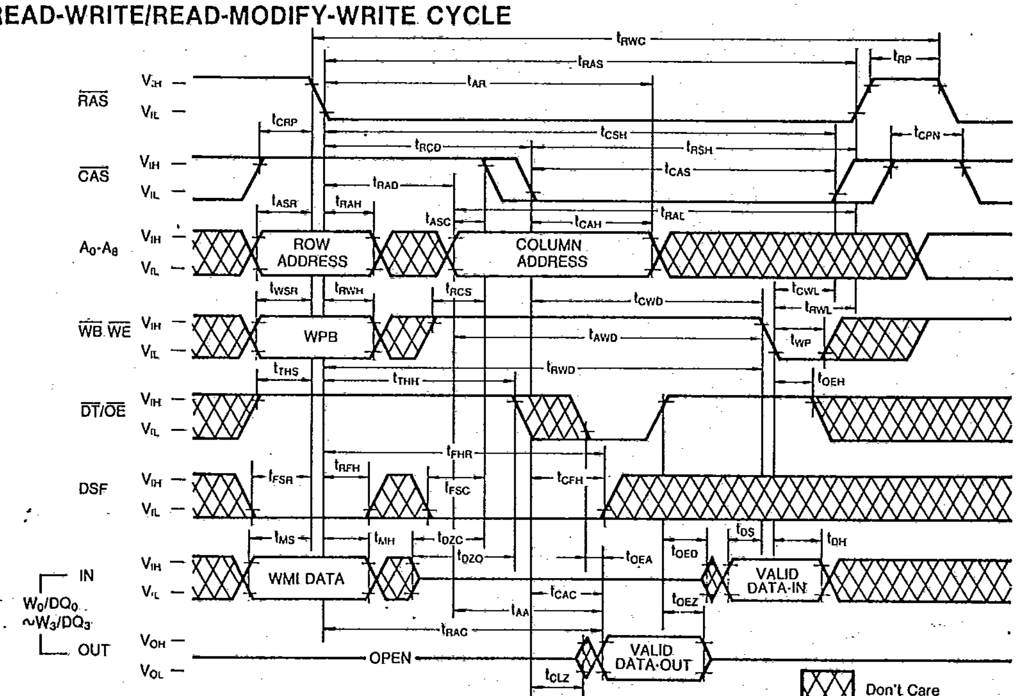
TIMING DIAGRAMS (Continued)

WRITE CYCLE (OE CONTROLLED WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE



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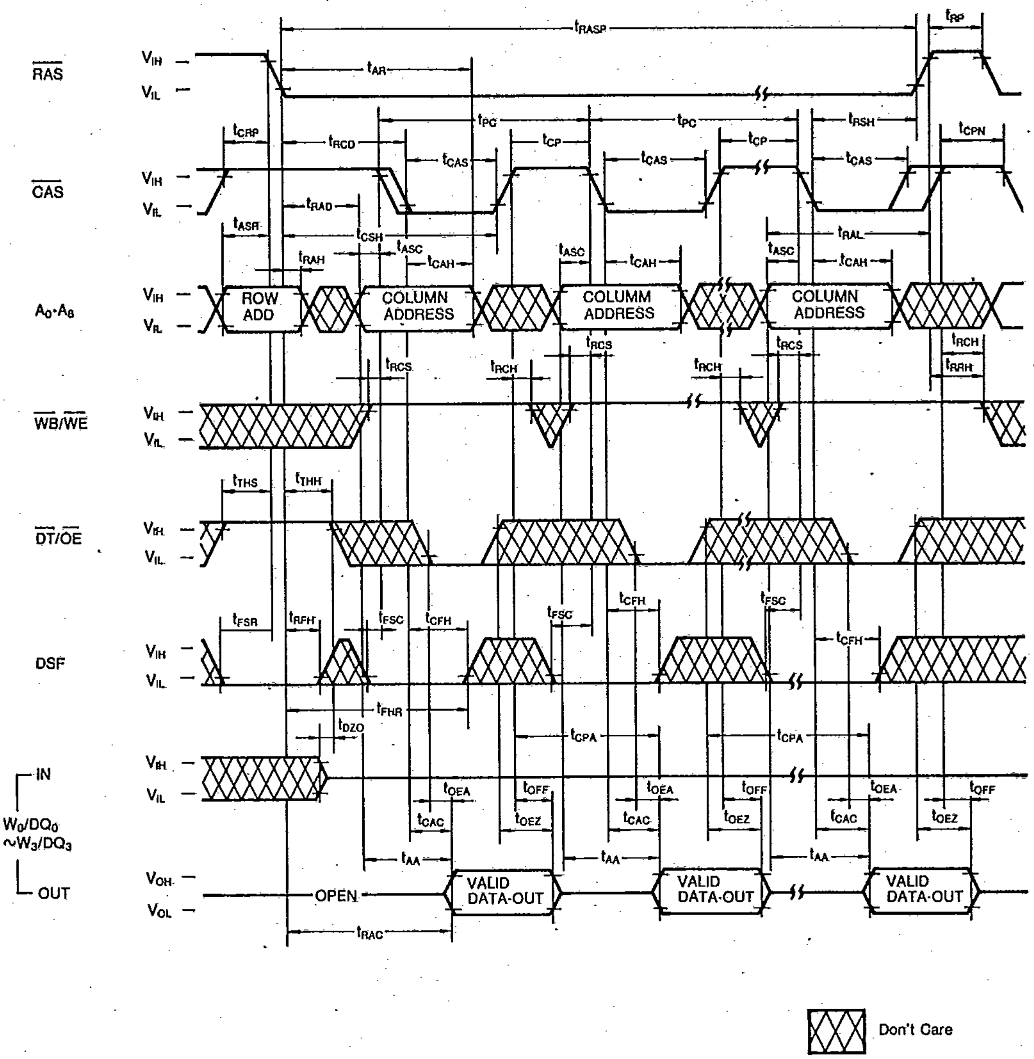
TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



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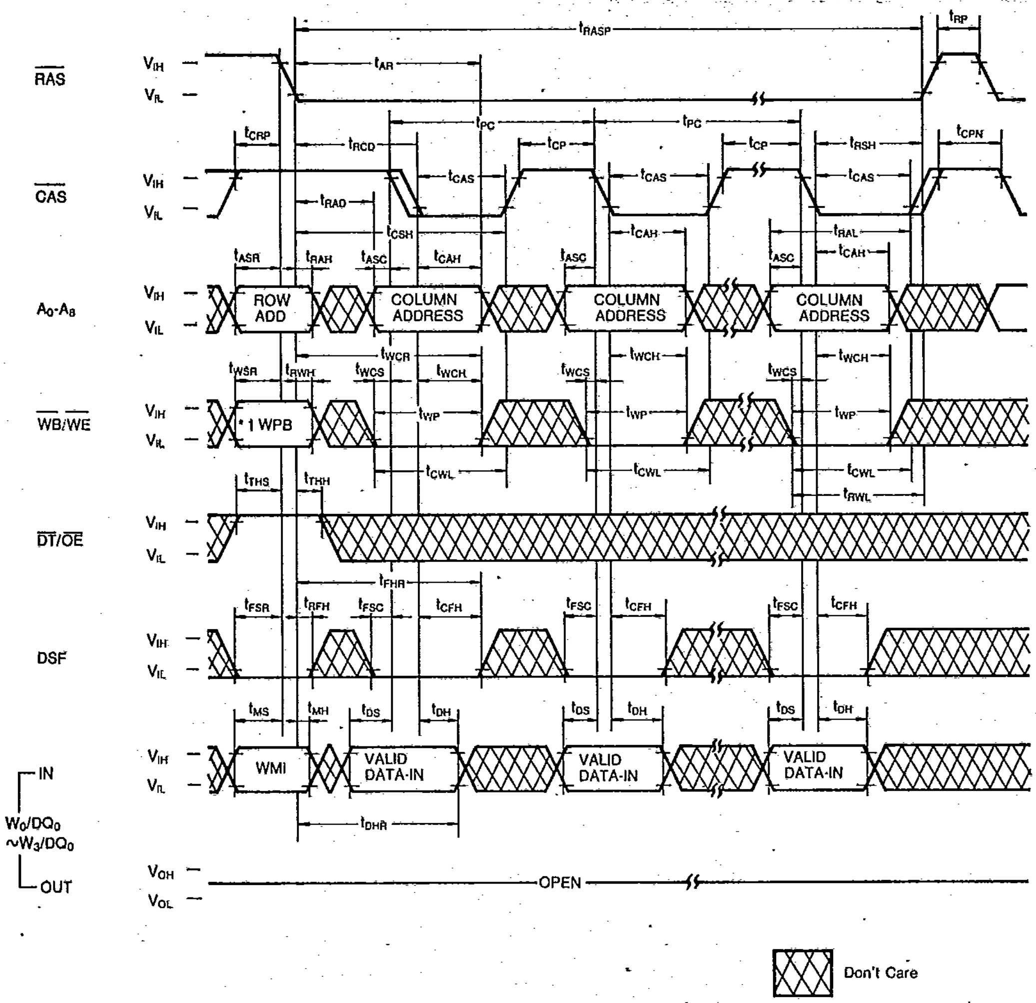
TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE (EARLY WRITE)



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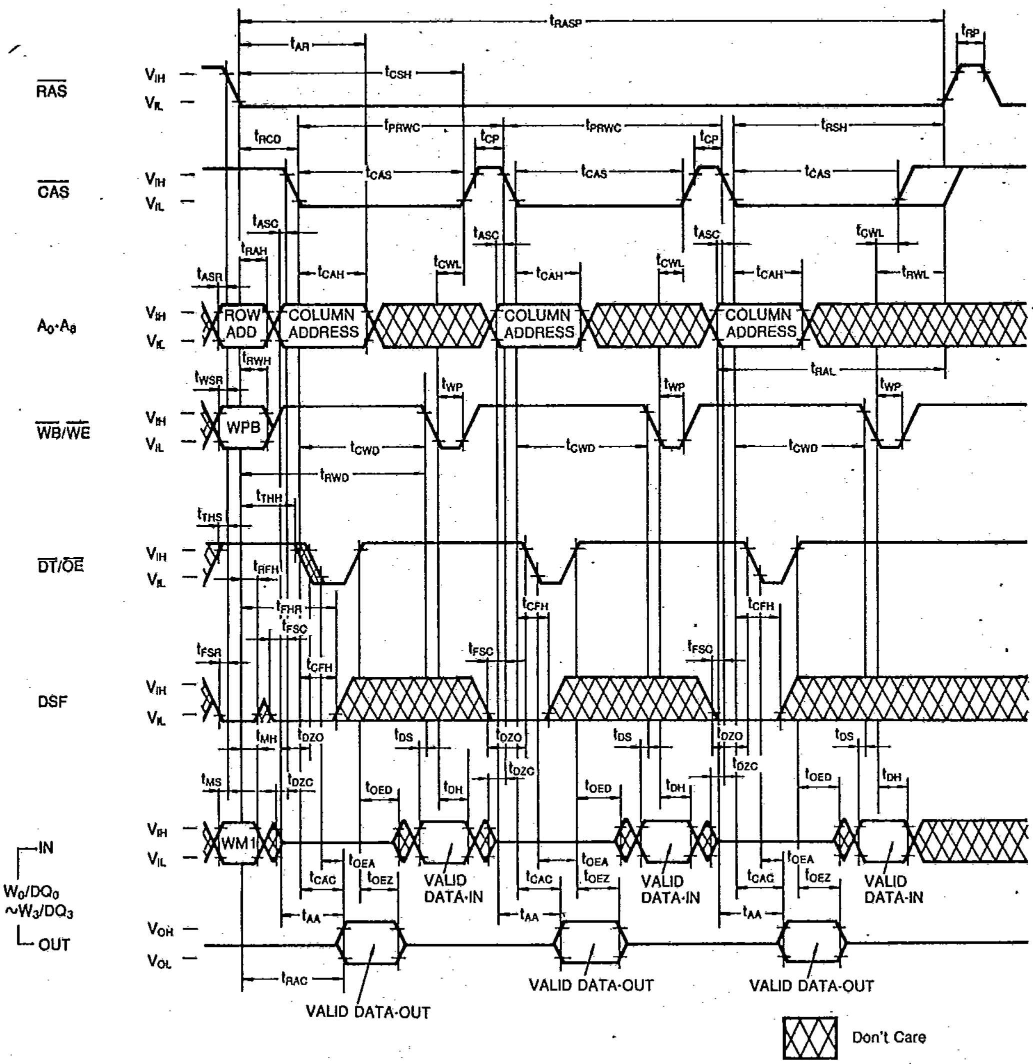
TIMING DIAGRAMS (Continued)

PAGE MODE READ-MODIFY-WRITY CYCLE



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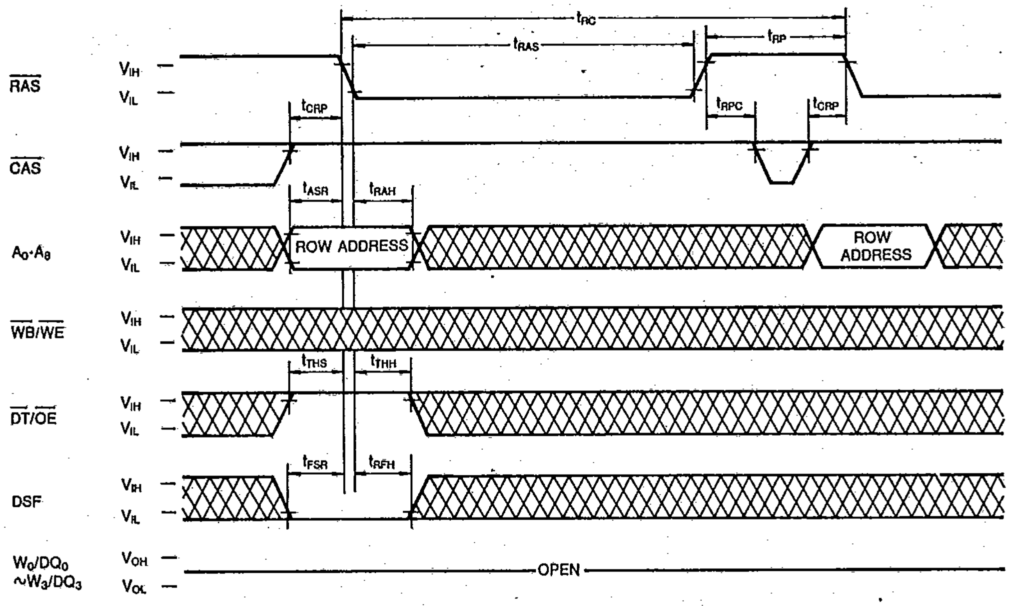
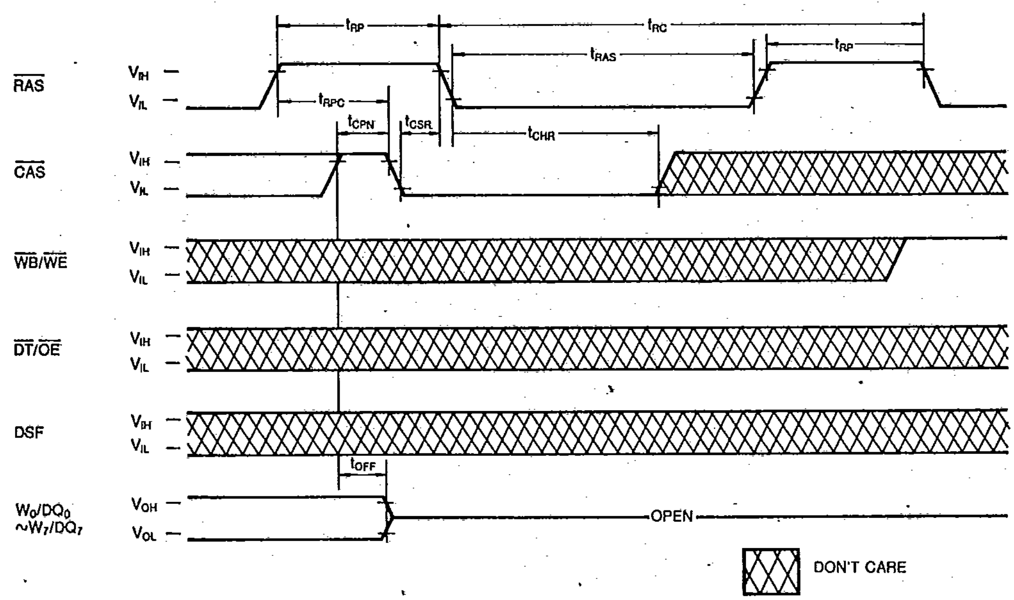
TIMING DIAGRAMS (Continued)

RAS ONLY REFRESH CYCLE

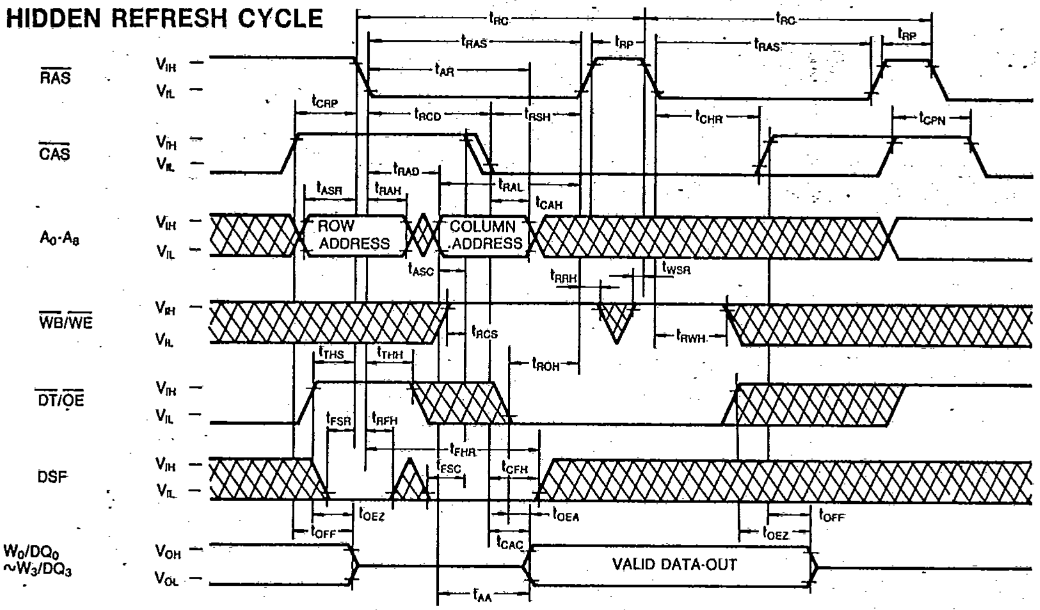


CAS BEFORE RAS REFRESH

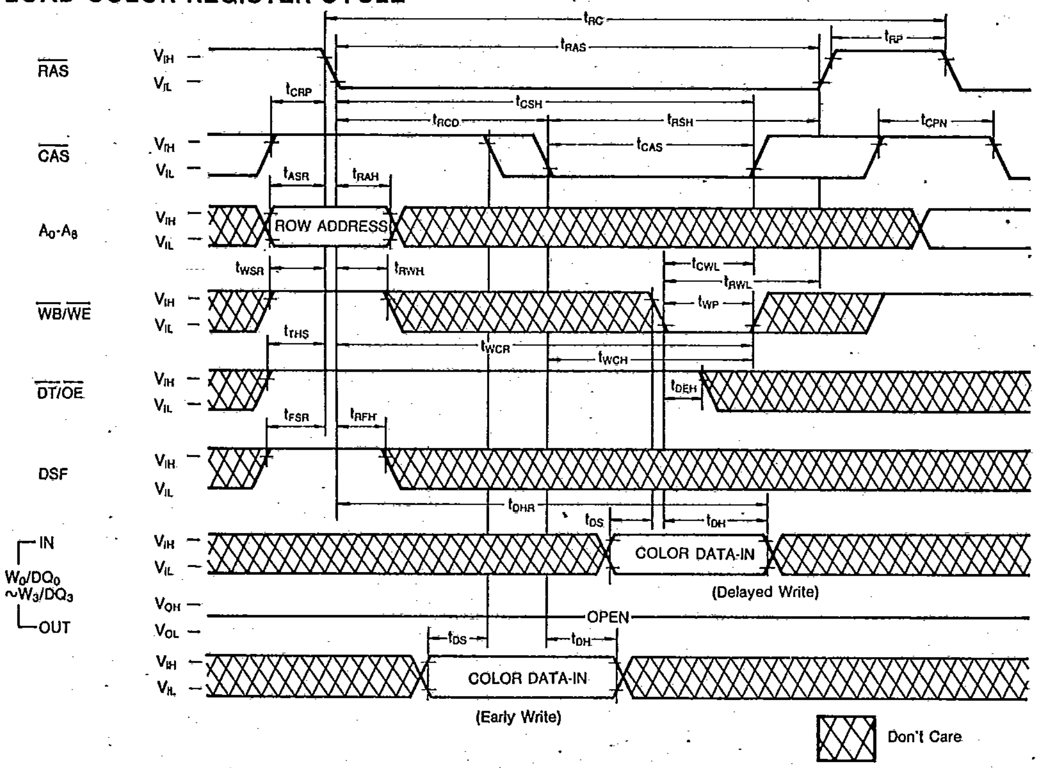


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



LOAD COLOR REGISTER CYCLE



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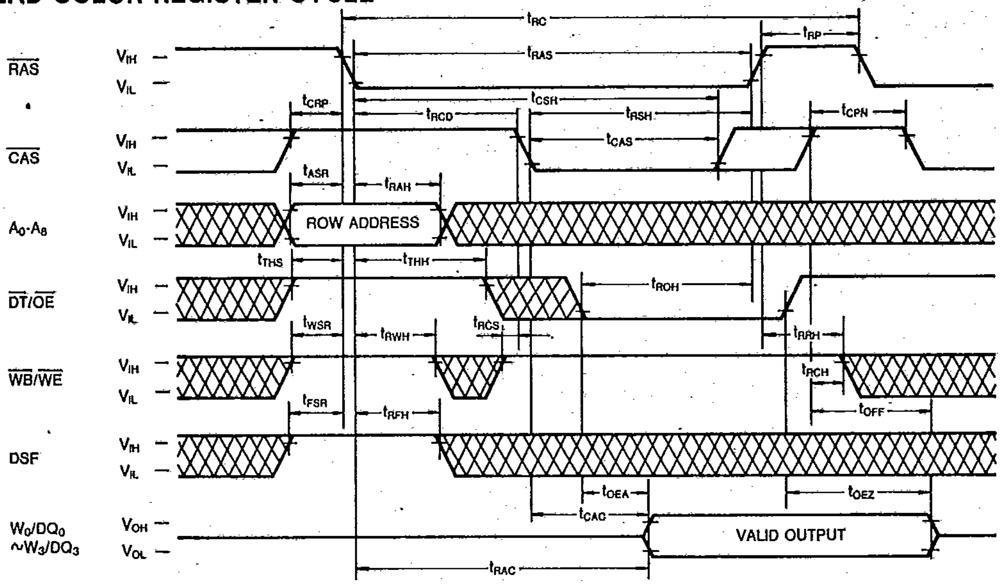
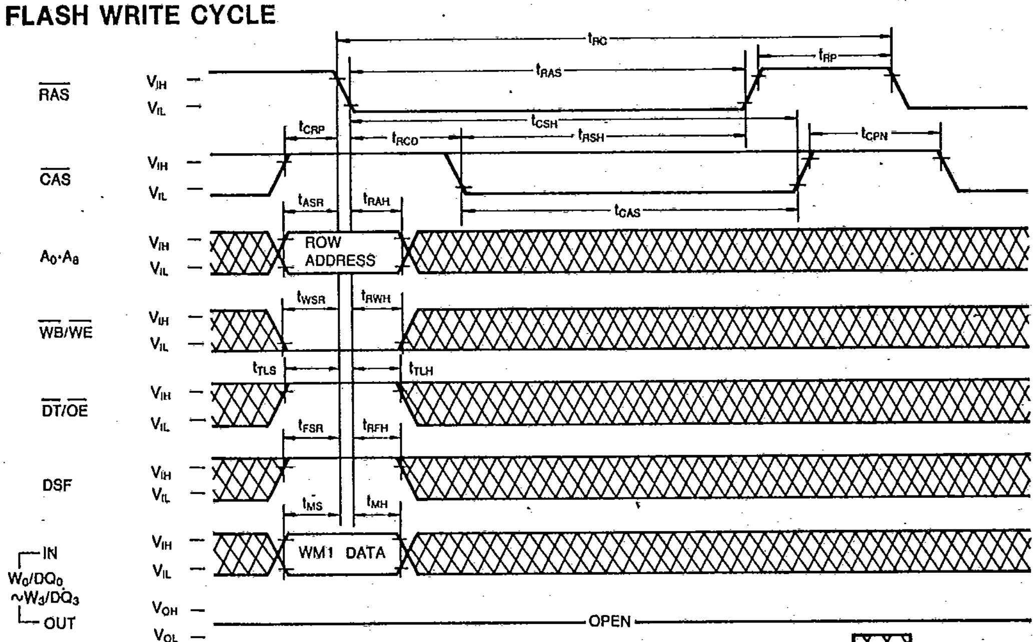
TIMING DIAGRAMS (Continued)

READ COLOR REGISTER CYCLE



FLASH WRITE CYCLE



WM1 DATA	CYCLE
O	Flash write Disable
I	Flash write Enable

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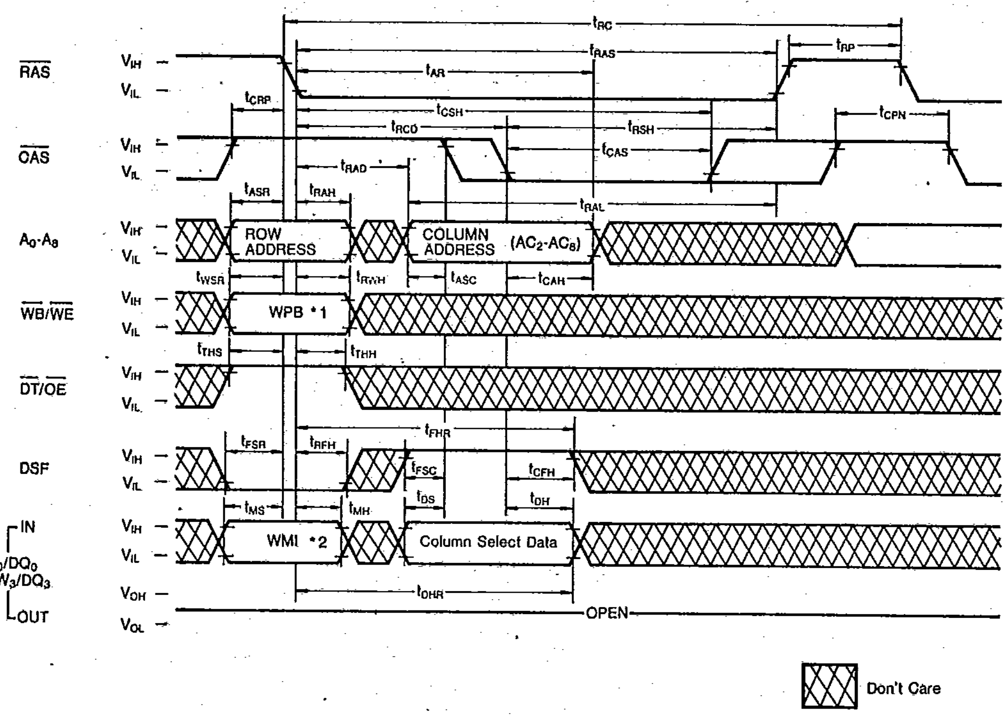
TIMING DIAGRAMS (Continued)

BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W_0/DQ_0-W_3/DQ_3	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 Data: 0: Write Disable
1: Write Enable

COLUMN SELECT DATA

W_0/DQ_0 — Column 0 (A_{IC}=0, A_{OC}=0)
W_1/DQ_1 — Column 1 (A_{IC}=0, A_{OC}=1)
W_2/DQ_2 — Column 2 (A_{IC}=1, A_{OC}=0)
W_3/DQ_3 — Column 3 (A_{IC}=1, A_{OC}=1)

Wn/DQn = 0: Disable
= 1: Enable

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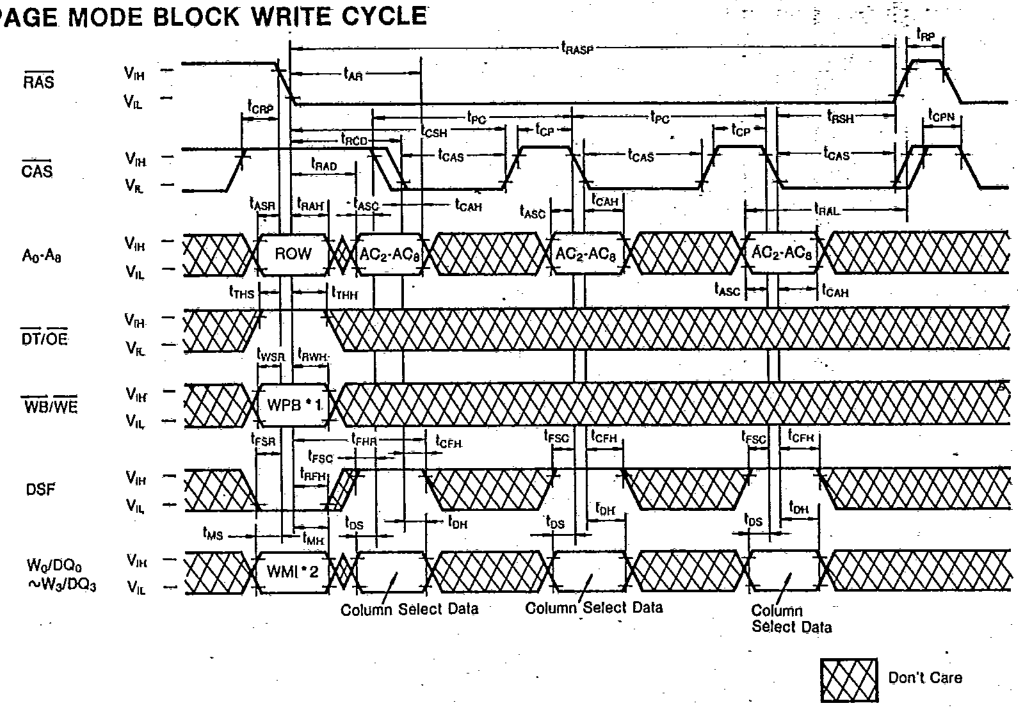
TIMING DIAGRAMS (Continued)

PAGE MODE BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W_0/DQ_0-W_3/DQ_3	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 Data: 0: Write Disable
1: Write Enable

COLUMN SELECT DATA
W_0/DQ_0 — Column 0 ($A_{IC}=0$, $A_{OC}=0$)
W_1/DQ_1 — Column 1 ($A_{IC}=0$, $A_{OC}=1$)
W_2/DQ_2 — Column 2 ($A_{IC}=1$, $A_{OC}=0$)
W_3/DQ_3 — Column 3 ($A_{IC}=1$, $A_{OC}=1$)

Wn/DQn
= 0: Disable
= 1: Enable

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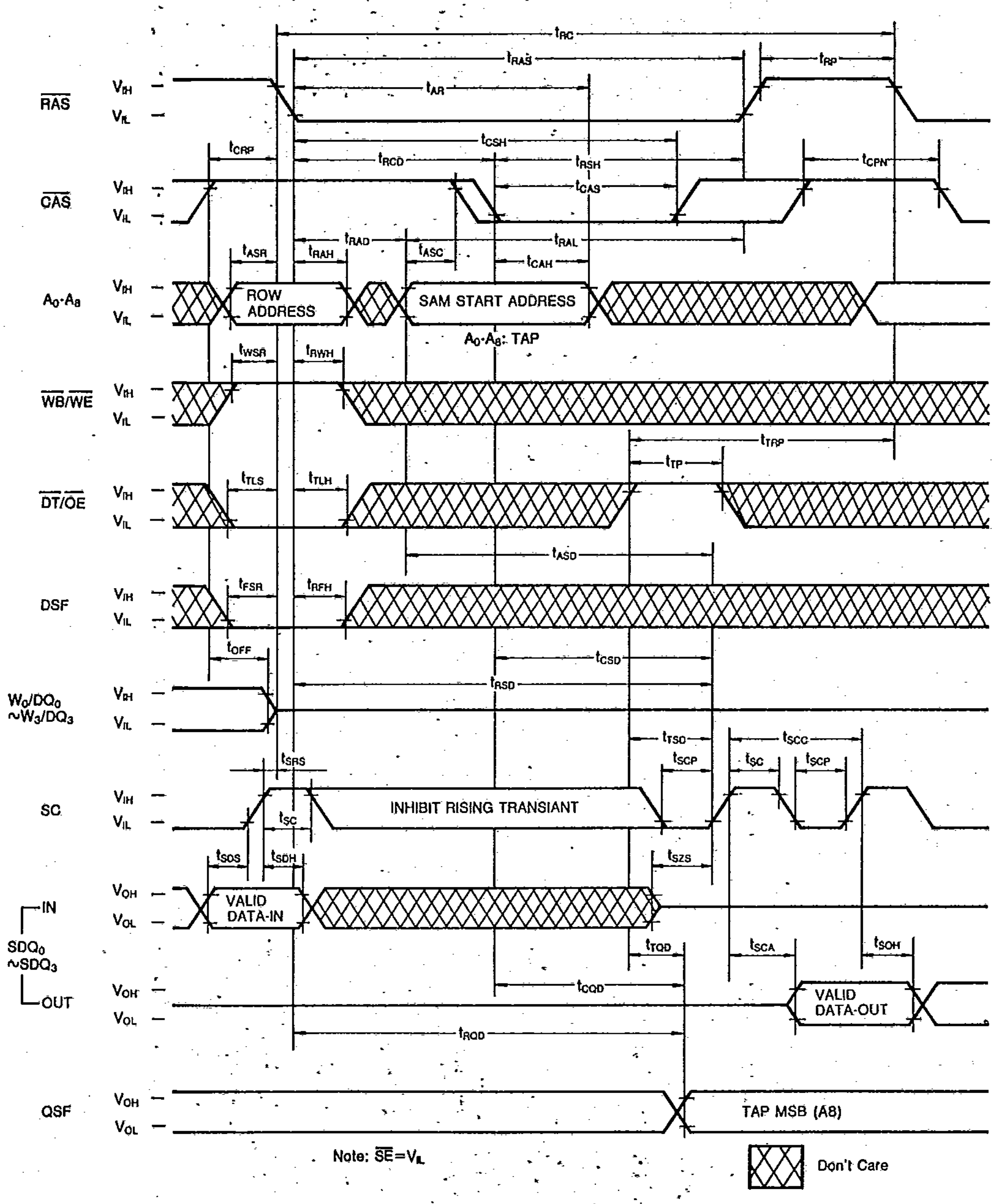
TIMING DIAGRAMS (Continued)

READ TRANSFER CYCLE



TIMING DIAGRAMS (Continued)

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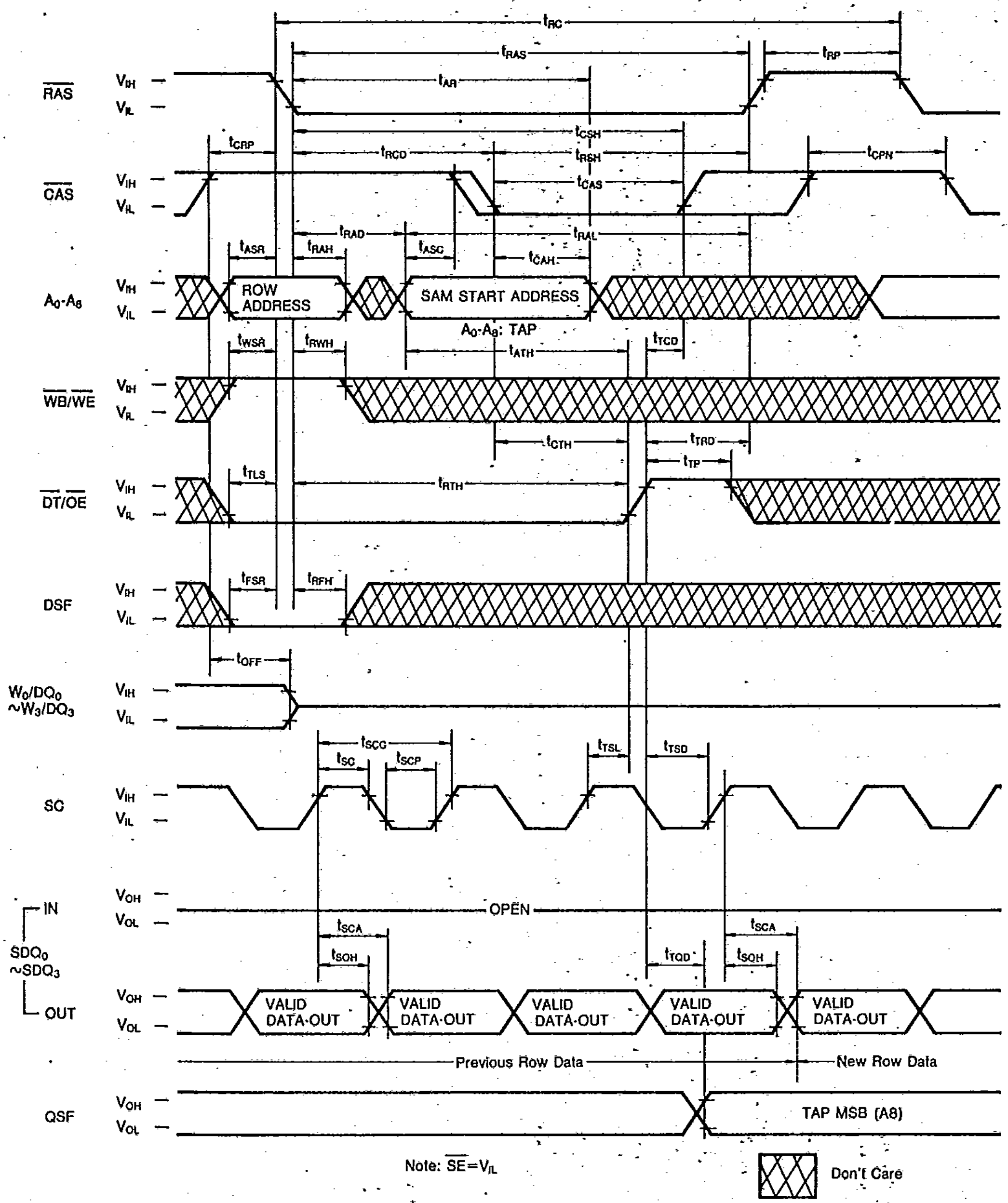
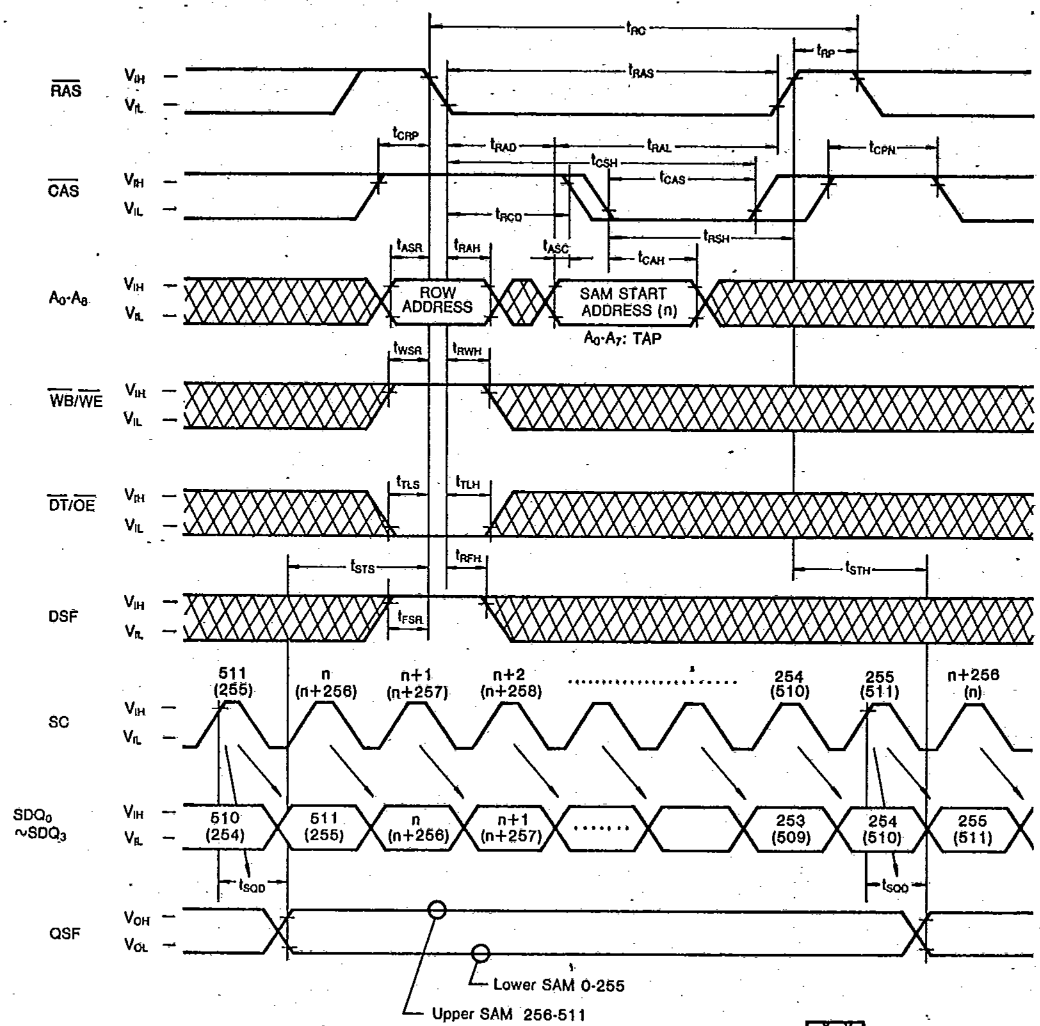
REAL TIME READ TRANSFER CYCLE



4

TIMING DIAGRAMS (Continued)

SPLIT READ TRANSFER CYCLE

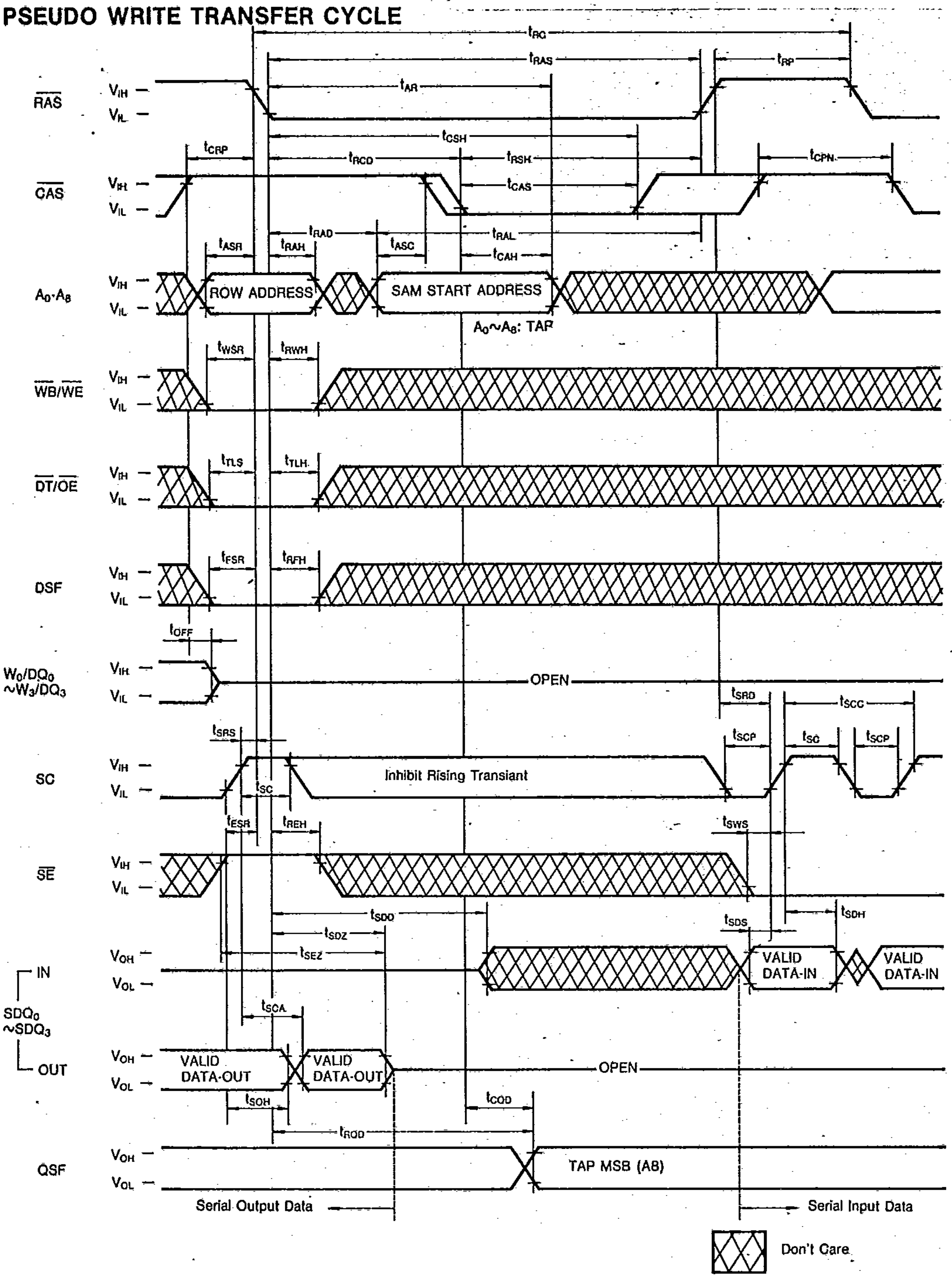


Note: $\overline{SE}=V_{IL}$

Dont' Care

TIMING DIAGRAMS (Continued)

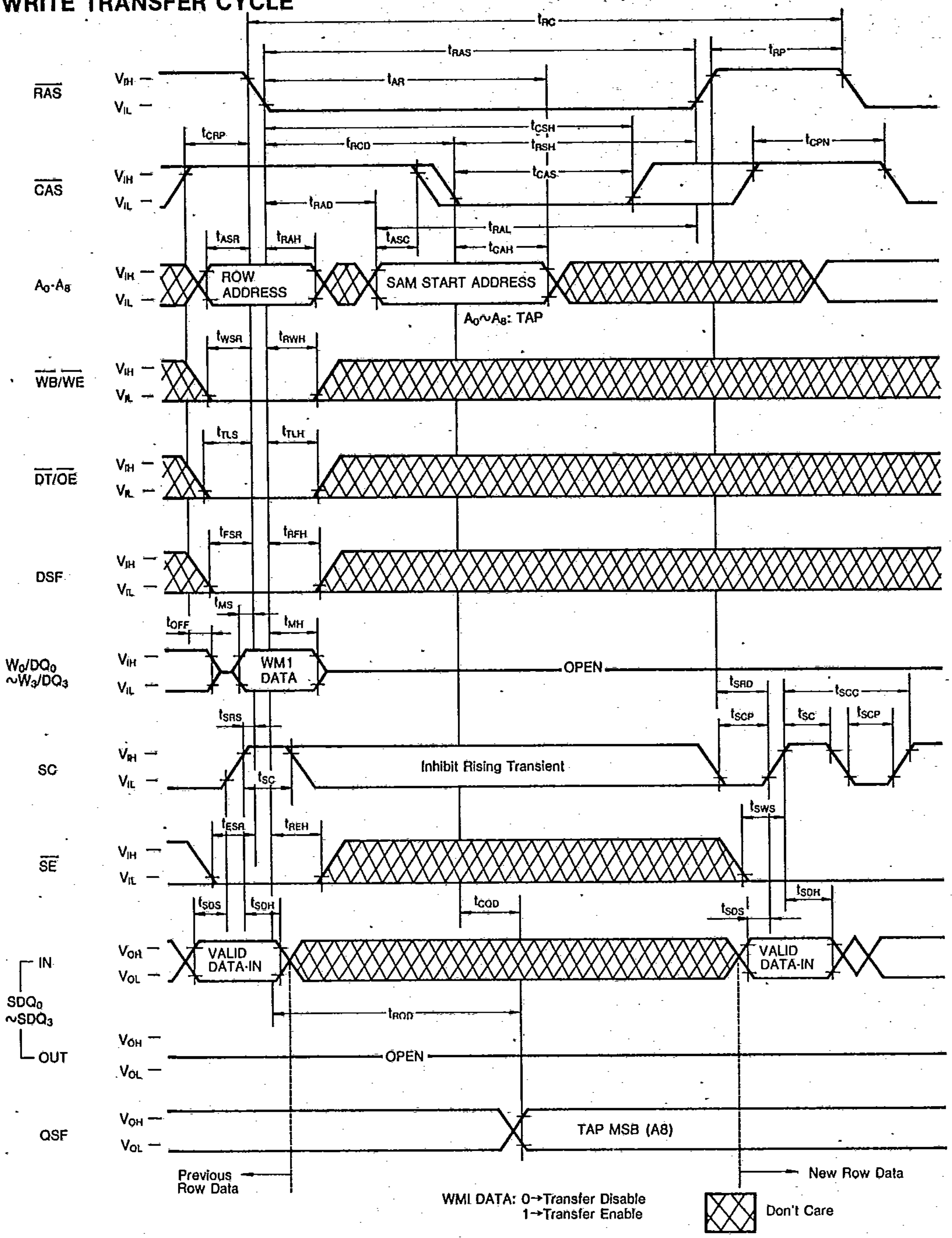
PSEUDO WRITE TRANSFER CYCLE



4

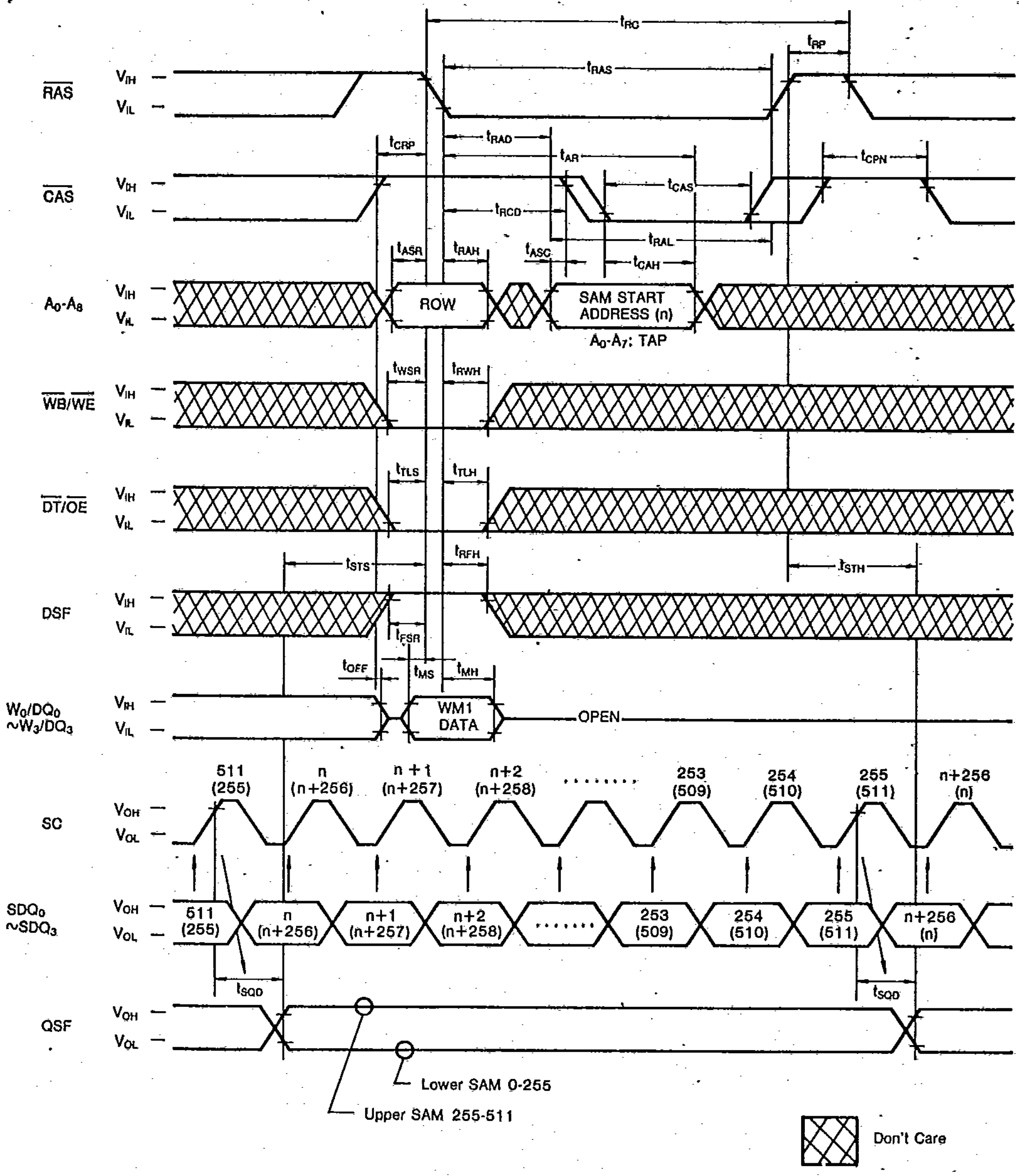
TIMING DIAGRAMS (Continued)

WRITE TRANSFER CYCLE



TIMING DIAGRAMS (Continued)

SPLIT WRITE TRANSFER CYCLE



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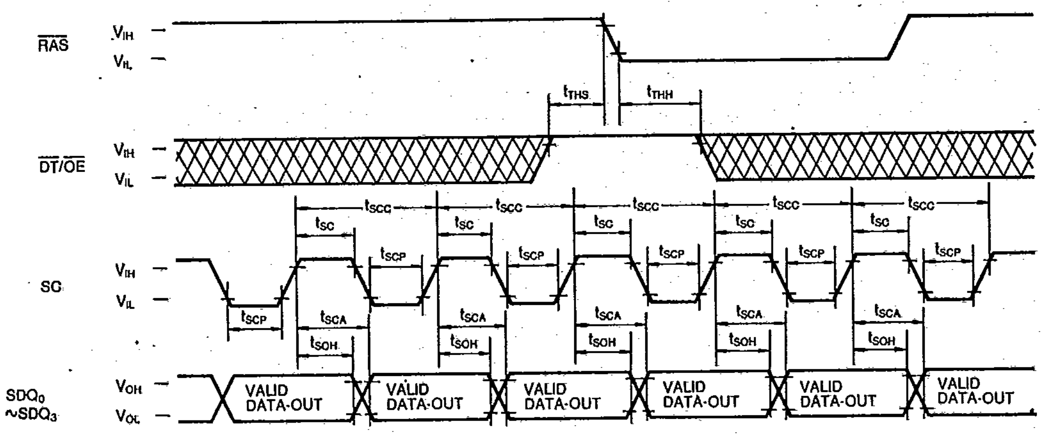
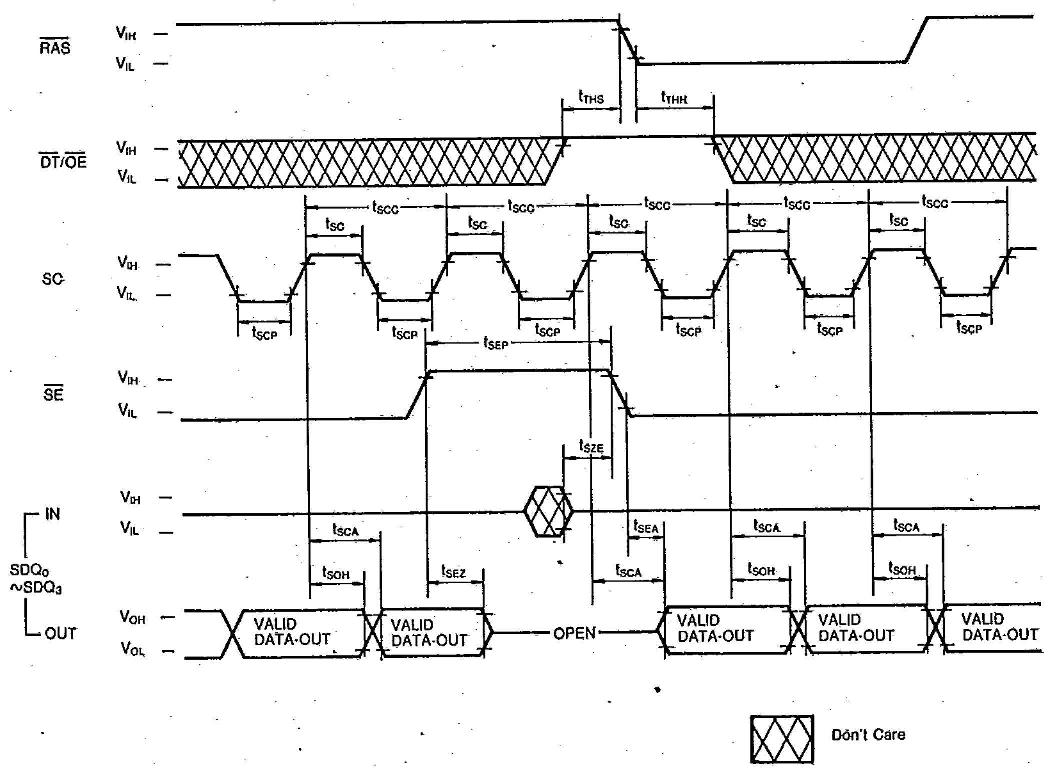
SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



Note: $\overline{SE}$ = V_{IL}

SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



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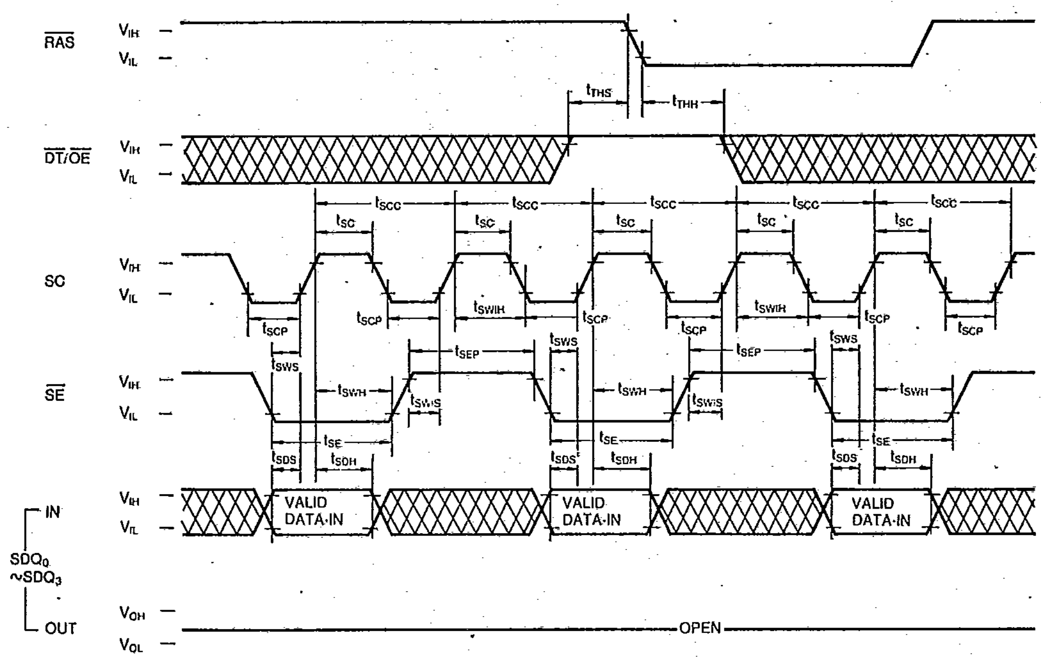
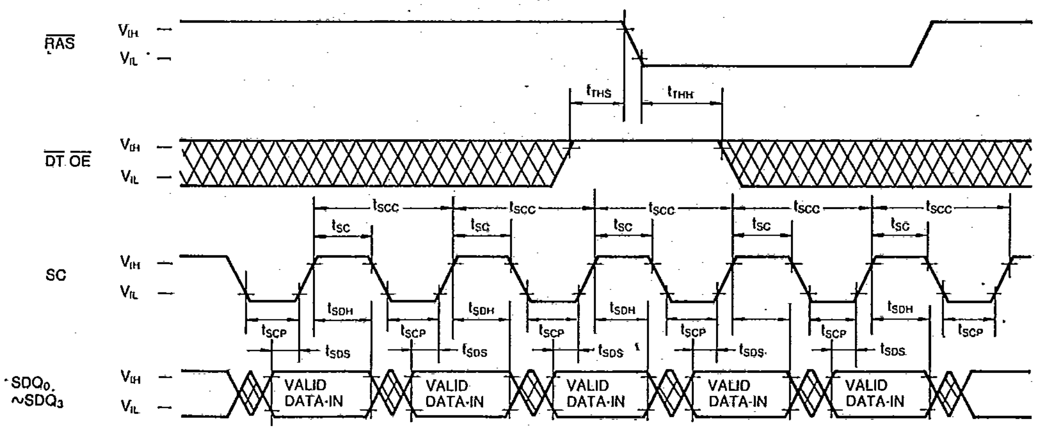
TIMING DIAGRAMS (Continued)

SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



Note: $\overline{SE} = V_{IL}$

Don't Care

DEVICE OPERATIONS

The KM424C257 contains 1,048,576 memory locations. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM424C257 has only 0 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM424C257 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM424C257 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM424C257 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}.

The KM424C257 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Write

The KM424C257 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{WB}/\overline{WE}$, whichever is later.

Fast Page Mode

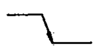
Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Write-Per-Bit

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/DQi pins is latched onto the write-mask register (WM1). When a '0' is sensed on any of the Wi/DQi pins, their corresponding write circuits are disabled and new data will not be written.

When a '1' is sensed on any of the Wi/DQi pins, their corresponding write circuits will remain enabled so that new data is written. The write mask data is valid for only one cycle the truth table of the write-per-bit function are shown in Table 2.

Table 2. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/DQi	FUNCTION
	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	WRITE MASK

DEVICE OPERATIONS (Continued)

Block Write

A block write cycle is performed by holding CAS, DT/OE "high" and DSF "Low" at the falling edge of RAS and by holding DSF "high" at the falling edge of CAS. The state of the WB/WE at the falling edge of RAS determines whether or not the I/O data mask is enabled as write per bit function. At the falling edge of CAS, the starting column address pointer and column mask data must be provided. During a block write cycle, the 2 least significant column address (A0 and A1) are internally controlled and only the seven most significant column address (A2-A8) are latched at the falling edge of CAS.

Flash Write

Flash write is mainly used for fast clear operations in frame buffer applications. A flash write cycle is performed by holding CAS "high", WB/WE "Low" and DSF "high" at the falling edge of RAS. The mask data must also be provided on the Wi/DQi lines at the falling edge of RAS in order to enable the flash write operation for selected I/O blocks.

Data Output

The KM424C257 has a three state output buffers which are controlled by CAS and DT/OE. When either CAS or DT/OE is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of CAS. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until CAS returns high. This is true even if a new RAS cycle occurs (as in hidden refresh). Each of the KM424C257 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modity-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write, Read Color Register.

Refresh

The data in the KM424C257 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 2048 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

RAS-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while CAS remains high. This cycle must be repeated for each of the 512 row address, (A_0-A_8).

CAS-before-RAS Refresh: The KM424C257 has CAS-before-RAS on-chip refresh capability that eliminates the need for external refresh addresses. If CAS is held low for the specified set up time (t_{SCR}) before RAS goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next CAS-before-RAS refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the CAS active time and cycling RAS. The KM424C257 hidden refresh cycle is actually a CAS-before-RAS refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM424C257 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only refresh or CAS-before-RAS refresh is the preferred method.

Transfer Operation

1. Normal Write/Read Transfer (SAM→RAM/RAM→SAM.).
2. Pseudo Write Transfer (Switches serial port from serial Read to serial Write. No actual data transfer takes place between the RAM and the SAM.).
3. Real Time Read Transfer (On the fly Read Transfer operation).
4. Split Write/Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred from/to the SAM while the other half is write to/read from the SDQ pins.).

Read-Transfer Cycle

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding CAS high, DT/OE low and WB/WE high at the falling edge of RAS. The row address

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DEVICE OPERATIONS (Continued)

selected at the falling edge of $\overline{RAS}$ determines the RAM row to be trasferred into the SAM.

The actual data transfer completed at the rising edge of data transfer. A psuedo write transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo write transfer cycle must be performed after a read transfer cycle if

Table 3. Truth table for Transfer operation

$\overline{RAS}$ Falling Edge					Function	Transfer Direction	Transfer Data Bits	Sam port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM→SAM	512×4	Input→Output
H	L	L	L	L	Masked Write Transfer	SAM→RAM	512×4	Output→Input
H	L	L	H	L	Pseudo Write Transfer	—	—	Output→Input
H	L	H	*	H	Split Read Transfer	RAM→SAM	256×4	Not Changed
H	L	L	*	H	Split Write Transfer	SAM→RAM	256×4	Not Changed

*: Don't Care

$\overline{DT}/\overline{OE}$. When the transfer is completed, the SDQ lines are set into the otuput mode. In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SDQ lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Write Transfer Cycle

A write transfer cycle consists of loading the content of the SAM data register into a selected row of RAM array. A write transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transfered. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are in the input mode so that serial data synchronized with SC can be loaded. When two consecutive write transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SCP} has seen satisfied, a rising edge of the SC clock until after a specified delay t_{RSD} from the falling edge of $\overline{RAS}$.

Pseudo Write Transfer Cycle

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform the subsequent operation is a write transfer cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{RSD} from the falling edge of $\overline{RAS}$.

Special Function Input (DSF)

In read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split register mode read transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of most significant column address bit (A8) that is strobed in on the falling edge of $\overline{CAS}$. If A8 is high, the transfer is to the high half of the register. If A8 is low, the transfer is to the low half of the register. Use of the split register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{DT}/\overline{OE}$ to the serial clock. The transfer can be to either the active half or the inactive half register. If the transfer is to the active register, with an uninterrupted serial data stream, then the timings t_{TSL} and t_{TSD} must be met.

In write tranfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of a Split Register mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without performing a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

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DEVICE OPERATIONS (Continued)

Split Register Active Status Output (QSF)

QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

Serial Clock (SC)

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SDQ pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9 bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle.

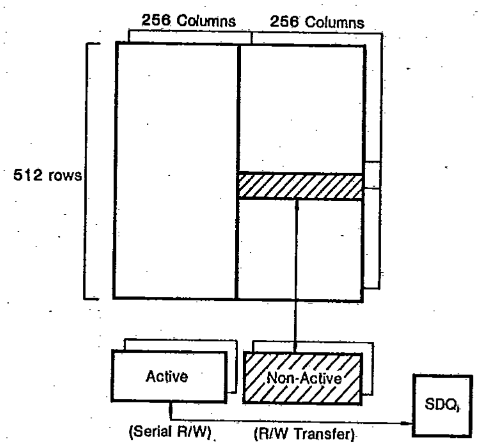
Serial Input/Output (SDQ_0-SDQ_3)

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a pseudo write is performed, the SAM port operation is switched from output mode to input mode. During subsequent write transfer cycle, the SAM port remains in the input mode.

Power-up

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured.

Table 4. SPLIT REGISTER MODE



Active SAM	QSF Level
LOWER SAM	LOW
UPPER SAM	HIGH

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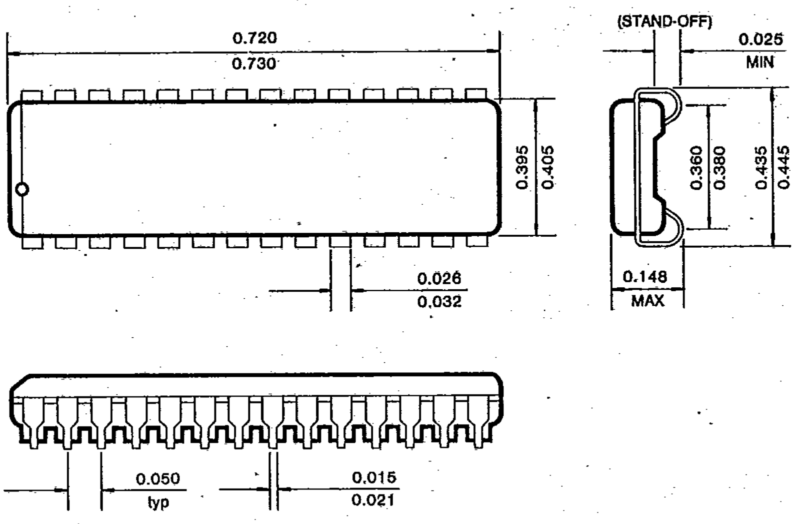
PACKAGE DIMENSIONS

28-PIN PLASTIC SOJ

Units: Inches



28-PIN PLASTIC ZIP