2-WIRE REAL-TIME CLOCK S-35392A

The S-35392A is a low-current-consumption 2-wire CMOS real-time clock IC that features a wide operating voltage range (1.3 V to 5.5 V) and can be driven on a variety of supply voltages, from a main supply to a backup supply. The time keeping current consumption of 0.45 μA and minimum time keeping operation voltage of 1.1 V enable greatly increased battery duration.
In a system that operates on a backup battery, the free register incorporated in the real-time clock can be used for the user backup memory function. The user register can hold data on a supply voltage as low as 1.2 V (min.), so the data stored in the register before the main power supply was cut can be called any time after the voltage is restored.
This product also includes a clock adjustment function that enables wide-ranging correction of deviation in the frequency of the crystal oscillator at a minimum resolution of 1 ppm. Also, by combining this function with a temperature sensor, the clock adjustment value can be set in accordance with changes in the temperature, which makes it possible to realize a clock function that retains a high degree of accuracy regardless of temperature variation.

■ Features

- Low current consumption : 0.45 μA typ. (V_{DD} = 3.0 V, Ta = 25°C)
- Constant 32 kHz clock pulse output (Nch open-drain output)
- Wide operating voltage range : 1.3 to 5.5 V
- Minimum time keeping operation voltage : 1.1 V
- Built-in clock adjustment function
- Built-in free user register
- 2-wire (I^2C-bus) CPU interface
- Built-in alarm interrupter
- Built-in flag generator at power down or power on
- Auto calendar up to the year 2099, automatic leap year calculation function
- Built-in constant voltage circuit
- Built-in 32 kHz crystal oscillator circuit (C_d built in, C_g external)
- Package : SNT-8A
- Lead-free products

■ Applications

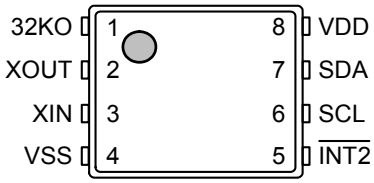
- Digital still cameras
- Digital video cameras
- Electronic power meters
- DVD recorders
- TVs, VCRs
- PHS
- Mobile phones
- Car navigation

■ Package

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A	PH008-A	PH008-A	PH008-A

■ Pin Assignment

SNT-8A
Top view



S-35392A-I8T1G

Figure 1

■ Description of Pins

Table 1

Pin No.	Symbol	Description	Configuration
1	32KO	32,768 Hz constant output pin It constantly outputs clock pulses after power-on. Since clock pulses are output from the crystal oscillator circuit, the clock adjustment function is not reflected.	Nch open-drain output (no protective diode on the side of VDD)
2	XOUT	Crystal oscillator connect pin (32,768 Hz) (C_d built in, C_g external)	–
3	XIN		
4	VSS	Negative power supply pin (GND)	–
5	$\overline{\text{INT2}}$	Interrrupt 2 signal output pin Depending on the mode set by INT1 register_2 and the status register, it outputs low or clock when time is reached. It is disabled by rewriting the status register.	Nch open-drain output (no protective diode on the side of VDD)
6	SCL	Serial clock input pin Since signal processing is done on the SCL signal rising/falling edge, give great care to the rising/falling time and comply strictly with the specifications.	CMOS input (no protective diode on the side of VDD)
7	SDA	Serial data I/O pin Normally, it is pulled up to the V_{DD} voltage by a resistor and connected with another open-drain output or open-collector output device via a wired-OR connection.	Nch open-drain output (no protective diode on the side of VDD) CMOS input
8	VDD	Positive power supply pin	–

■ Block Diagram

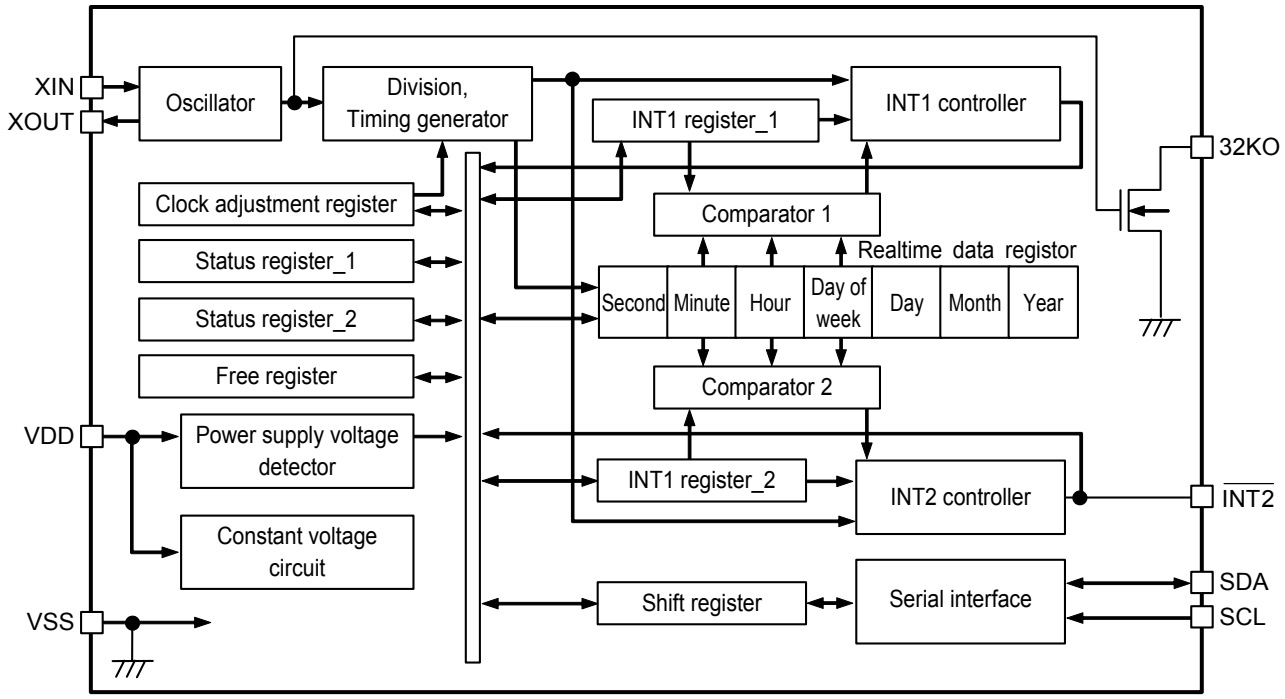


Figure 2

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Applicable Pin	Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	SCL, SDA	V_{SS} – 0.3 to V_{SS} + 6.5	V
Output voltage	V_{OUT}	SDA, 32KO, $\overline{INT2}$	V_{SS} – 0.3 to V_{SS} + 6.5	V
Operating ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	Ta = –40 to +85°C	1.3	3.0	5.5	V
Time keeping voltage range	V_{DDT}	Ta = –40 to +85°C	V_{DDTm}	–	5.5	V
Register hold voltage	V_{DH}	Ta = –40 to +85°C	V_{DDTm}	–	5.5	V
Minimum time keeping voltage range	V_{DDTm}	Ta = –40 to +85°C	0.5 *1	–	1.1	V
Crystal oscillator C_L value	C_L	–	–	–	7.0	pF

***1.** Reference value

■ Oscillation Characteristics

Table 4

(Ta = 25°C, V_{DD} = 3.0 V, VT-200 crystal oscillator (C_L = 6 pF, 32,768 Hz) manufactured by Seiko Instruments Inc.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within 10 seconds	1.1	–	5.5	V
Oscillation start time	t_{STA}	V_{DD} = 3.0 V	–	–	1	s
IC-to-IC frequency deviation *1	δIC	–	–10	–	+10	ppm
Frequency voltage deviation	δV	V_{DD} = 1.3 to 5.5 V	–3	–	+3	ppm/V
Input capacitance	C_g	Applied to XIN pin	0	–	9.1	pF
Internal oscillation capacitance	C_d	Applied to XOUT pin	–	8	–	pF

***1.** Reference value

■ DC Electrical Characteristics

Table 5 DC Characteristics (V_{DD} = 3.0 V)

(Ta = −40 to +85°C, V_{DD} = 3.0 V, VT-200 crystal oscillator (C_L = 6 pF, 32,768 Hz, C_g = 9.1 pF) manufactured by Seiko Instruments Inc.)

Parameter	Symbol	Applicable Pin	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	Out of communication	–	0.45	1.13	µA
Current consumption 2	I_{DD2}	–	During communication (SCL = 100 kHz)	–	6	14	µA
Input current leakage 1	I_{IZH}	SCL, SDA	$V_{IN} = V_{DD}$	−0.5	–	0.5	µA
Input current leakage 2	I_{IZL}	SCL, SDA	$V_{IN} = V_{SS}$	−0.5	–	0.5	µA
Output current leakage 1	I_{OZH}	32KO, $\overline{INT2}$, SDA	$V_{OUT} = V_{DD}$	−0.5	–	0.5	µA
Output current leakage 2	I_{OZL}	32KO, $\overline{INT2}$, SDA	$V_{OUT} = V_{SS}$	−0.5	–	0.5	µA
Input voltage 1	V_{IH}	SCL, SDA	–	$0.8 \times V_{DD}$	–	$V_{SS} + 5.5$	V
Input voltage 2	V_{IL}	SCL, SDA	–	$V_{SS} - 0.3$	–	$0.2 \times V_{DD}$	V
Output current 1	I_{OL1}	32KO, $\overline{INT2}$	V_{OUT} = 0.4 V	3	5	–	mA
Output current 2	I_{OL2}	SDA	V_{OUT} = 0.4 V	5	10	–	mA
Power supply voltage detection voltage *1	V_{DET}	–	Ta = −40 to +85°C	$V_{DDTm} + 0.15$ *2	–	$V_{DDTm} + 0.4$	V

***1.** Power supply voltage detection voltage: Constantly maintains the relation of $V_{DET} > V_{DDTm}$ (minimum time keeping voltage). Refer to **"Characteristics (Typical Data)"**.

***2.** Reference value

Table 6 DC Characteristics (V_{DD} = 5.0 V)

(Ta = −40 to +85°C, V_{DD} = 5.0 V, VT-200 crystal oscillator (C_L = 6 pF, 32,768 Hz, C_g = 9.1 pF) manufactured by Seiko Instruments Inc.)

Parameter	Symbol	Applicable Pin	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	Out of communication	–	0.6	1.4	µA
Current consumption 2	I_{DD2}	–	During communication (SCL = 100 kHz)	–	14	30	µA
Input current leakage 1	I_{IZH}	SCL, SDA	$V_{IN} = V_{DD}$	−0.5	–	0.5	µA
Input current leakage 2	I_{IZL}	SCL, SDA	$V_{IN} = V_{SS}$	−0.5	–	0.5	µA
Output current leakage 1	I_{OZH}	32KO, $\overline{INT2}$, SDA	$V_{OUT} = V_{DD}$	−0.5	–	0.5	µA
Output current leakage 2	I_{OZL}	32KO, $\overline{INT2}$, SDA	$V_{OUT} = V_{SS}$	−0.5	–	0.5	µA
Input voltage 1	V_{IH}	SCL, SDA	–	$0.8 \times V_{DD}$	–	$V_{SS} + 5.5$	V
Input voltage 2	V_{IL}	SCL, SDA	–	$V_{SS} - 0.3$	–	$0.2 \times V_{DD}$	V
Output current 1	I_{OL1}	32KO, $\overline{INT2}$	V_{OUT} = 0.4 V	5	8	–	mA
Output current 2	I_{OL2}	SDA	V_{OUT} = 0.4 V	6	13	–	mA
Power supply voltage detection voltage *1	V_{DET}	–	Ta = −40 to +85°C	$V_{DDTm} + 0.15$ *2	–	$V_{DDTm} + 0.4$	V

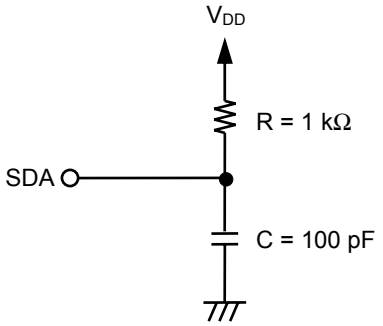
***1.** Power supply voltage detection voltage: Constantly maintains the relation of $V_{DET} > V_{DDTm}$ (minimum time keeping voltage). Refer to **"Characteristics (Typical Data)"**.

***2.** Reference value

■ AC Electrical Characteristics

Table 7 Measurement Conditions

Input pulse voltage	$V_{IH} = 0.9 \times V_{DD}$, $V_{IL} = 0.1 \times V_{DD}$,
Input pulse rise/fall time	20 ns
Output determination voltage	$0.5 \times V_{DD}$
Output load	100 pF + pull-up resistor 1 kΩ



Remark The power supplies of the IC and load have the same electrical potential.

Figure 3 Output Load Circuit

Table 8 AC Characteristics

(Ta = –40 to +85°C)

Parameter	Symbol	V_{DD} = 1.3 to 5.5 V			V_{DD} = 1.8 to 5.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	–	100	0	–	400	kHz
SCL clock “L” time	t_{LOW}	4.7	–	–	1.3	–	–	µs
SCL clock “H” time	t_{HIGH}	4	–	–	0.6	–	–	µs
SDA output delay time *1	t_{PD}	–	–	3.5	–	–	0.9	µs
Start condition setup time	$t_{SU.\ STA}$	4.7	–	–	0.6	–	–	µs
Start condition hold time	$t_{HD.\ STA}$	4	–	–	0.6	–	–	µs
Data input setup time	$t_{SU.\ DAT}$	250	–	–	100	–	–	ns
Data input hold time	$t_{HD.\ DAT}$	0	–	–	0	–	–	µs
Stop condition setup time	$t_{SU.\ STO}$	4.7	–	–	0.6	–	–	µs
SCL and SDA rise time	t_R	–	–	1	–	–	0.3	µs
SCL and SDA fall time	t_F	–	–	0.3	–	–	0.3	µs
Bus release time	t_{BUF}	4.7	–	–	1.3	–	–	µs
Noise suppression time	t_I	–	–	100	–	–	50	ns

***1.** Since the output format of the SDA pin is Nch open-drain output, the SDA output delay time is determined by the values of the load resistance (R_L) and load capacity (C_L) outside the IC. Therefore, use this value only as a reference value.

■ Timing Chart

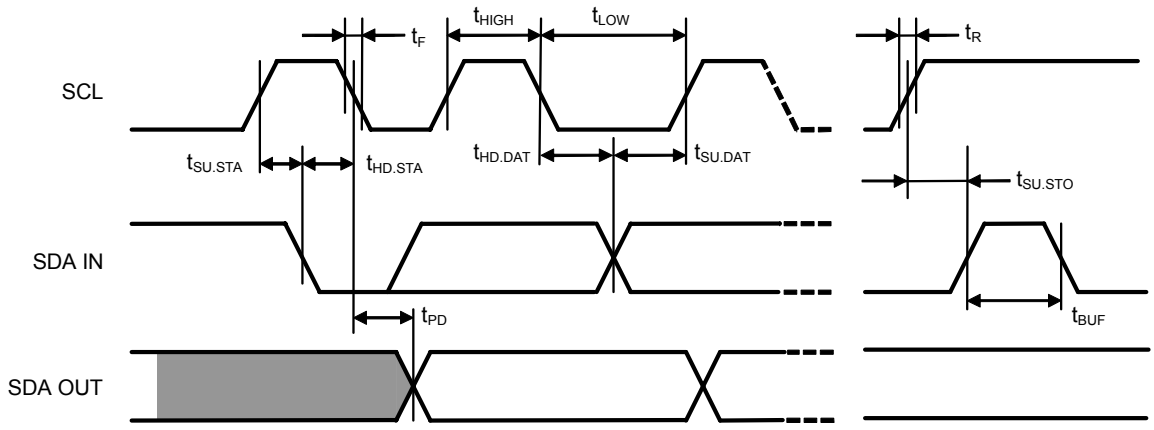


Figure 4 Bus Timing

■ Operation

1. Communication data configuration

The master device on the system generates a start condition to the slave device to communicate. Then it transmits a 4-bit device address, 3-bit command, and 1-bit read/write command on the SDA bus.
The higher 4 bits that indicate the device address are called the device code and are fixed to "0110". Refer to "**Serial Interface**".

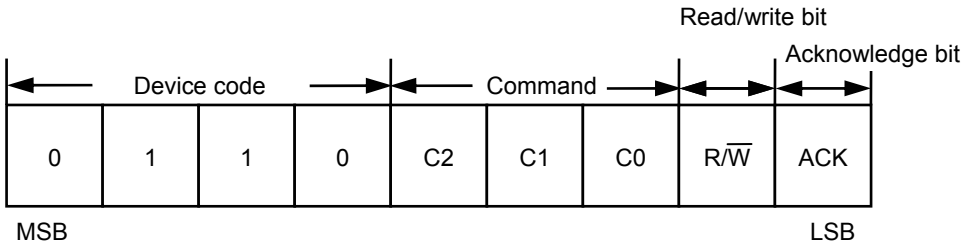


Figure 5 Communication Data

2. Command configuration

There are eight types of commands that read from and write to various registers. The table below lists these commands.

Table 9 Command List

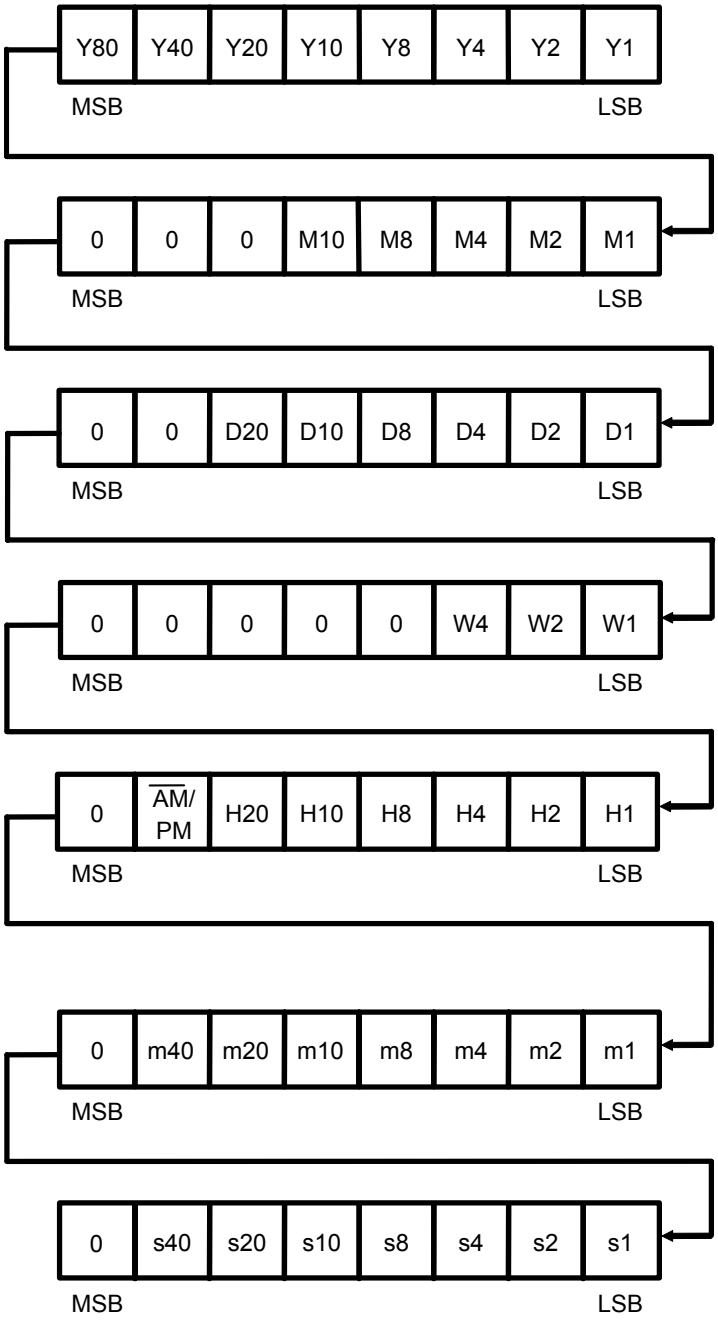
Command				Data							
C2	C1	C0	Description	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	Status register_1 access	POC *4	BLD *4	INT2 *3	INT1 *3	SC1 *2	SC0 *2	$\overline{12}$/24	RESET *1
0	0	1	Status register_2 access	TEST *5	INT2AE	INT2ME	INT2FE	SC *7	INT1AE	INT1ME	INT1FE
0	1	0	Real-time data 1 access (year data to)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
				– *6	– *6	– *6	M10	M8	M4	M2	M1
				– *6	– *6	D20	D10	D8	D4	D2	D1
				– *6	– *6	– *6	– *6	– *6	W4	W2	W1
				– *6	$\overline{AM}$/PM	H20	H10	H8	H4	H2	H1
				– *6	m40	m20	m10	m8	m4	m2	m1
				– *6	s40	s20	s10	s8	s4	s2	s1
0	1	1	Real-time data 2 access (hour data to)	– *6	$\overline{AM}$/PM	H20	H10	H8	H4	H2	H1
				– *6	m40	m20	m10	m8	m4	m2	m1
				– *6	s40	s20	s10	s8	s4	s2	s1
1	0	0	INT1 register_1 access (alarm time 1) (INT1AE = 1, INT1ME = 0, INT1FE = 0)	A1WE	– *6	– *6	– *6	– *6	W4	W2	W1
				A1HE	$\overline{AM}$/PM	H20	H10	H8	H4	H2	H1
				A1mE	m40	m20	m10	m8	m4	m2	m1
			INT1 register_1 access (free register function) (setting other than alarm time 1)	SC *2	SC *2	SC *2	SC *2	SC *2	SC *2	SC *2	SC *2
1	0	1	INT1 register_2 access (alarm time 2) (INT2AE = 1, INT2ME = 0, INT2FE = 0)	A2WE	— *6	— *6	— *6	— *6	W4	W2	W1
				A2HE	$\overline{AM}$/PM	H20	H10	H8	H4	H2	H1
				A2mE	m40	m20	m10	m8	m4	m2	m1
			INT1 register_2 access (frequency duty setting) (INT2ME = 0, INT2FE = 1)	SC *7	SC *7	SC *7	16 Hz	8 Hz	4 Hz	2 Hz	1 Hz
1	1	0	Clock adjustment register access	V7	V6	V5	V4	V3	V2	V1	V0
1	1	1	Free register access	F7	F6	F5	F4	F3	F2	F1	F0

***1.** Write-only flag. By writing "1" to this register, the IC is reset.
***2.** Scratch bit. R/W-enabled register that can be freely used by users.
***3.** Read-only flag. It is cleared when read. It is valid only when the alarm is set.
***4.** Read-only flag. "POC" is set to "1" when power is applied. It is cleared when read. For the "BLD", refer to "**Power Supply Voltage Detector**".
***5.** For IC testing. Normally set this register to "0".
***6.** No effect by writing. It is "0" when read.
***7.** This is a R/W-enabled register that does not affect interrupts.

■ Register Configuration

1. Real-time data register

The real-time data register is a 56-bit register that stores the BCD code of the year, month, day, day of week, hour, minute, and second data. Any read/write operation performed by the real-time data access command transmits or receives the data from the LSB which is the first digit of the year.



Year data (00 to 99)

Sets the lower two digits of the Western Calendar Year (00 to 99) and links together with the auto calendar feature until 2099.

Month data (01 to 12)

The count value is automatically changed by the auto calendar feature.

1 to 31 : 31-day months (1, 3, 5, 7, 8, 10, 12)
1 to 30 : 30-day months (4, 6, 9, 11)
1 to 29 : Feb. (leap year)
1 to 28 : Feb. (common year)

Day data (01 to 31)

Day of week data (00 to 06)

A septenary counter. Set it so that it corresponds to the day of the week.

Hour data (00 to 23 or 00 to 11)

$\overline{\text{AM}}$/PM

For a 12-hour expression, write 0 and 1 for AM and PM, respectively.
For a 24-hour expression, either 0 or 1 can be written. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.

Minute data (00 to 59)

Second data (00 to 59)

Figure 6 Real-time Data Register

2. Status register_1

Status register_1 is an 8-bit register that is used to display and set various modes. The bit configuration is shown below.

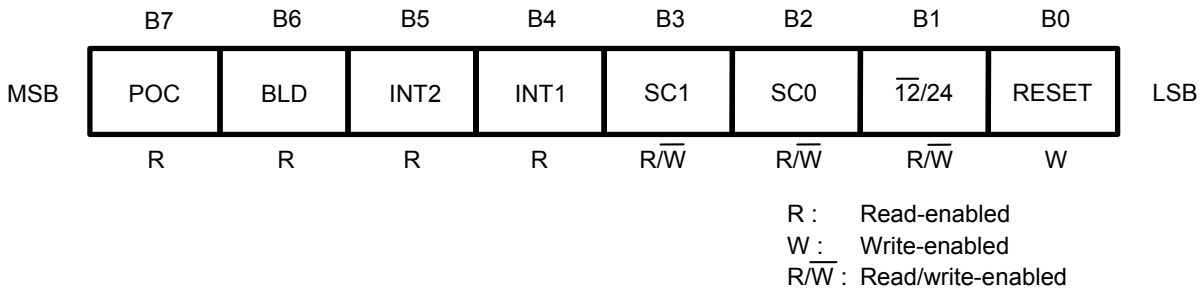


Figure 7 Status Register_1

B7 : POC This flag is set to "1" at power-on. Once this flag is set to "1", it is not set to "0" even when the power supply voltage reaches or exceeds the detection voltage (V_{DET}). This flag is read-only and can be read by the status register_1 access command. Once it is read, it is automatically set to "0". When the flag is "1", it must be initialized. For the method of initialization, refer to "**Initialization at Power-on and Power-on Detector**".

B6 : BLD If the power supply voltage detector detects a voltage of detection voltage (V_{DET}) or less this flag is set to "1", which enables the detection of a power supply voltage drop. Once this flag is set to "1", it is not set to "0" even when the power supply voltage reaches or exceeds the detection voltage (V_{DET}). This flag is read-only and can be read by the status register_1 access command. Once it is read, it is automatically set to "0". When the flag is "1", it must be initialized. For the method of initialization, refer to "**Initialization at Power-on and Power-on Detector**", and for the operation of the power supply voltage detector, refer to "**Power Supply Voltage Detector**".

B5 : INT2 When the interrupt signal is output from the $\overline{INT2}$ pin using the alarm interrupt function, the INT2 flag is set to "1". Once the flag is read, it is automatically cleared to "0".

B4 : INT1 When the alarm set time is reached with the alarm time setting function in use, the INT1 flag is set to "1". Once the flag is read, it is automatically cleared to "0".

B3, B2 : SC1, SC0

These flags configure a 2-bit SRAM type register that can be freely set by users. They are read and written within the operating voltage range (1.3 to 5.5 V).

B1 : $\overline{12}$/24 This flag is used to set 12-hour or 24-hour expression.

0 : 12-hour expression
1 : 24-hour expression

B0 : RESET By setting this bit to "1", the internal IC is initialized. This is a write-only bit and is always "0" when it is read. Be sure to write "1" to the reset flag when applying the power supply voltage to the IC.

3. Status Register_2

Status register_2 is an 8-bit register that is used to display and set various modes. The bit configuration is shown below.

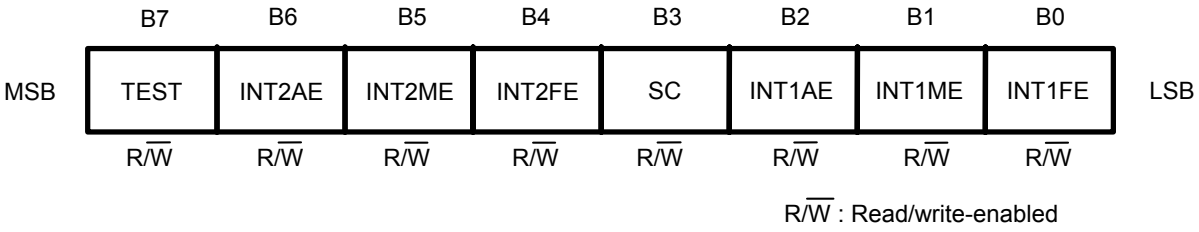


Figure 8 Status Register_2

B7 : TEST The TEST flag is a bit for testing the IC. If the TEST flag is set to "1", the IC is switched to the TEST mode. If this flag is "1", it is necessary to initialize it to "0" by setting the reset flag of status register_1 to "1".

B6 : INT2AE, B5 : INT2ME, B4 : INT2FE

These flags are used to select the output mode from the $\overline{INT2}$ pin. Mode selections are shown below. When using the alarm 2 function, after setting the alarm interrupt mode, access INT1 register_2.

Table 10 Interrupt Modes ($\overline{INT2}$)

INT2AE	INT2ME	INT2FE	$\overline{INT2}$ Pin Output Mode
0	0	0	No interrupt
*1	0	1	Selected frequency steady interrupt
*1	1	0	Per-minute edge interrupt
*1	1	1	Per-minute steady interrupt 1 (50% duty)
1	0	0	Alarm interrupt

***1.** Don't care (Both 0 and 1 are acceptable.)

B3 : SC This flag configures a 1-bit SRAM type register that can be freely set by users. It is read and written within the operating voltage range (1.3 to 5.5 V).

B2 : INT1AE, B1 : INT1ME, B0 : INT1FE

When using the alarm 1 function, set INT1AE to "1", INT1ME to "0", and INT1FE to "0". When a setting other than this is set, the alarm setting is disabled (free register function).

4. INT1 register_1 and INT1 register_2

INT1 register_1 is a register for setting alarm time and INT1 register_2 is a register for setting interrupts, and they can be independently set. The alarm output can be confirmed by reading INT1 of status register_1. An interrupt output of INT1 register_2 is output from the $\overline{INT2}$ pin. INT1 register_1 functions as alarm time setting or free register function. INT1 register_2 functions as alarm time setting or frequency duty setting. The function is switched by using status register_2.

(1) Alarm time setting

Data set in INT1 register_1 and INT1 register_2 is considered as alarm time data. Having the same configuration as the hour and minute registers of the real-time data register, these registers represent hours and minutes with BCD codes. When setting these registers, do not set any nonexistent day. Data to be set must be in accordance with the 12-hour or 24-hour expression that is set in status register_1.

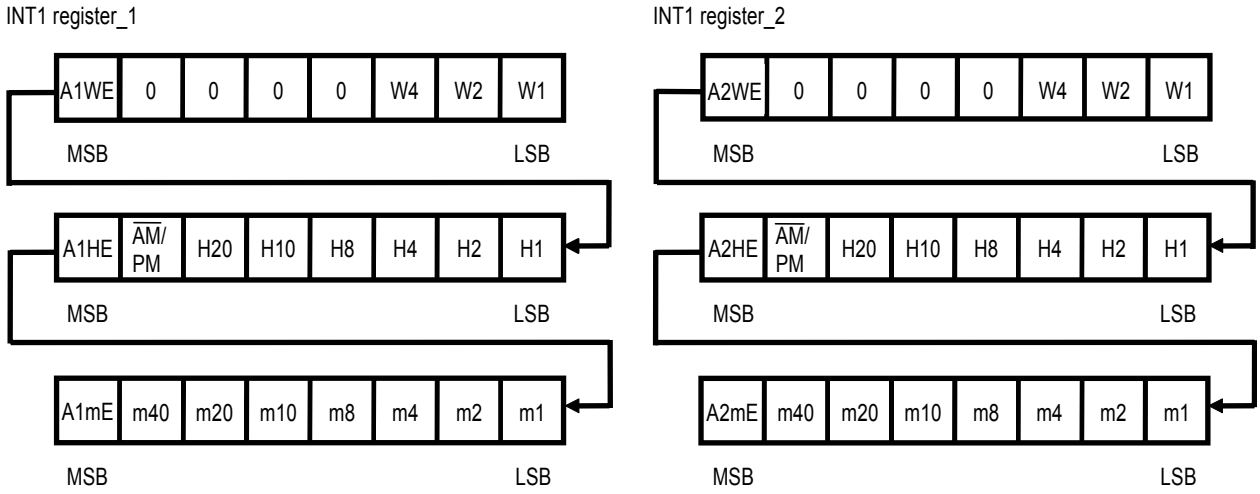


Figure 9 INT1 Register_1, INT1 Register_2 (Alarm Time Data)

In INT1 register_1, A1WE, A1HE, and A1mE are respectively in the MSB of each byte. By setting each bit to "1", the setting of the day of week data, hour data, and minute data in the corresponding byte becomes valid. A2WE, A2HE, and A2mE of INT1 register_2 are the same.

Example of setting The case of setting PM 7:00 as the alarm time in INT1 register_1 is shown below.

(a) 12-hour expression (status register_1 B1 = 0)

Set up 7:00 PM
Writing in INT1 register_1

Day of week data	0	–*1	–*1	–*1	–*1	–*1	–*1	–*1
Hour data	1	1	0	0	0	1	1	1
Minute data	1	0	0	0	0	0	0	0
	MSB							LSB

***1.** Don't care (Both 0 and 1 are acceptable.)

(b) 24-hour expression (status register_1 B1 = 1)

Set up 19:00 PM
Writing in INT1 register_1

Day of week data	0	–*1	–*1	–*1	–*1	–*1	–*1	–*1
Hour data	1	1*2	0	1	1	0	0	1
Minute data	1	0	0	0	0	0	0	0
	MSB							LSB

***1.** Don't care (Both 0 and 1 are acceptable.)
***2.** Set up $\overline{AM}$/PM flag along with the time setting.

(2) Free register function (INT1 register_1)

INT1 register_1 is a 1-byte SRAM type register that can be set freely by users. These bits can be read and written within the operating voltage range (1.3 to 5.5 V).

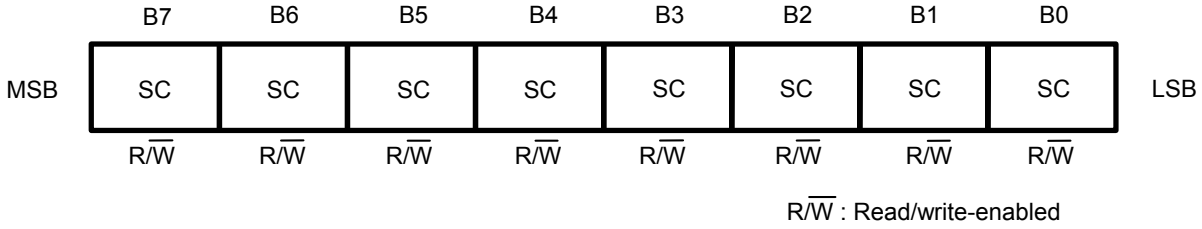


Figure 10 INT1 Register_1 (Free Data)

(3) Selected frequency steady interrupt (INT1 register_2)

Data set in INT1 register_2 is considered as frequency duty data. By setting each bit from B4 to B0 of the register to "1", the frequency corresponding to each bit is selected in an ANDed form. The SC bits configure a 3-bit SRAM type register that can be set freely by users. These bits can be read and written within the operating voltage range (1.3 to 5.5 V). There is no impact on the duty function.

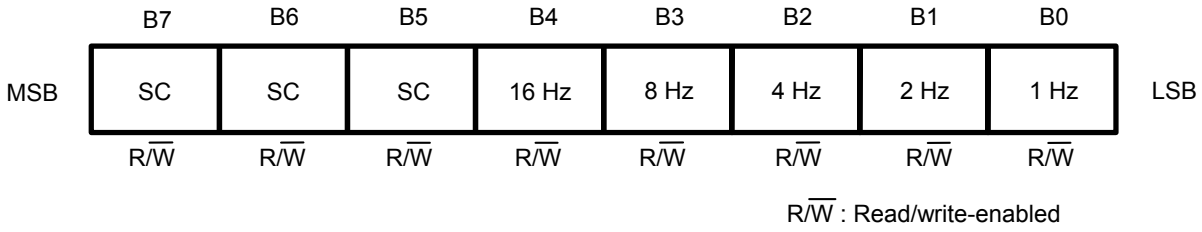


Figure 11 INT1 Register_2 (Frequency Duty Data)

Example B4 to B0 = 0Ah

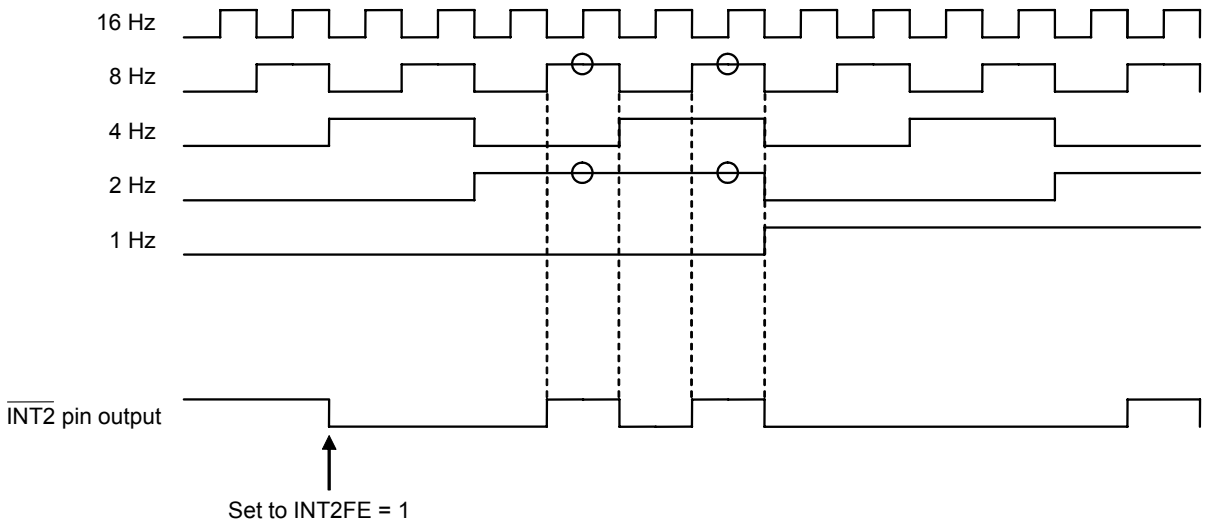


Figure 12 INT1 Register_2 (Frequency Duty Data) Output Example

5. Clock adjustment register

The clock adjustment register is a 1-byte register that is used to logically correct real-time data. When not using the clock adjustment register, set this register to 00h using the clock adjustment register write command.
For the “register value”, refer to “**Clock Adjustment Function**”.

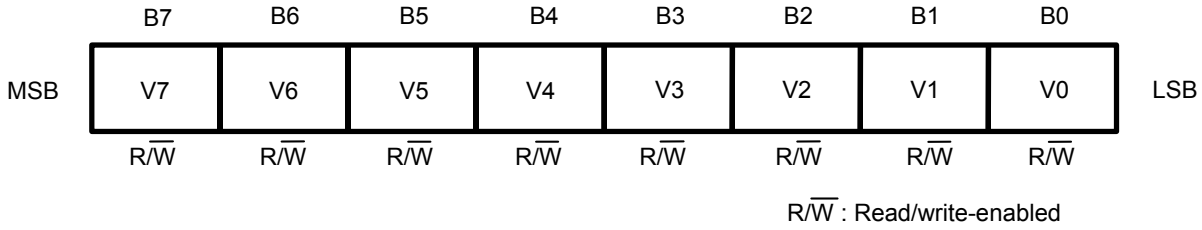


Figure 13 Clock Adjustment Register

6. Free register

The free register is a 1-byte SRAM type register that can be set freely by users. It can be read and written within the operating voltage range (1.3 to 5.5 V).

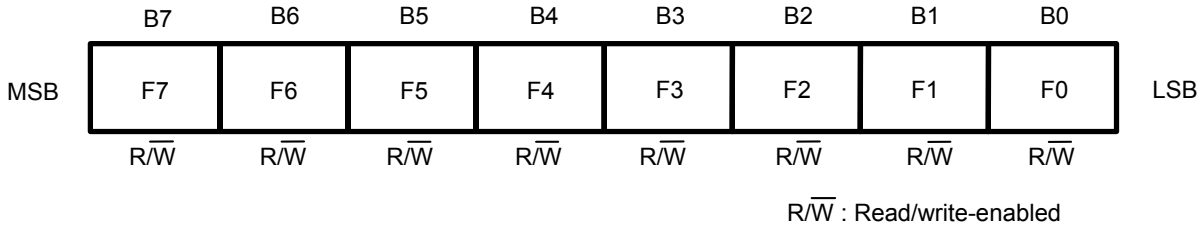


Figure 14 Free Register

■ Initialization at Power-on and Power-on Detector

When power is applied to this IC, status register_1 is set to “80h” (bit 7 (POC flag) of status register_1 is set to “1”) by the power-on detector.
The IC must be initialized when the POC flag is set to “1”. Initialization is performed by writing “1” to bit 0 (RESET flag) of status register_1. After initialization, the POC flag is set to “0”. For normal operation of the power-on detector, first hold the IC power supply voltage at 0 V and then increase it.

■ Register State After Initialization

The state of each register after initialization is as follows.

Real-time data register :	00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register_1 :	“0 0 0 0 B3 B2 B1 0 b” (The B3, B2, and B1 data of status register_1 after initialization are set in B3, B2, and B1.)
Status register_2 :	“00h”
INT1 register_1 :	“00h”
INT1 register_2 :	“00h”
Clock adjustment register :	“00h”
Free register :	“00h”

■ Power Supply Voltage Detector

S-35392A has an internal power supply voltage detector, which monitors drops in the power supply voltage by reading the BLD flag. This circuit samples the voltage for only 15.6 ms per second. If the power supply voltage drops below the detection voltage (V_{DET}), the BLD latch circuit latches the "H" level, bit 6 (BLD flag) of internal status register_1 is set to "1", and sampling stops. Detection voltage and release voltage have approximate 0.15 V (Typ.) of hysteresis width respectively (Refer to "**Characteristics (Typical Data)**"). Once "1" is detected in the BLD flag, no detection operation is performed unless initialization is performed or the BLD flag is read by the status register_1 access command, and "1" is held in the BLD flag. Sampling resumes only when the subsequent communication action is initialization or BLD flag read.
In addition, if this BLD flag is "1" after the power supply voltage is recovered, it must be initialized.

Caution In case the power supply voltage falls and returns after the latch circuit latches "H", the BLD flag can be read as "1" by a status register_1 accsess command first. After that the sampling is resumed and the read-out of the next BLD flag is performed, the BLD flag is reset and read as "0". Refer to the timing chart below.

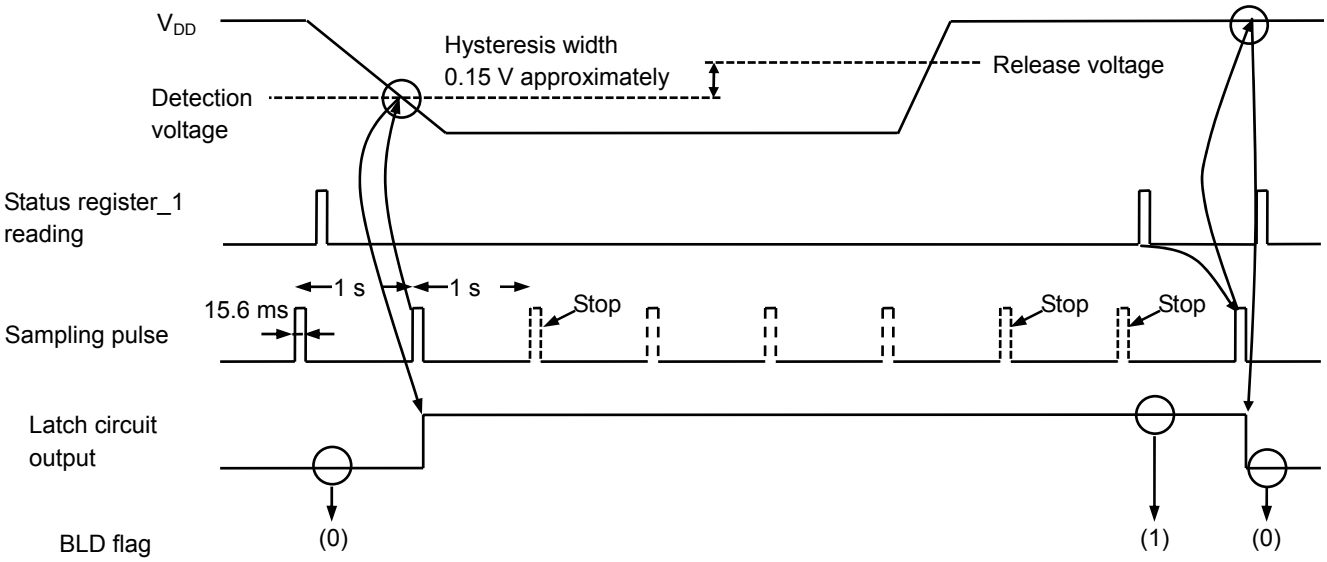


Figure 15 Timing of Power Supply Voltage Detector

■ Processing of Nonexistent Data and End-of-Month

When real-time data is written, the data is checked for validity, invalid data is processed, and the end-of-month is corrected.

1. Processing of nonexistent data

Table 11 Processing of Nonexistent Data

Register	Normal Data	Error Data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XA to XF	01
Day data	01 to 31	00, 32 to 39, XA to XF	01
Day of week data	0 to 6	7	0
Hour data*1 (24-hour)	0 to 23	24 to 29, 3X, XA to XF	00
(12-hour)	0 to 11	12 to 19, 2X, 3X, XA to XF	00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data*2	00 to 59	60 to 79, XA to XF	00

***1.** For 12-hour expression, write the $\overline{\text{AM}}$/PM flag.
The $\overline{\text{AM}}$/PM flag is ignored in 24-hour expression, but "0" for 0 to 11 hours and "1" for 12 to 23 hours are read in a read operation.

***2.** Processing of nonexistent data for second data is performed by a carry pulse one second after the end of writing. At this point, the carry pulse is sent to the minute counter.

2. Processing of end-of-month

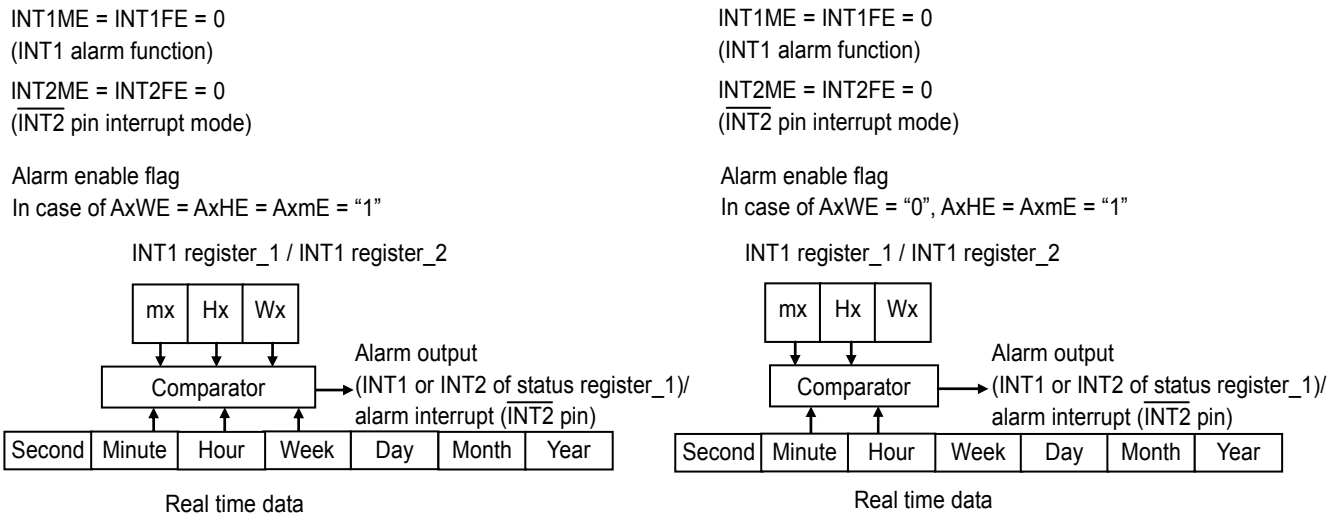
A nonexistent day is set to the first day of the next month. If February 30th is written, March 1st is set. Leap year correction is also performed at this time.

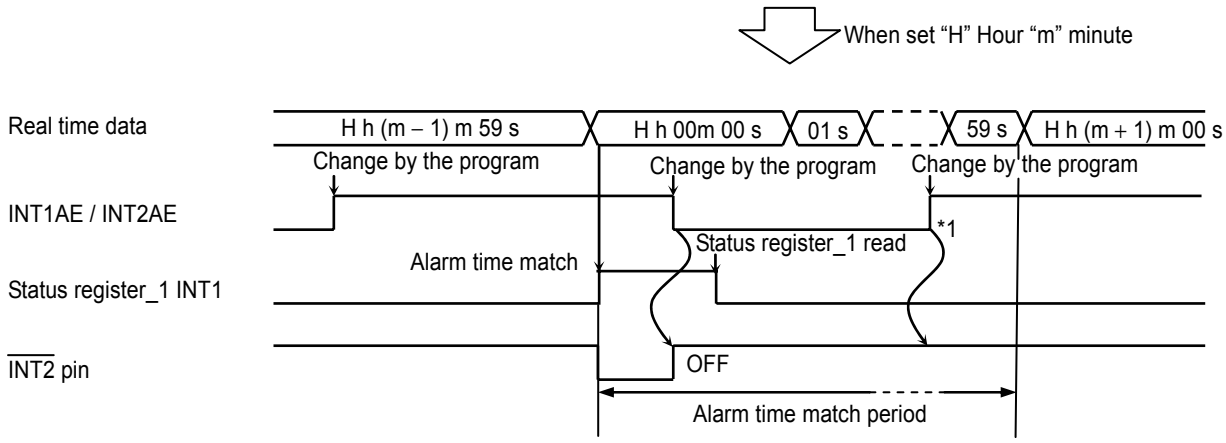
■ Alarm Function and Interrupts

The INT1 alarm function is selected by the INT1AE, INT1ME, and INT1FE flags of status register_2. Similarly, the $\overline{INT2}$ interrupt mode is selected by the INT2AE, INT2ME, and INT2FE flags of status register_2 (Refer to **Table 10 Interrupt Modes ($\overline{INT2}$)**).

(1) Alarm function and alarm interrupt output

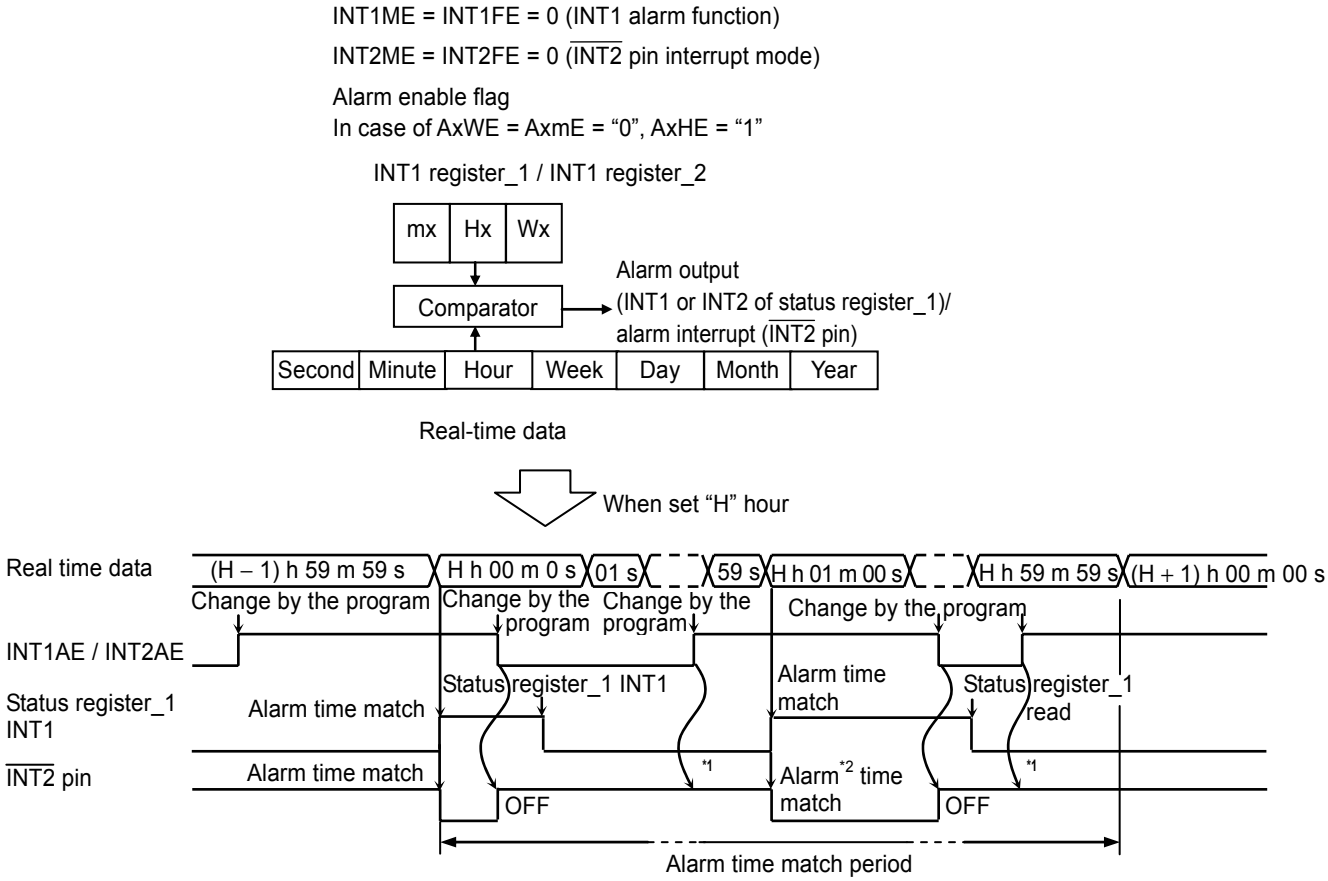
When the INT1 alarm is set using status register_2 and the day of week, hour, and minute data is set in INT1 register_1, the INT1 flag of status register_1 becomes "1" when the set hour is reached. When the $\overline{INT2}$ pin output mode is set as the alarm setting using status register_2 and the day of week, hour, and minute data is set in INT1 register_2, low is output from the $\overline{INT2}$ pin, the INT2 flag of status register_1 becomes "1" when the set hour is reached. Since the $\overline{INT2}$ pin output is held, rewrite INT2AE of status register_2 to "0" using serial communication to set the $\overline{INT2}$ pin output to high (OFF state).





***1.** Once it clears, even if it enables again within a coincidence period, "L" will not be output from the $\overline{INT2}$ pin.

Figure 16 Timing of Alarm Interrupt Output (1/2)



***1.** Once it clears, even if it enables again within a coincidence period, "L" will not be output from the $\overline{INT2}$ pin.

***2.** When an alarm output is turned on by change by the program within a coincidence period, "L" is again output from an $\overline{INT2}$ pin at the time of change of the following part.

Figure 16 Timing of Alarm Interrupt Output (2/2)

(2) Selected frequency steady interrupt output

When the $\overline{INT2}$ pin output mode is set as the selected frequency steady interrupt setting using status register_2 and the frequency/duty data is set in INT1 register_2, the set clock is output.

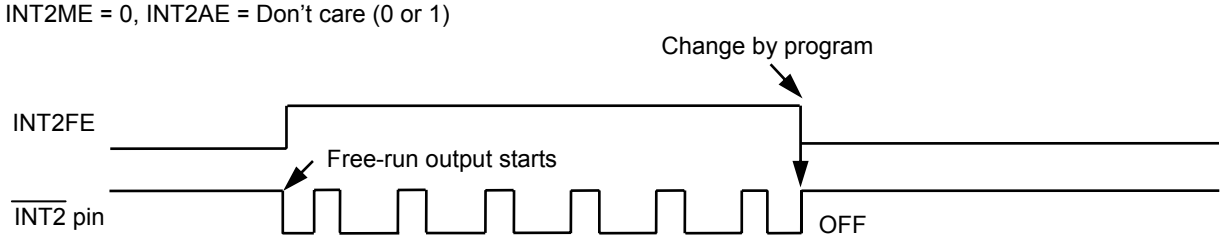


Figure 17 Timing of Selected Frequency Steady Interrupt Output

(3) Per-minute edge interrupt output

When the first minute carry is performed after the $\overline{INT2}$ pin output mode is set as the per-minute edge interrupt using status register_2, low is output from the $\overline{INT2}$ pin. Since the output is held, in the $\overline{INT2}$ pin output mode, rewrite INT2AE, INT2ME, and INT2FE of status register_2 to "0".

INT2FE = 0, INT2AE = Don't care (0 or 1)

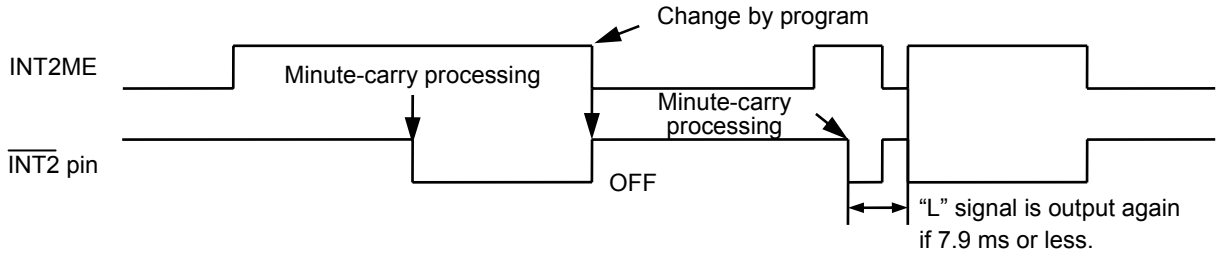


Figure 18 Timing of Per-Minute Edge Interrupt Output

Caution Since the minute carry processing signal is retained for 7.9 ms, if communication disable or enable is executed during this period, low is output from the $\overline{INT2}$ pin again.

(4) Per-minute steady interrupt output 1

When the first minute carry is performed after the $\overline{INT2}$ pin output mode is set as per-minute steady interrupt 1 using status register_2, a clock whose cycle is 1 minute (50% duty) is output from the $\overline{INT2}$ pin.

INT2AE = 0 ($\overline{INT2}$ pin output mode)

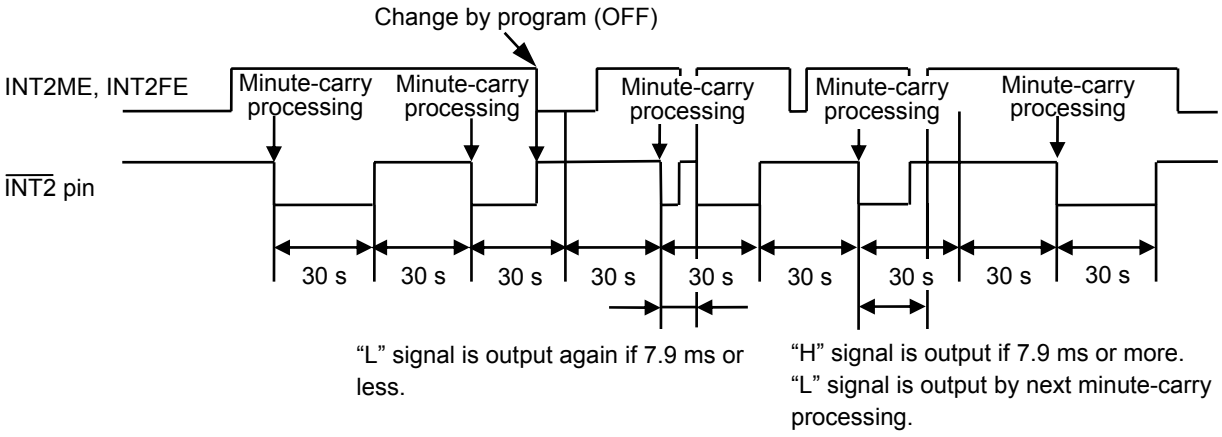


Figure 19 Timing of Per-Minute Steady Interrupt Output 1

Caution When communication disable or enable is execued while the $\overline{INT2}$ pin is low, low is output from the $\overline{INT2}$ pin again.

■ Clock Adjustment Function

A clock adjustment function is provided to logically perform slow/fast adjustment of the clock and correct a slow/fast clock with high accuracy. Use the clock adjustment register to set this function. When not using this function, be sure to set it to 00h.
The clock adjustment register value is calculated by the following expression.

(1) If current oscillation frequency > target frequency (in case the clock is fast)

$$\text{Register value}^{*1} = 128 - \text{Integral value}\left(\frac{(\text{Current oscillation frequency actual measurement value}^{*2}) - (\text{Target oscillation frequency}^{*3})}{(\text{Current oscillation frequency actual measurement value}^{*2}) \times (\text{Minimum resolution}^{*4})}\right)$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 64.

***1.** The register value is the value set to the clock adjustment register. Set the binarized value of this value to the clock adjustment register.
***2.** This is the measurement value of the signal that is output to the 32KO pin.
***3.** This is the frequency to be adjusted by using the clock adjustment function.
***4.** For the minimum resolution, 3.052 ppm or 1.017 ppm can be set using B7 of the clock adjustment register. When B7 is 0, 3.052 ppm is set and logical slow/fast adjustment is performed every 20 seconds. When B7 is 1, 1.017 ppm is set and logical slow/fast adjustment is performed every 60 seconds.

Table 12

	B7 = 0	B7 = 1
Slow/fast adjustment	Every 20 seconds	Every 60 seconds
Minimum resolution	3.052 ppm	1.017 ppm
Correction range	−195.3 ppm to +192.2 ppm	−65.1 ppm to +64.1 ppm

◆ The example of calculated value 1

Current oscillation frequency actual measurement value = 32,771 [Hz],
Target oscillation frequency = 32,768 [Hz],
B7 = 0 (minimum resolution = 3.052 ppm),

$$\text{Register value} = 128 - \text{Integral value}\left(\frac{(32771) - (32768)}{(32771) \times (3.052 \times 10^{-6})}\right)$$

$$= 128 - \text{Integral value}\,(29.99) = 128 - 29 = 99$$

Thus, set up (B7, B6, B5, B4, B3, B2, B1, B0) = (0, 1, 1, 0, 0, 0, 1, 1) for the clock adjustment register.

(2) If current oscillation frequency < target frequency (in case the clock is slow)

$$\text{Register value} = \text{Integral value}\left(\frac{(\text{Target oscillation frequency}) - (\text{Current oscillation frequency actual measurement value})}{(\text{Current oscillation frequency}) \times (\text{Minimum resolution})}\right) + 1$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 62.

◆ The example of calculated value 2

Current oscillation frequency actual measurement value = 32,765 [Hz],
Target oscillation frequency = 32,768 [Hz],
B7 = 0 (minimum resolution = 3.052 ppm),

$$\text{Register value} = \text{Integral value}\left(\frac{(32768) - (32765)}{(32765) \times (3.052 \times 10^{-6})}\right) + 1$$

= Integral value (30.00) + 1 = 30 + 1 = 31

Thus, set up (B7, B6, B5, B4, B3, B2, B1, B0) = (0, 0, 0, 1, 1, 1, 1, 1) for the clock register.

◆ The example of calculated value 3

Current oscillation frequency actual measurement value = 32,765 [Hz],
Target oscillation frequency = 32,768 [Hz],
B7 = 1 (minimum resolution = 1.017 ppm),

$$\text{Register value} = \text{Integral value}\left(\frac{(32768) - (32765)}{(32765) \times (1.017 \times 10^{-6})}\right) + 1$$

= Integral value (90.03) + 1

Thus, this calculated value exceeds the correctable range 0 to 62,
B7 = “1” (minimum resolution = 1.017 ppm) indicates the correction is impossible.

■ Serial Interface

The S-35392A receives various commands via an I^2C-BUS serial interface to read/write data. This section covers the transfer methods via I^2C-BUS.

1. Start condition

The start condition is established at the point where the SDA line changes from “H” to “L” when the SCL line is “H” level. All operations start with the start condition.

2. Stop condition

The stop condition is established at the point where the SDA line changes from “L” to “H” when the SCL line is “H” level. If the stop condition is received during a readout sequence, the read operation is discontinued and the device enters the standby mode.

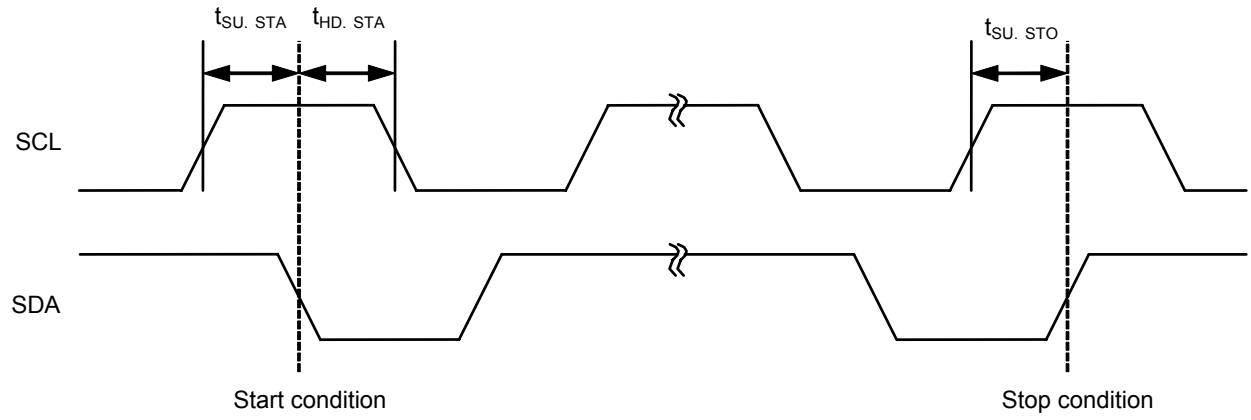


Figure 20 Start Condition and Stop Condition

3. Data transfer

Data transfer is performed by changing the SDA line during the period that the SCL line is “L”.
If the SDA line changes during the period that the SCL line is “H”, it is recognized as the start or stop condition.

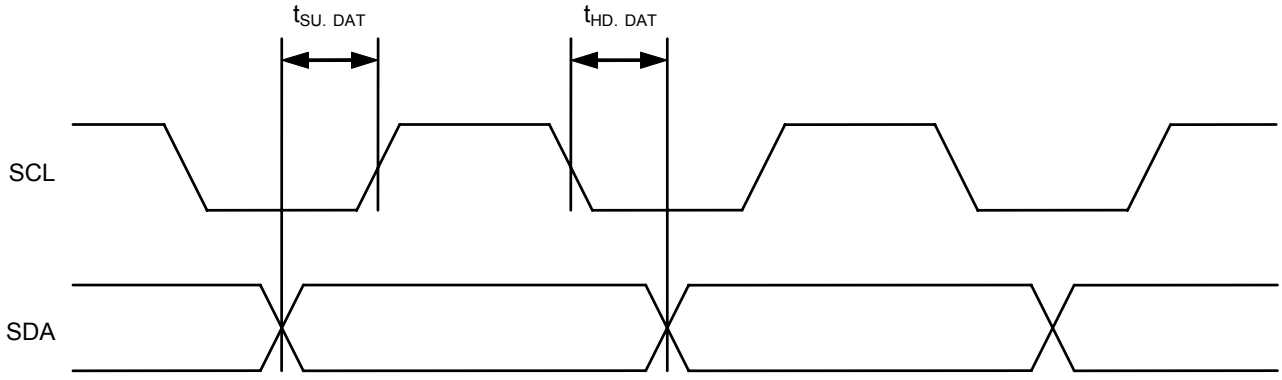


Figure 21 Timing of Data Transfer

4. Acknowledge

Data is transferred 8 bits in a row. Subsequently, in the 9th clock cycle period, the device on the system bus that is receiving the data changes the SDA line to “L” and returns the acknowledge signal to acknowledge data reception.

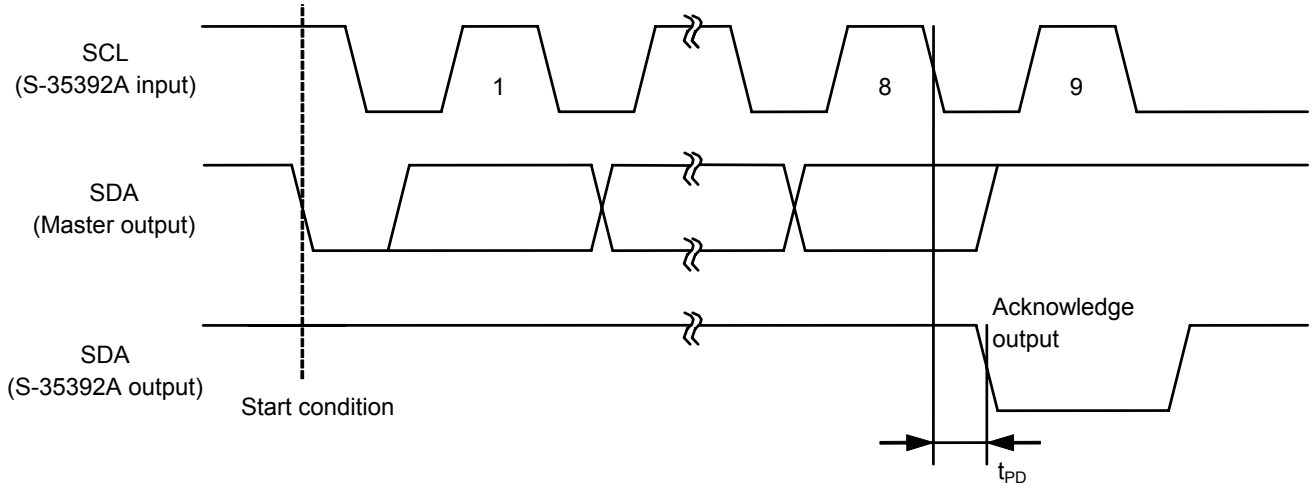


Figure 22 Timing of Acknowledge Output

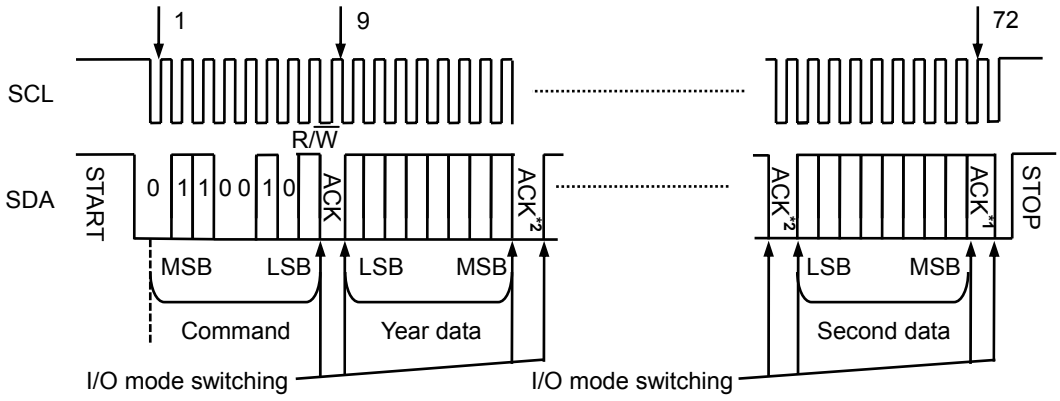
5. Data reading

After detecting the start condition from outside, a device code and command are received. If the read/write bit is “1” at this point, the data read mode is entered. The data output sequence is output from the LSB.

6. Data writing

After detecting the start condition from outside, a device code and command are received. If the read/write bit is "0" at this point, the real-time data write mode or another register write mode is entered. Input the data input sequence for both the real-time data write mode and status register write mode from the LSB.
In real-time data writing, the calendar and time counter is reset by the rising of the ACK signal after the real-time write command and update operations are then prohibited. Subsequently, when minute data reception is completed, an end-of-month correction is performed while the second data is loaded. Counting up is started from the rising of the ACK signal after the second data reception.

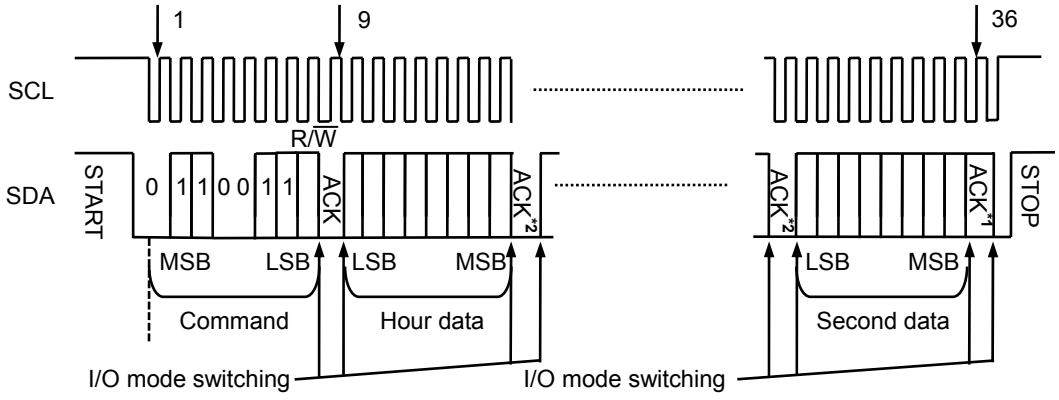
(1) Real-time data 1 access



***1.** During reading, set NO_ACK to 1.
***2.** During reading, transmit ACK = 0 to S-35392A from the master device.

Figure 23 Real-time Data 1 Access

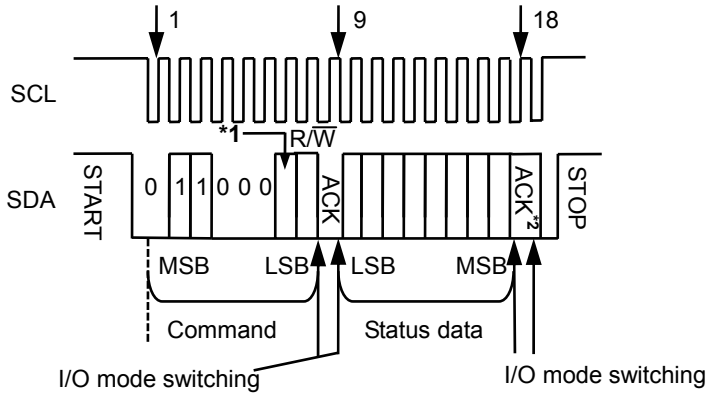
(2) Real-time data 2 access



***1.** During reading, set NO_ACK to 1.
***2.** During reading, transmit ACK = 0 to S-35392A from the master device.

Figure 24 Real-time Data 2 Access

(3) Status register_1 access and status register_2 access



***1.** 0 : Status register_1 selected, 1 : Status register_2 selected
***2.** During reading, set NO_ACK to 1.

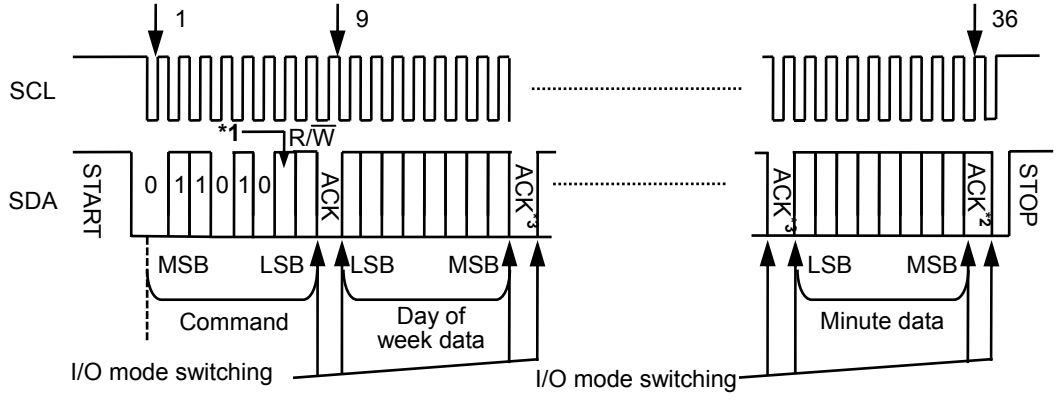
Figure 25 Status Register_1 Access and Status Register_2 Access

(4) INT1 register_1 access and INT1 register_2 access

Since data written to and read from INT1 register_1 varies according to the setting of status register_2, be sure to set status register_2 before reading/writing INT1 register_1. When an alarm is set using status register_2, these registers function as 3-byte alarm time data registers, and other than that, they function as 1-byte registers.

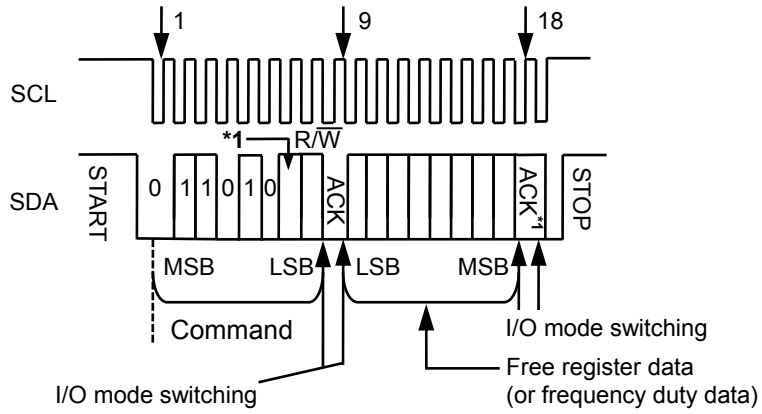
Caution Alarm time data and free register data cannot be operated simultaneously.

Since data written to and read from INT1 register_2 varies according to the setting of status register_2, be sure to set status register_2 before reading/writing INT1 register_1. When an alarm is set using status register_2, these registers function as 3-byte alarm time data registers, and other than that, they function as 1-byte registers. When the selected frequency steady interrupt setting is set, the data in these registers is frequency duty setting data. For details of each data, refer to **"■ Register Configuration 4. INT1 register_1 and INT1 register_2"**.



***1.** 0 : INT1 register_1 selected, 1 : INT1 register_2 selected
***2.** During reading, set NO_ACK to 1.
***3.** During reading, transmit ACK = 0 to S-35392A from the master device.

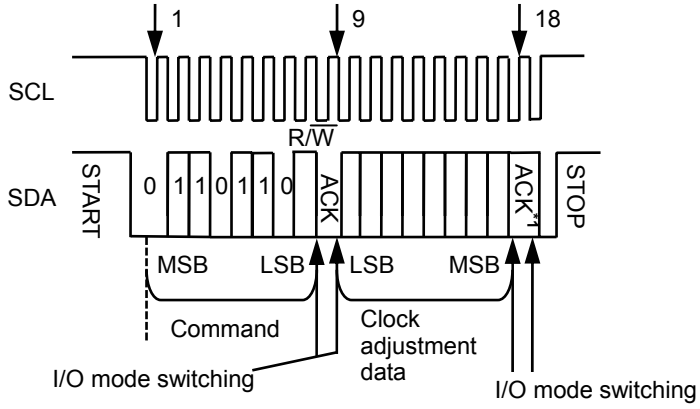
Figure 26 INT1 Register_1 Access and INT1 Register_2 Access



***1.** 0 : INT1 register_1 selected, 1 : INT1 register_2 selected
***2.** During reading, set NO_ACK to 1.

Figure 27 INT1 Register_1 (Free Register Data) and INT1 Register_2 (Frequency Duty Data) Access

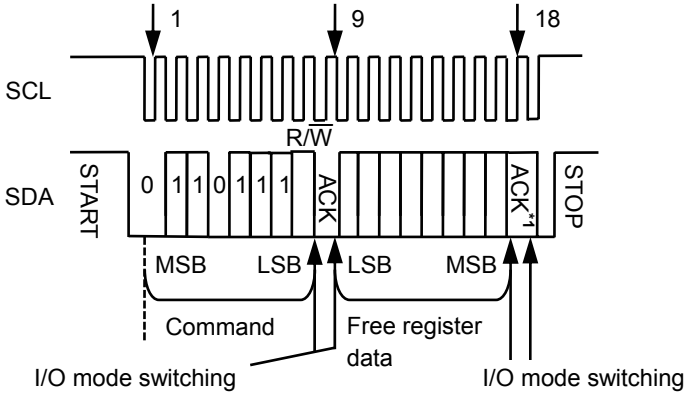
(5) Clock adjustment register access



***1.** During reading, set NO_ACK to 1.

Figure 28 Clock Adjustment Register Access

(6) Free register access

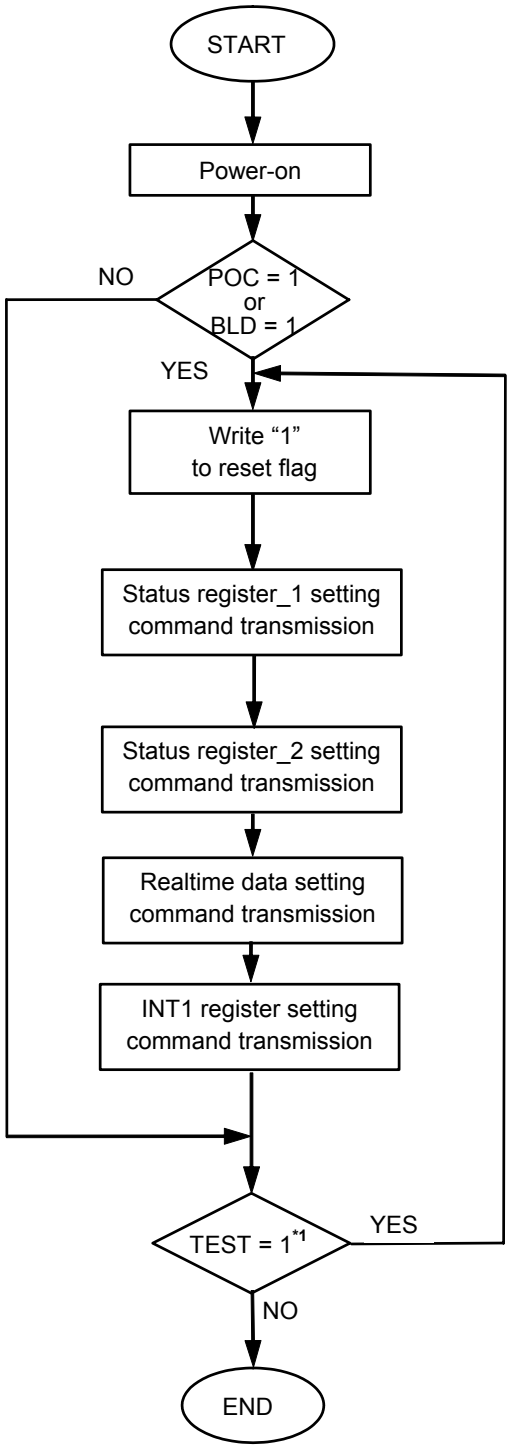


***1.** During reading, set NO_ACK to 1.

Figure 29 Free Register Access

■ Example of Software Processing

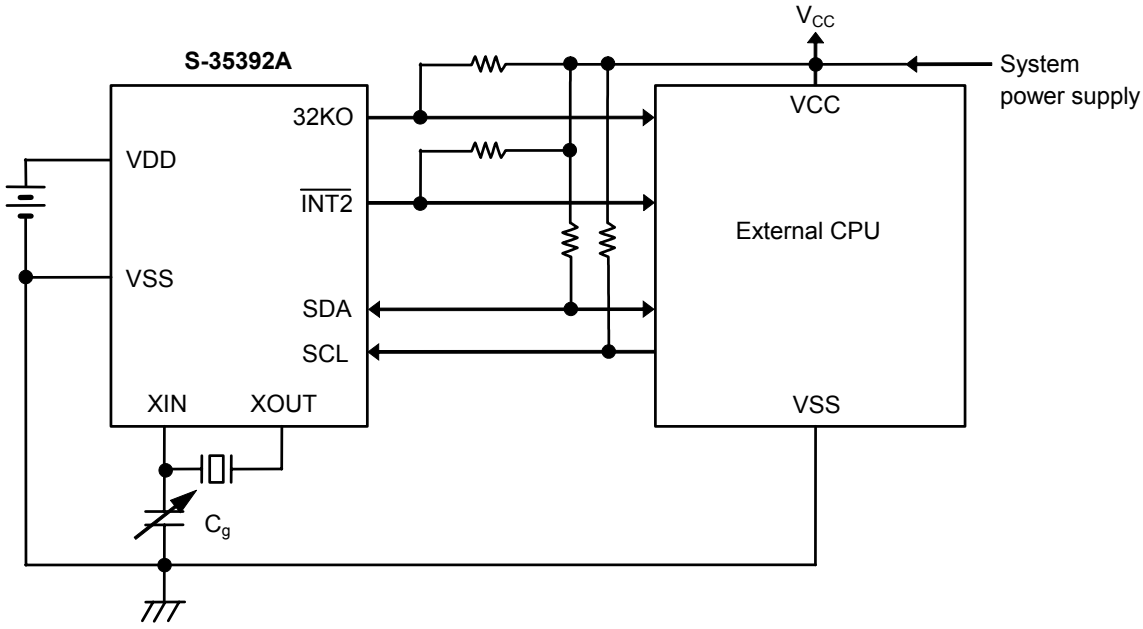
1. Initialization flow at power-on



***1.** If conditions are poor (e.g., in a noisy environment) and there is a high probability that commands transmitted via serial communication will be garbled, it is recommended to verify the TEST flag.

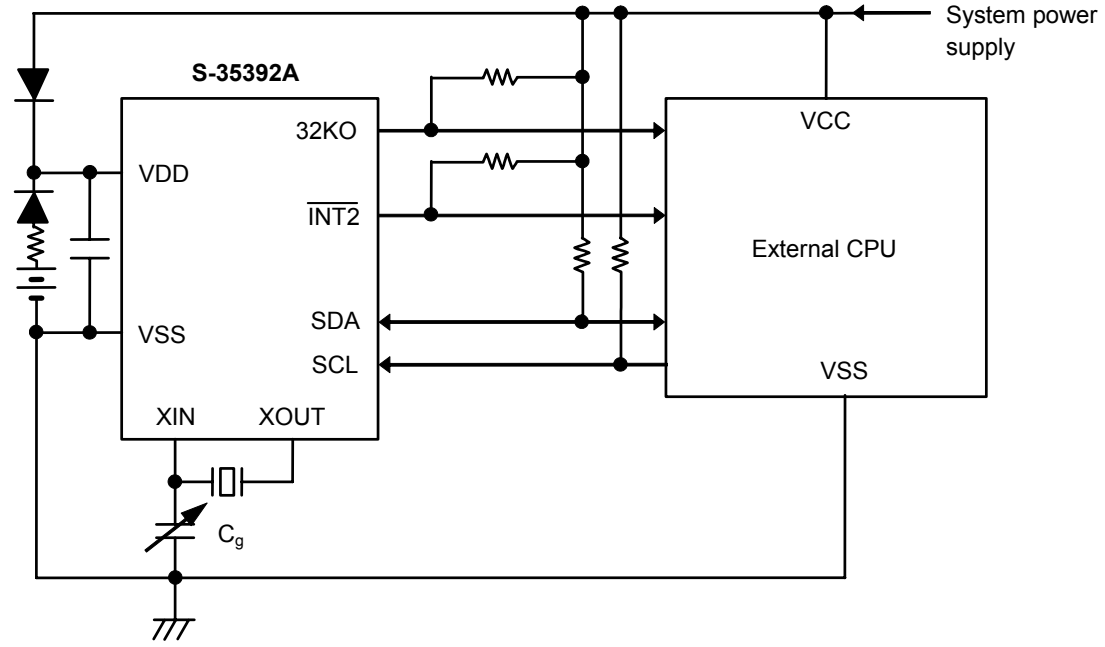
Figure 30 Initialization Flow

■ Examples of Application Circuits



Cautions 1. Because the I/O pin has no protective diode on the VDD side, the relation of $V_{CC} \geq V_{DD}$ is possible. But pay careful attention to the specifications.
2. Communication should be executed after the system power supply is turned on and a stable state is obtained.

Figure 31 Application Circuit 1



Caution Communication should be executed after the system power supply is turned on and a stable state is obtained.

Figure 32 Application Circuit 2

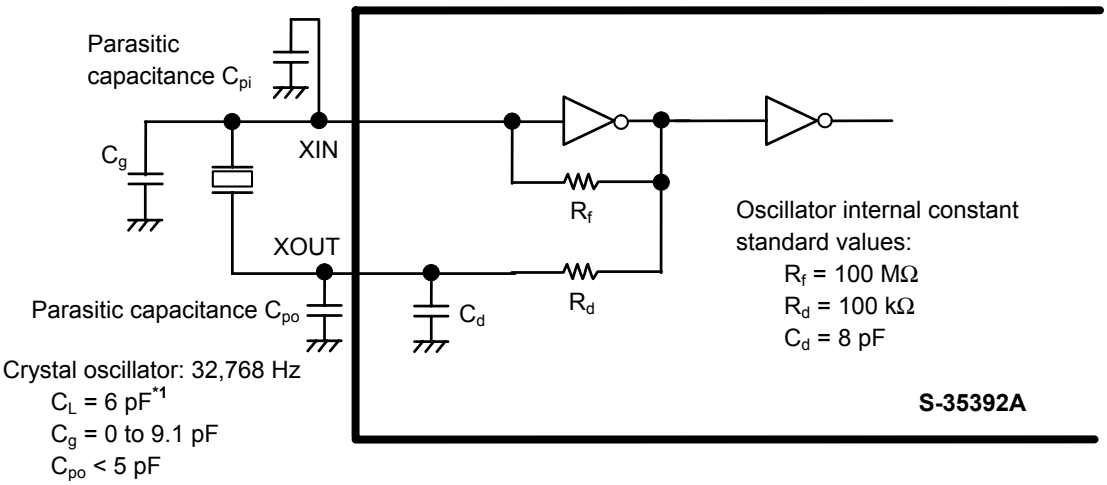
Caution The above connection diagrams do not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

■ Adjustment of Oscillation Frequency

1. Configuration of oscillator

Since crystal oscillation is sensitive to external noise (the clock accuracy is affected), the following measures are essential for optimizing the oscillator configuration.

(1) Place the S-35392A, crystal oscillator, and external capacitor (C_g) as close to each other as possible.
(2) Increase the insulation resistance between pins and the substrate wiring patterns of XIN and XOUT.
(3) Do not place any signal or power lines close to the oscillator.



***1.** When using the crystal oscillator with a C_L value of 7 pF, externally connect C_d if necessary.

Figure 33 Connection Diagram 1

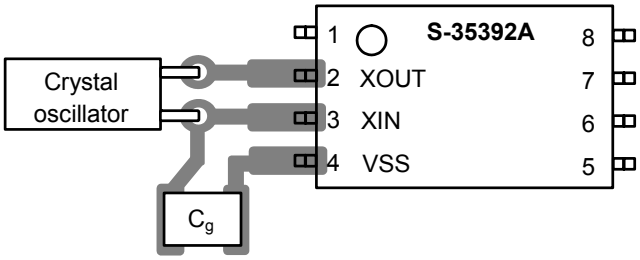


Figure 34 Connection Diagram 2

Cautions 1. When using the crystal oscillator with a C_L exeeding the rated value (7.0 pF) (e.g : C_L = 12.5 pF), oscillation operation may become unstable. Use a crystal oscillator with a C_L value of 6 pF or 7 pF.
2. Oscillation characteristics is subject to the variation of each component such as substrate parastic capacitance, parastic resistance, crystal oscillator, and C_g. When configurating oscillation circuit, pay sufficient attention for them.

2. Measurement of oscillation frequency

The S-35392A outputs a 32,768 Hz signal from the 32KO pin after the power is on. Turn the power on and measure the signal with a frequency counter following the circuit configuration shown in **Figure 35**.

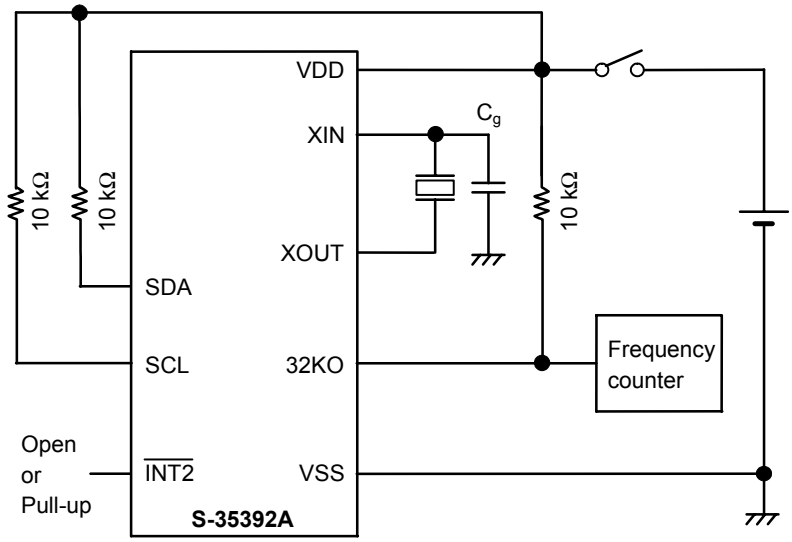


Figure 35 Configuration of Oscillation Frequency Measurement Circuit

Caution Use a high-accuracy frequency counter (1 ppm order).

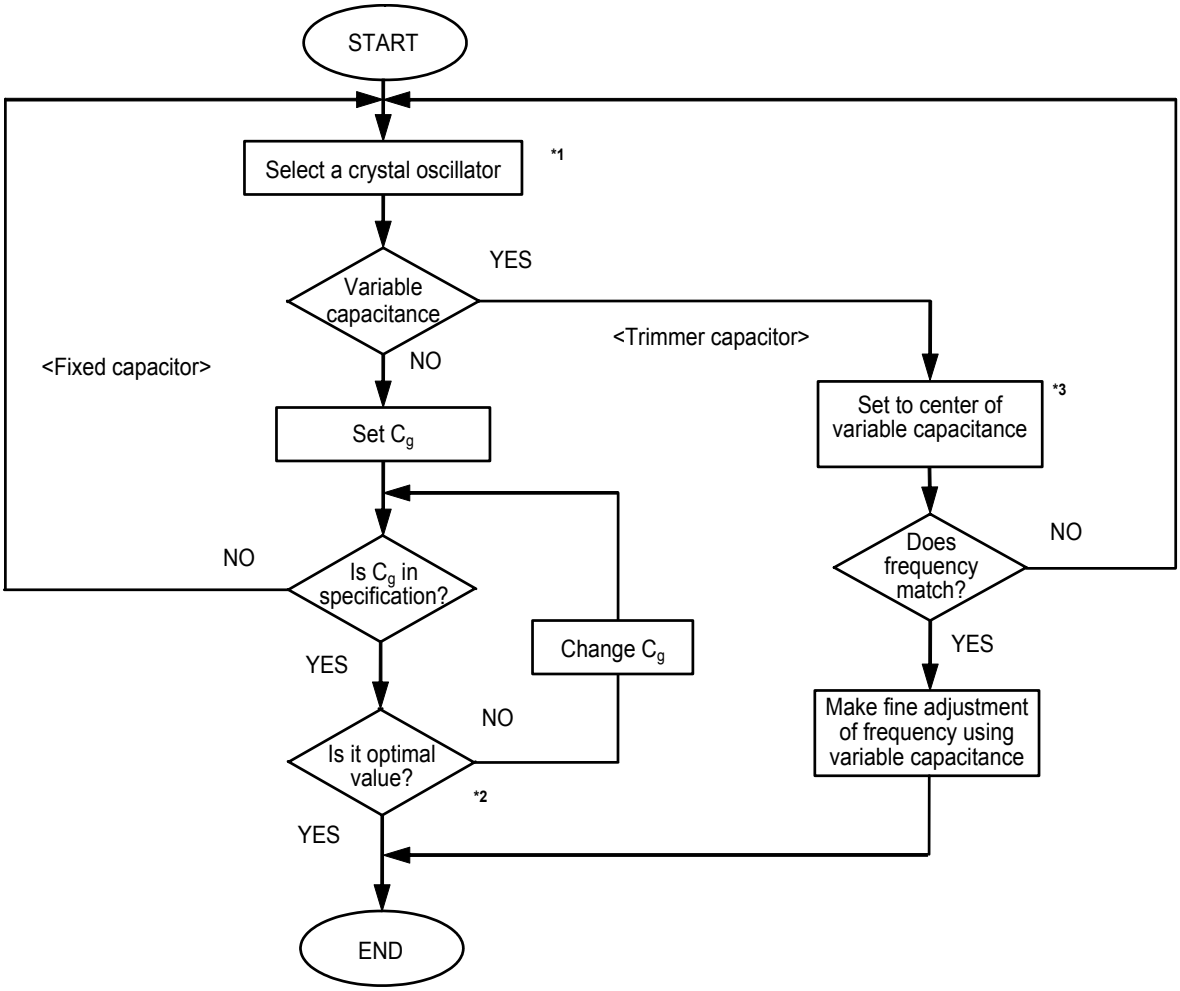
Remark If the error range is ±1 ppm in relation to 32,768 Hz, the time is shifted by approximately 2.6 seconds per month (calculated using the following expression).

$$10^{-6}\ (1\ \text{ppm}) \times 60\ \text{seconds} \times 60\ \text{minutes} \times 24\ \text{hours} \times 30\ \text{days} = 2.592\ \text{seconds}$$

3. Adjustment of oscillation frequency

Adjustment by setting C_g

Matching of the crystal oscillator with the nominal frequency must be performed with the stray capacitance on the board included. Select a crystal oscillator and optimize the C_g value in accordance with the flowchart below.



***1.** For the matching adjustment of the IC with a crystal, contact the crystal manufacturer to determine the C_L value (load capacitance) and R_1 value (equivalent series resistance). C_L = 6 pF and R_1 = 50 kΩ max. are recommended values.

***2.** The C_g value must be selected on the actual PCB since it is affected by stray capacitance. Select the external C_g value in a range of 0 pF to 9.1 pF.

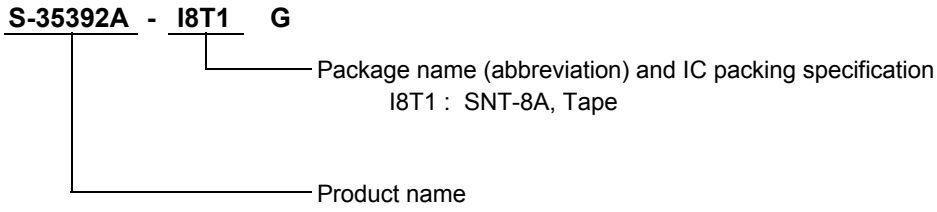
***3.** Adjust the rotation angle of the variable capacitance so that the capacitance value is slightly smaller than the center, and confirm the oscillation frequency and the center value of the variable capacitance. This is done in order to make the capacitance of the center value smaller than one half of the actual capacitance value because a smaller capacitance value increases the frequency variation.

Figure 36 Crystal Oscillator Setting Flow

Cautions 1. The oscillation frequency varies depending on the ambient temperature and power supply voltage. Refer to the "Characteristics (Typical Data)".

2. The 32 kHz crystal oscillator operates more slowly at an operating temperature than higher or lower 20 to 25°C. Therefore, it is recommended to adjust or set the oscillator to operate slightly faster at normal temperature.

■ Product Name Structure

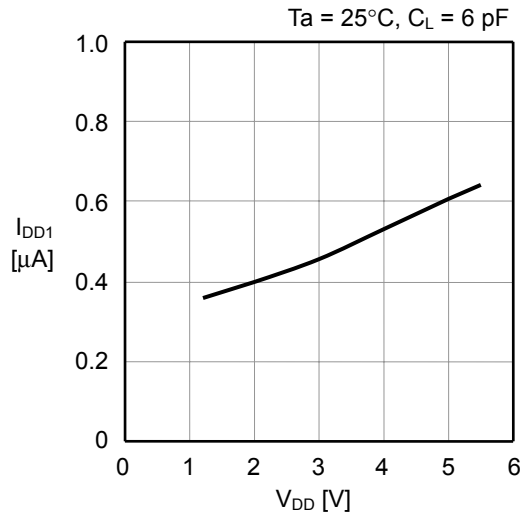


■ Precautions

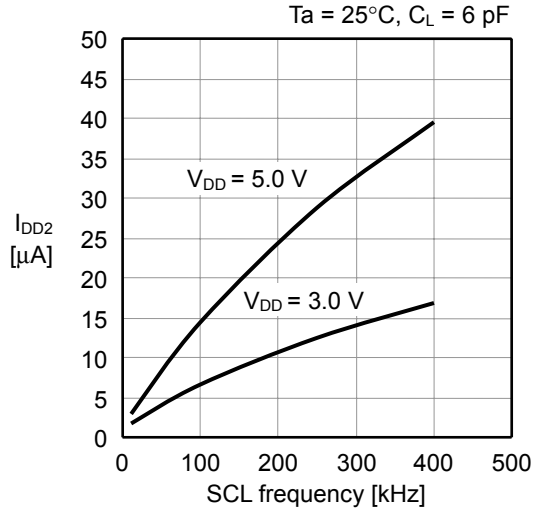
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- Seiko Instruments Inc. assumes no responsibility for the way in which this IC is used in products created using this IC or for the specifications of that product, nor does Seiko Instruments Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

■ Characteristics (Typical Data)

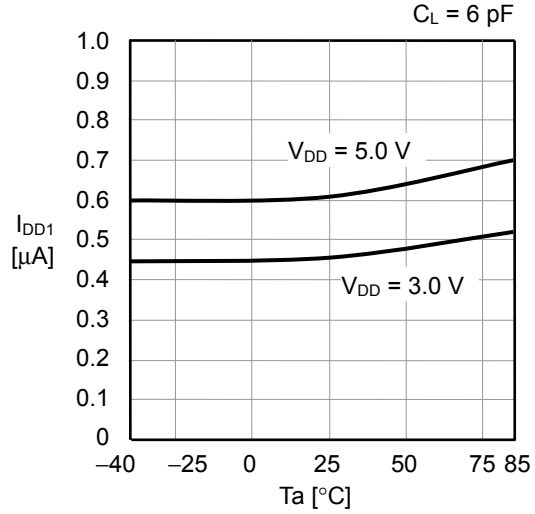
(1) Standby current vs. V_{DD} characteristics



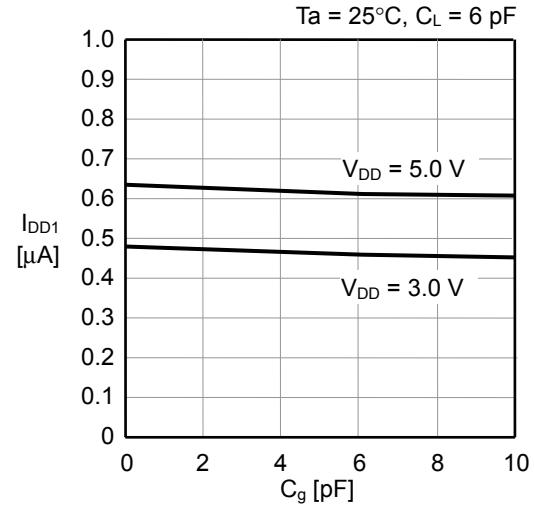
(2) Current consumption during operation vs. Input clock characteristics



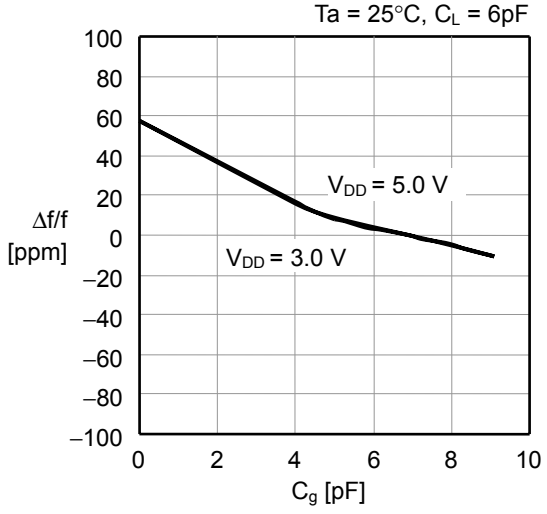
(3) Standby current vs. Temperature characteristics



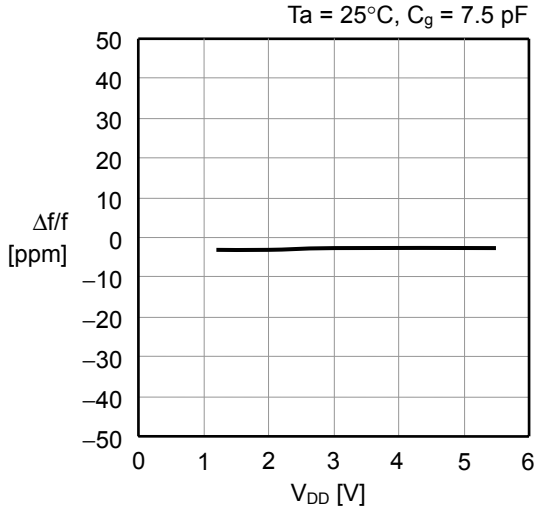
(4) Standby current vs. C_g characteristics



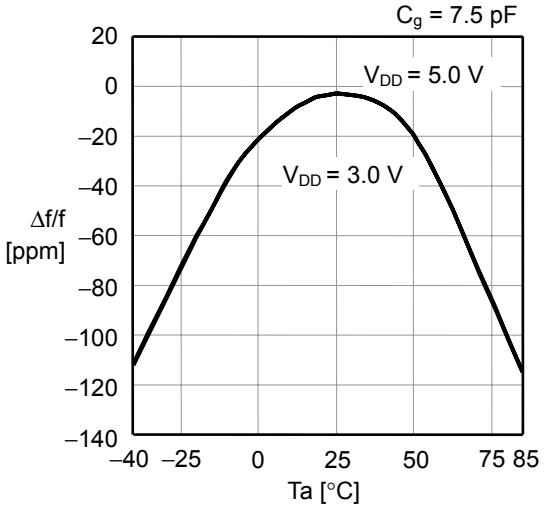
(5) Oscillation frequency vs. C_g characteristics



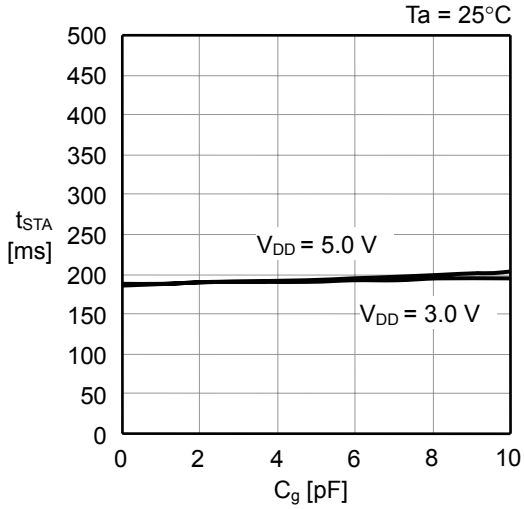
(6) Oscillation frequency vs. V_{DD} characteristics



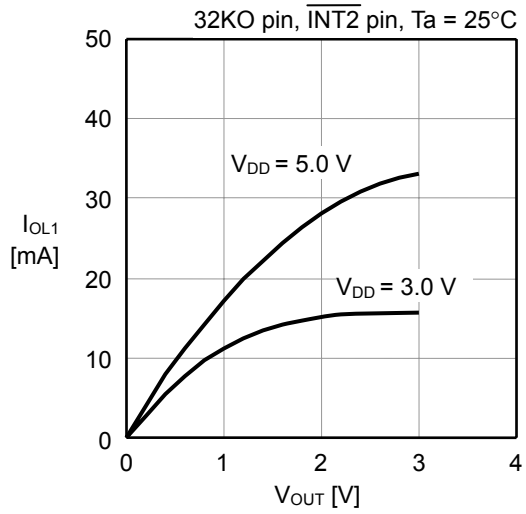
(7) Oscillation frequency vs. Temperature characteristics



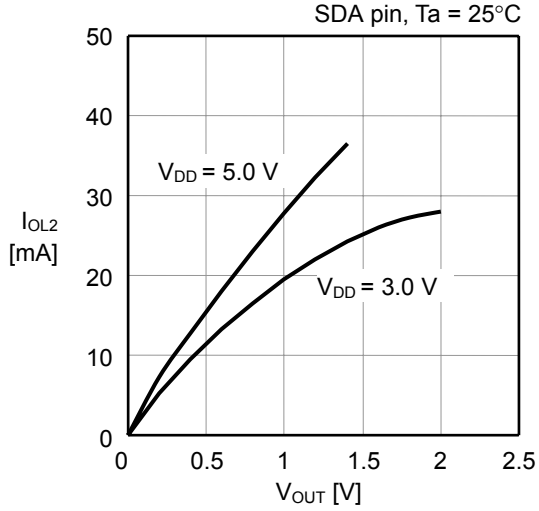
(8) Oscillation start time vs. C_g characteristics



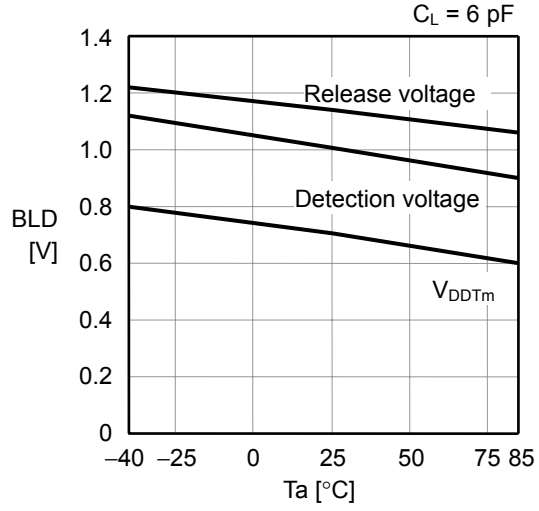
(9) Output current characteristics 1 (V_{OUT} vs. I_{OL1})

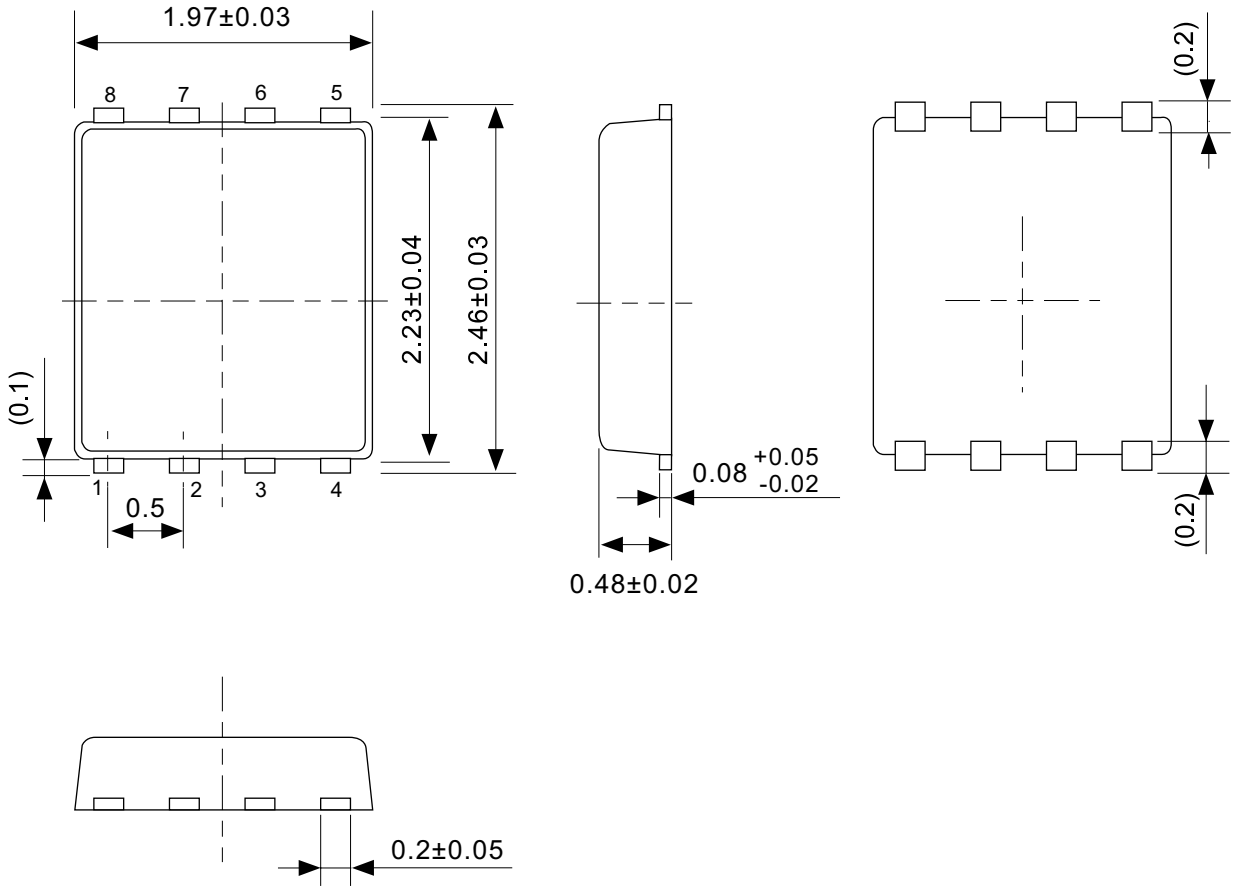


(10) Output current characteristics 2 (V_{OUT} vs. I_{OL2})



(11) BLD detection, release voltage, V_{DDTm} vs. Temperature characteristics





No. PH008-A-P-SD-2.0

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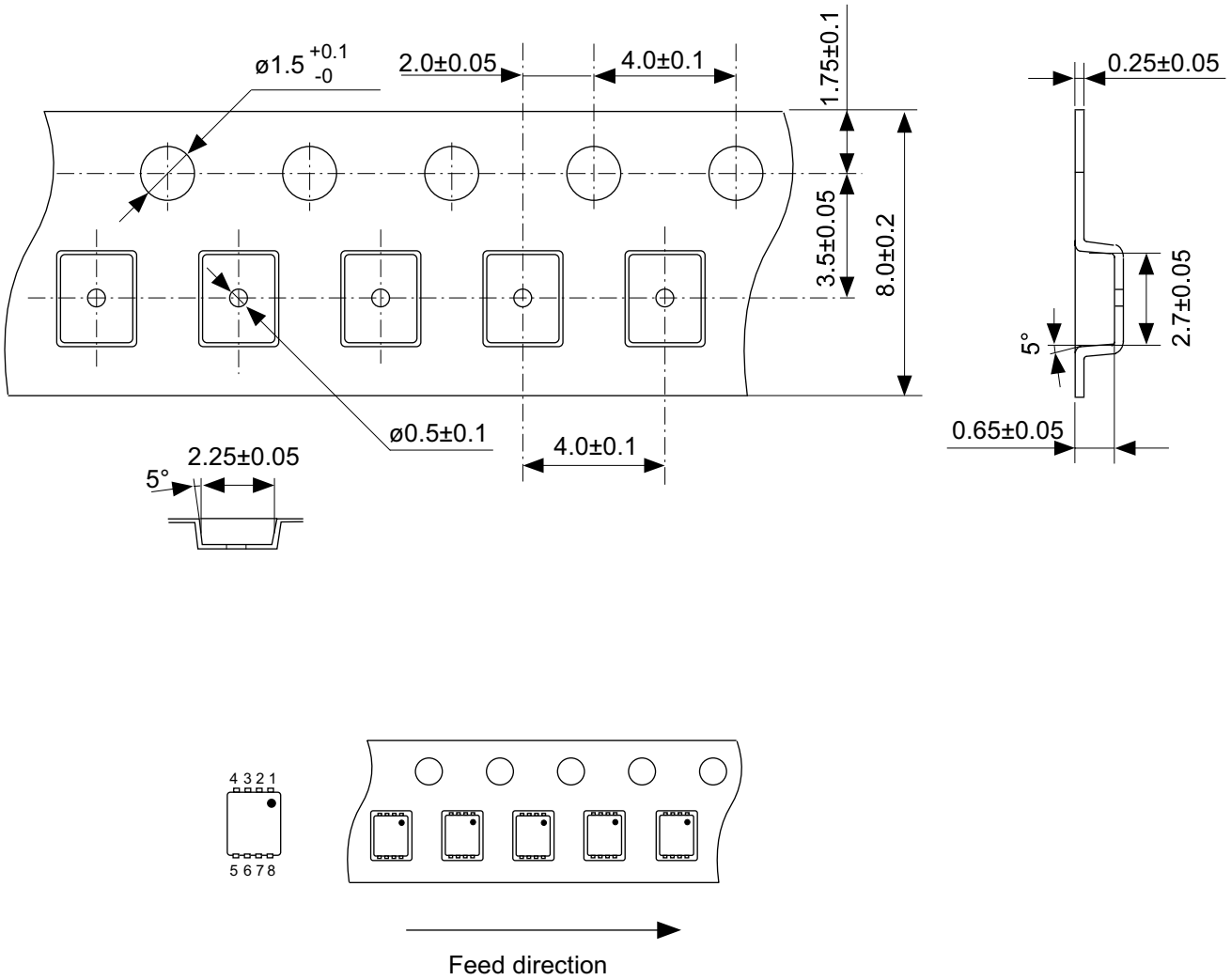
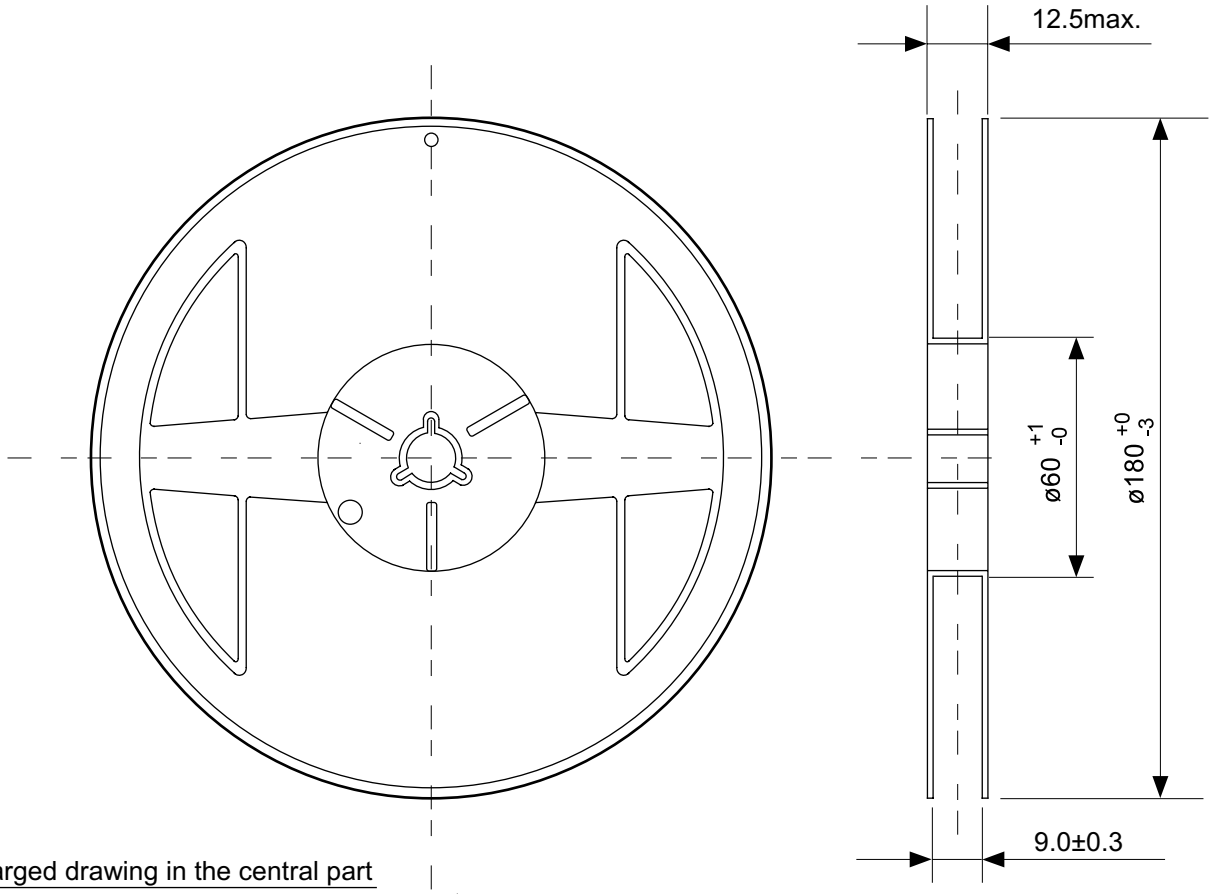
UNIT	mm
Seiko Instruments Inc.	

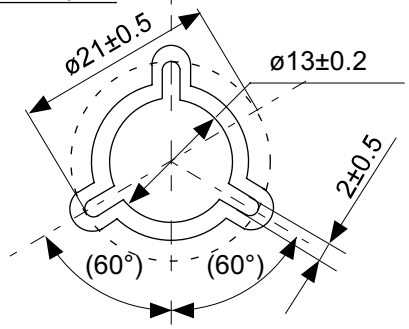


No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

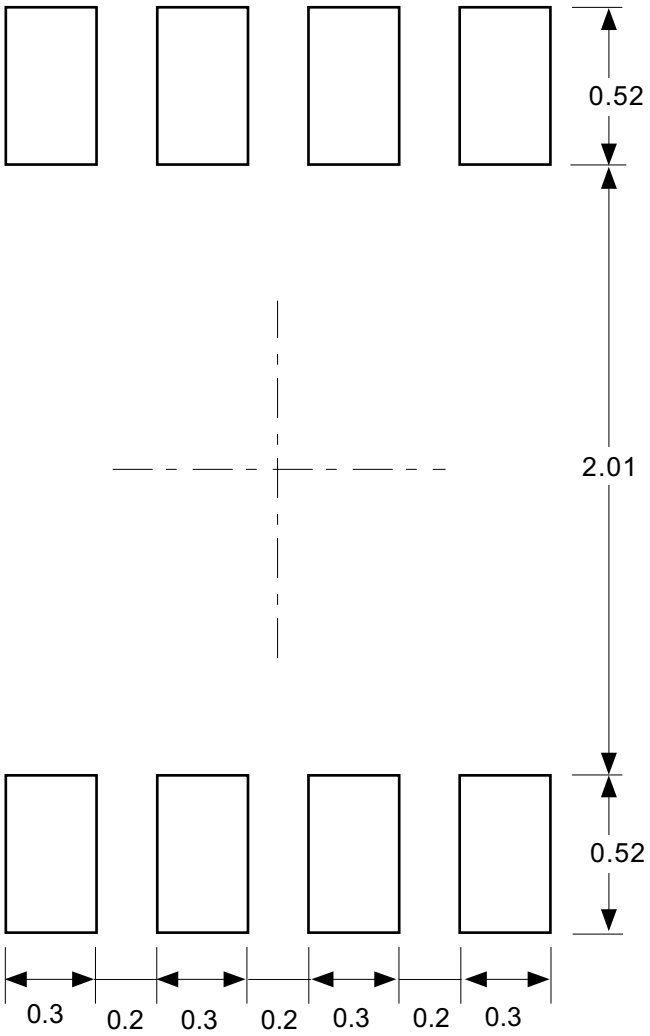


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			



Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がることがありますのでご配慮ください。

No. PH008-A-L-SD-3.0

TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

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