TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

16,777,216-WORD BY 72-BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM73V1615BTG is a 16,777,216-word by 72-bit dynamic RAM module consisting of 18 TC5165405BFT DRAMs on a printed circuit board. This module is optimized for applications which require high density and high capacity, such as computer main memory and image memory, and also for applications which require compactness.

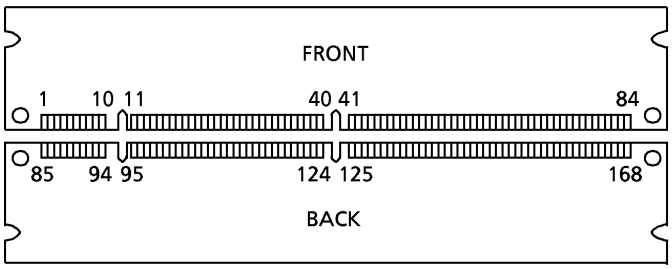
FEATURES

- 16,777,216-word by 72-bit organization
- Fast access and cycle times

	-4	-5
t_{RAC} $\overline{RAS}$ Access Time	40 ns	50 ns
t_{AA} Column Address Access Time	20 ns	25 ns
t_{CAC} $\overline{CAS}$ Access Time	11 ns	13 ns
t_{RC} Cycle Time	69 ns	84 ns
t_{HPC} Hyper Page Mode Cycle Time	16 ns	20 ns

- Single power supply of 3.3 V ± 5%
- Low power dissipation (max)
  - Operating 7496 mW (40-ns type)
  - 6246 mW (50-ns type)
  - Standby 31.3 mW (both devices)
- Read-Modify-Write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-Only refresh, Hidden refresh and EDO (Hyper Page mode) capability
- All inputs and outputs LVTTL-compatible
- 4096 refresh cycles per 64 ms
- Package: 168-pin TSOP Gold contacts

PIN ASSIGNMENT (TOP VIEW)



1	Vss	85	Vss	29	/CAS1	113	/CAS5	57	DQ18	141	DQ50
2	DQ0	86	DQ32	30	/RAS0	114	NC	58	DQ19	142	DQ51
3	DQ1	87	DQ33	31	/OE0	115	NC	59	Vcc	143	Vcc
4	DQ2	88	DQ34	32	Vss	116	Vss	60	DQ20	144	DQ52
5	DQ3	89	DQ35	33	A0	117	A1	61	NC	145	NC
6	Vcc	90	Vcc	34	A2	118	A3	62	NC	146	NC
7	DQ4	91	DQ36	35	A4	119	A5	63	NC	147	NC
8	DQ5	92	DQ37	36	A6	120	A7	64	Vss	148	Vss
9	DQ6	93	DQ38	37	A8	121	A9	65	DQ21	149	DQ53
10	DQ7	94	DQ39	38	A10	122	A11	66	DQ22	150	DQ54
11	DQ8	95	DQ40	39	NC	123	NC	67	DQ23	151	DQ55
12	Vss	96	Vss	40	Vcc	124	Vcc	68	Vss	152	Vss
13	DQ9	97	DQ41	41	Vcc	125	NC	69	DQ24	153	DQ56
14	DQ10	98	DQ42	42	NC	126	NC	70	DQ25	154	DQ57
15	DQ11	99	DQ43	43	Vss	127	Vss	71	DQ26	155	DQ58
16	DQ12	100	DQ44	44	/OE2	128	NC	72	DQ27	156	DQ59
17	DQ13	101	DQ45	45	/RAS2	129	NC	73	Vcc	157	Vcc
18	VCC	102	Vcc	46	/CAS2	130	/CAS6	74	DQ28	158	DQ60
19	DQ14	103	DQ46	47	/CAS3	131	/CAS7	75	DQ29	159	DQ61
20	DQ15	104	DQ47	48	/WE2	132	NC	76	DQ30	160	DQ62
21	CB0	105	CB4	49	Vcc	133	Vcc	77	DQ31	161	DQ63
22	CB1	106	CB5	50	NC	134	NC	78	Vss	162	Vss
23	Vss	107	Vss	51	NC	135	NC	79	NC	163	NC
24	NC	108	NC	52	CB2	136	CB6	80	NC	164	NC
25	NC	109	NC	53	CB3	137	CB7	81	NC	165	SA0
26	Vcc	110	Vcc	54	Vss	138	Vss	82	SDA	166	SA1
27	/WE0	111	NC	55	DQ16	139	DQ48	83	SCL	167	SA2
28	/CAS0	112	/CAS4	56	DQ17	140	DQ49	84	Vcc	168	Vcc

PIN NAMES

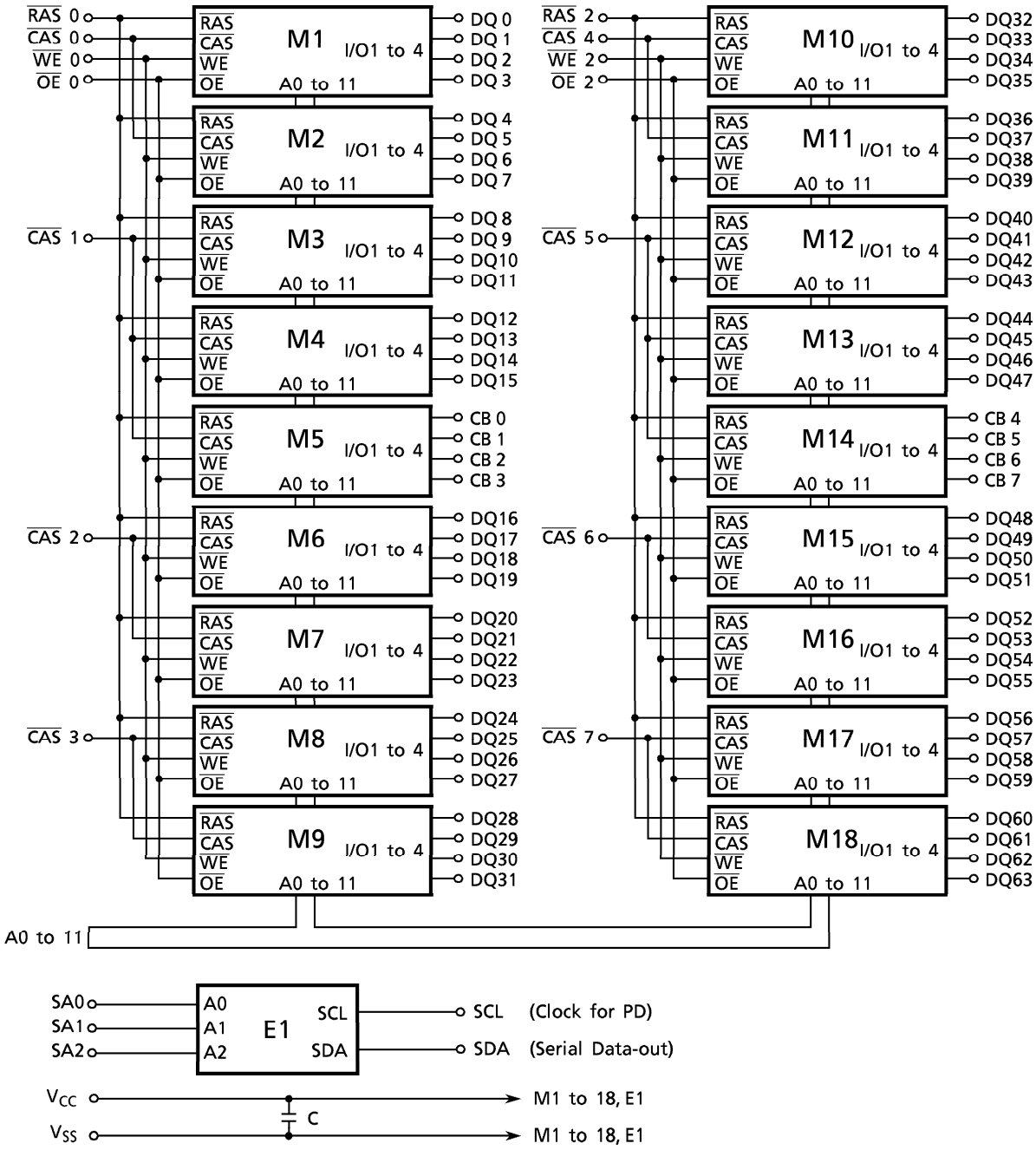
A0 to 11	Address Inputs
DQ0 to 63,CB0 to 7	Data Inputs/Outputs
$\overline{RAS}$0,2	Row Address Strobe
$\overline{CAS}$0 to 7	Column Address Strobe
$\overline{WE}$0,2	Read/Write Input
$\overline{OE}$0,2	Output Enable
V_{CC}	Power (+3.3 V)
V_{SS}	Ground
SCL	Presence Detect Clock
SDA	Serial Data-out
SA0 to 2	Serial PD Address
NC	No Connection

SERIAL PRESENCE DETECT

	-4 (hex)	-5 (hex)	Notes
Byte-0	80	80	128 bytes
Byte-1	08	08	256 bytes
Byte-2	02	02	EDO
Byte-3	0C	0C	A_R
Byte-4	0C	0C	A_C
Byte-5	01	01	DIMM Bank
Byte-6	48	48	x72
Byte-7	00	00	—
Byte-8	01	01	LVTTL
Byte-9	28	32	tRAC
Byte-10	0B	0D	tCAC
Byte-11	02	02	ECC
Byte-12	00	00	15.625 μs (Normal)
Byte-13	04	04	x4
Byte-14	04	04	ECC

961001EBA1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	– 0.3 to V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	– 0.3 to V_{CC} + 0.3	V	1
V_{CC}	Power Supply Voltage	– 0.3 to 4.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1
T_{STG}	Storage Temperature	– 55 to 125	°C	1
P_D	Power Dissipation	8.3	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	3.13	3.3	3.47	V	2
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 0.3*	V	2
V_{IL}	Input Low Voltage	– 0.3**	–	0.8	V	2

* V_{CC} + 1.2 V at pulse width ≦ 20 ns (pulse width is measured at V_{CC})

** – 1.2 V at pulse width ≦ 20 ns (pulse width is measured at V_{SS})

CAPACITANCE (V_{CC} = 3.3 V ± 5%, f = 1 MHz, Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 to 11)	–	T.B.D.	pF
C_{I2}	Input Capacitance ($\overline{WE}$0,2)	–	T.B.D.	pF
C_{I3}	Input Capacitance ($\overline{RAS}$0,2)	–	T.B.D.	pF
C_{I4}	Input Capacitance ($\overline{CAS}$0 to 7)	–	T.B.D.	pF
C_{I5}	Input Capacitance ($\overline{OE}$0,2)	–	T.B.D.	pF
C_{DQ}	I/O Capacitance (DQ0 to 63, CB0 to 7)	–	T.B.D.	pF

DC CHARACTERISTICS (V_{CC} = 3.3 V ± 5%, Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	THMxxxxxx-4	–	2160	mA	3, 4, 5
		THMxxxxxx-5	–	1800		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	18	mA	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	THMxxxxxx-4	–	2160	mA	3, 5
		THMxxxxxx-5	–	1800		
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, Address Cycling: t_{HPC} = t_{HPC} min)	THMxxxxxx-4	–	1620	mA	3, 4, 5
		THMxxxxxx-5	–	1350		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		–	9	mA	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min)	THMxxxxxx-4	–	2160	mA	3, 5
		THMxxxxxx-5	–	1800		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, Any Input (0 V ≦ V_{IN} ≦ V_{CC}, All Other Pins Not under Test = 0 V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, 0 V ≦ V_{OUT} ≦ V_{CC})		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output H Level Voltage (I_{OUT} = – 2 mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output L Level Voltage (I_{OUT} = 2 mA)		–	0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 5%, Ta = 0° to 70°C)

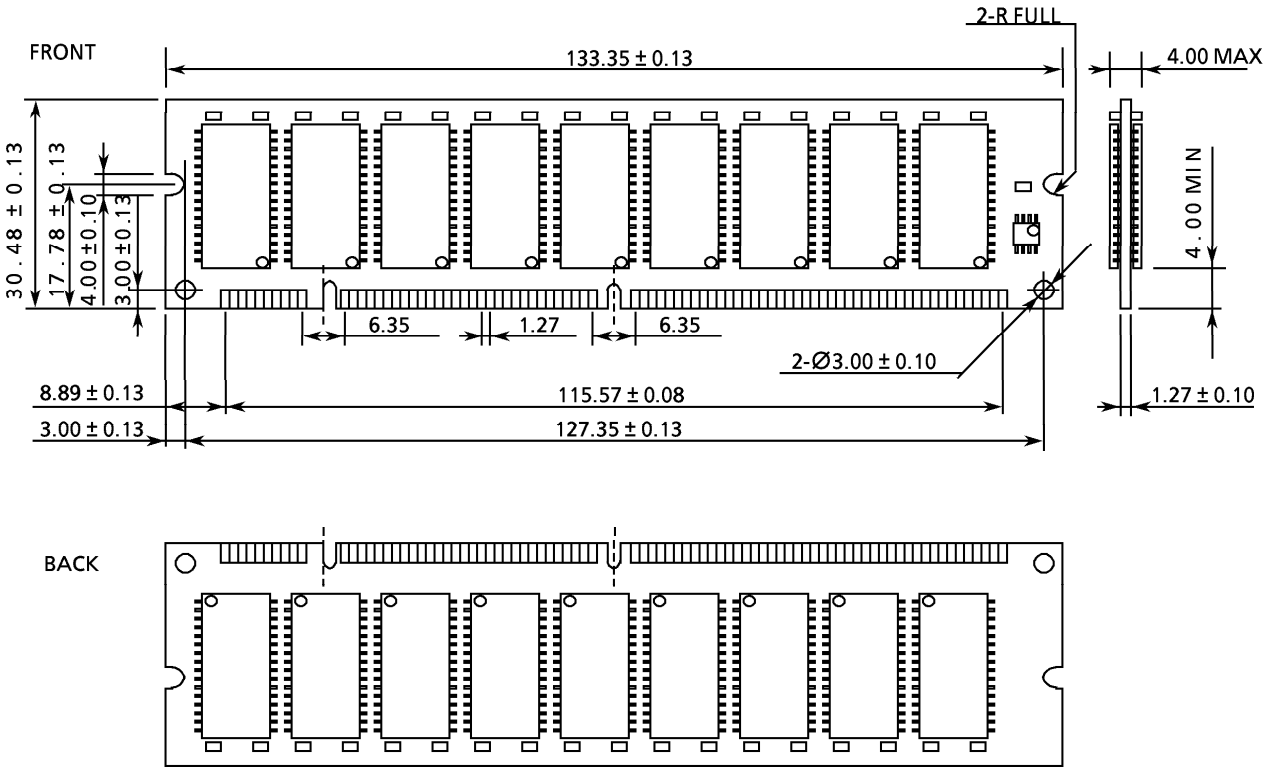
Please refer to DRAM MODULE AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No. 44

SERIAL PRESENCE DETECT AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

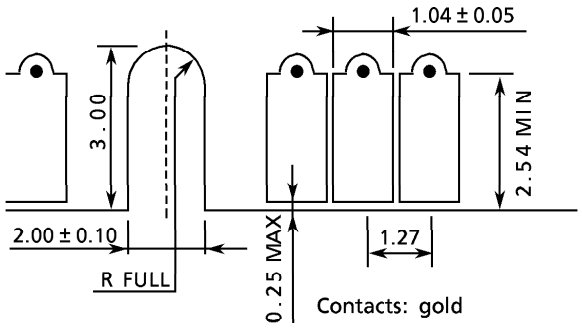
For information on SERIAL PRESENCE DETECT please refer to AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No. 100

PACKAGE DIMENSIONS (THM73V1615BTG)

Unit: mm



CONTACT DIMENSIONS



Weight: 24.4g (typ.)

DRAM MODULE
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.44

TC5164405BJ/BFT/BJS/BFTS	USING MODULE
TC5165405BJ/BFT/BJS/BFTS	USING MODULE
TC5164805BJ/BFT/BJS/BFTS	USING MODULE
TC5165805BJ/BFT/BJS/BFTS	USING MODULE
TC5164165BFT/BFTS	USING MODULE
TC5165165BFT/BFTS	USING MODULE

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	-40		-50		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	69	–	84	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	92	–	111	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	40	–	50	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	11	–	13	ns	9, 14
t_{AA}	Access Time from Column Address	–	20	–	25	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	22	–	28	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	11	0	13	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	25	–	30	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	40	10,000	50	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	6	–	8	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Hyper Page Mode)	22	–	28	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	30	–	35	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	6	10,000	8	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	29	12	37	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	8	20	10	25	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	6	–	8	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	6	–	8	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	6	–	8	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	6	–	8	–	ns	
t_{WP}	Write Command Pulse Width	6	–	8	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	6	–	8	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	6	–	8	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	6	–	8	–	ns	12

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	-40		-50		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{REF}	Refresh Period	–	64	–	64	ms	
t_{REF}	Refresh Period (Self Refresh)	–	128	–	128	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	26	–	30	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	55	–	67	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	35	–	42	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	37	–	45	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	6	–	8	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	11	–	13	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	11	–	13	–	ns	
t_{OLZ}	$\overline{OE}$ to output in Low-Z	0	–	0	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	11	0	13	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	6	–	8	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RNCD}	$\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode)	40	–	50	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	16	–	20	–	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	47	–	57	–	ns	
t_{COH}	Output Data Hold Time	5	–	5	–	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	11	0	13	ns	10, 16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	11	0	13	ns	10
t_{WED}	$\overline{WE}$ to Data Delay	11	–	13	–	ns	
t_{OE}	$\overline{OE}$ Pulse Width	11	–	13	–	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	6	–	8	–	ns	
t_{CPO}	$\overline{CAS}$ to $\overline{OE}$ Precharge Time	5	–	5	–	ns	
t_{OCH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$	6	–	8	–	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	100	–	100	–	μs	
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self refresh)	69	–	84	–	ns	
t_{CHS}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self refresh)	-50	–	-50	–	ns	

NOTES:

1. Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on the cycle rate.
4. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while $\overline{RAS}=V_{IL}$. In the case of I_{CC4}, it can be changed once at most during a Hyper Page Mode cycle (t_{HPC}).
6. An initial pause of 200μs is required after power-up followed by a minimum of eight $\overline{RAS}$-Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles instead of eight $\overline{RAS}$-Only refresh cycles is required.
7. AC measurements assume $t_T=2$ns.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the V_{IH} and V_{IL} levels.
9. This is measured with a load equivalent to 100pF at V_{OH} = 2.0V (I_{OUT} = −2mA), V_{OL} = 0.8V (I_{OUT} = 2mA).
10. t_{OFF} (max), t_{OEZ} (max), t_{REZ} (max) and t_{WEZ} (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of $\overline{CAS}$ in Early Write cycles and to the leading edge of $\overline{WE}$ in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then the access time is determined by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then the access time is determined by t_{AA}.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the output goes open circuit when $\overline{CAS}$ goes high (t_{OFF}).
    If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the output goes open circuit when $\overline{RAS}$ goes high (t_{REZ}).

DATA-OUT HI-Z CONTROL LOGIC

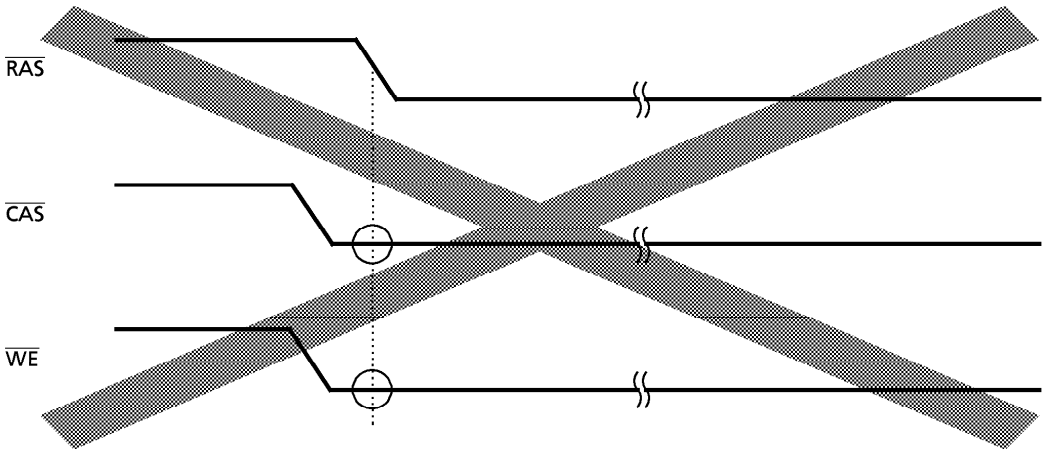
$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
H	↑	L	H	t_{OFF}
↑	H	L	H	t_{REZ}
L	L	↑	H	t_{OEZ}
L	H	L	↓	t_{WEZ}

DATA-OUT LO-Z CONTROL LOGIC

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
L	↓	L	H	t_{CLZ}
L	L	↓	H	t_{OLZ}
L	L	↓↑	H	t_{OLZ}

CAUTION

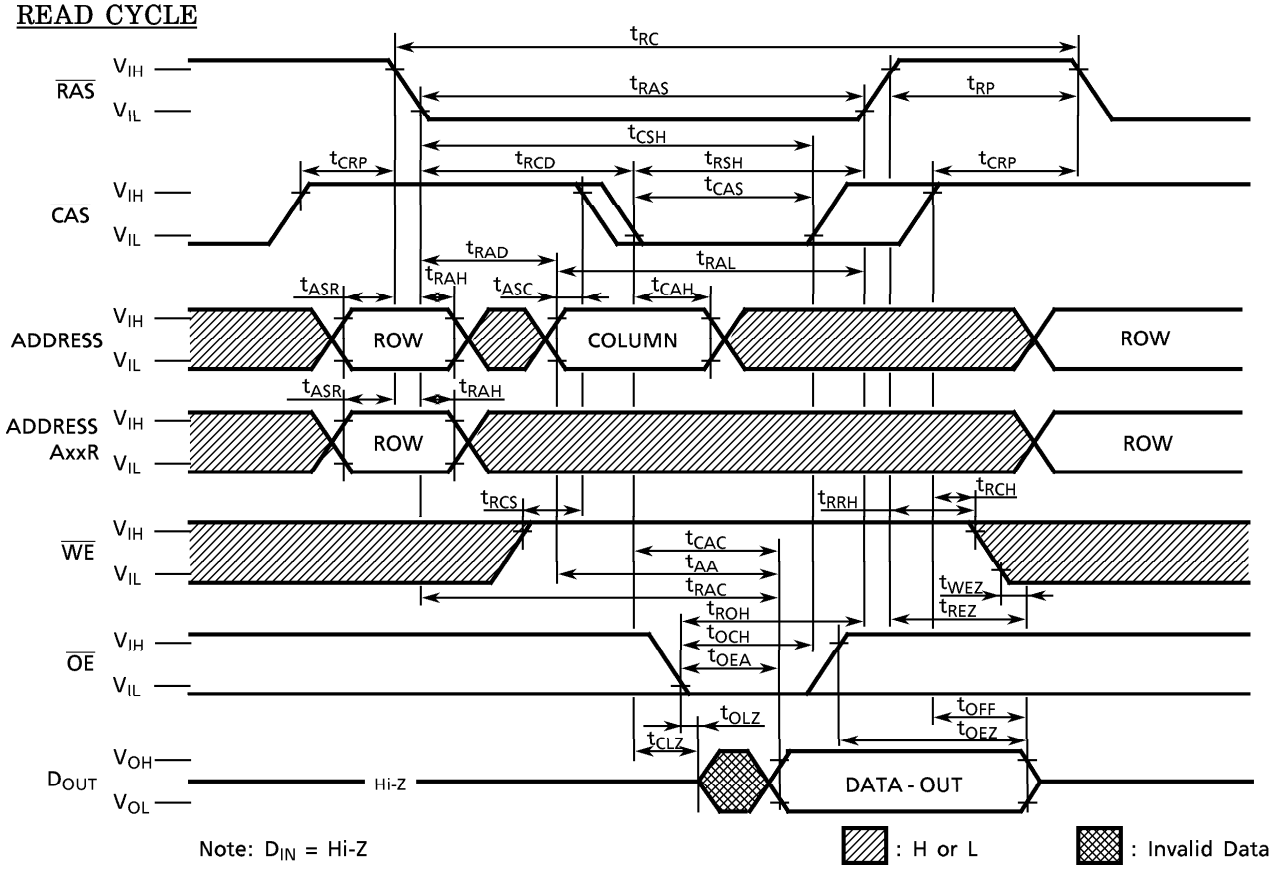
The WCBR ($\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.



WCBR timing

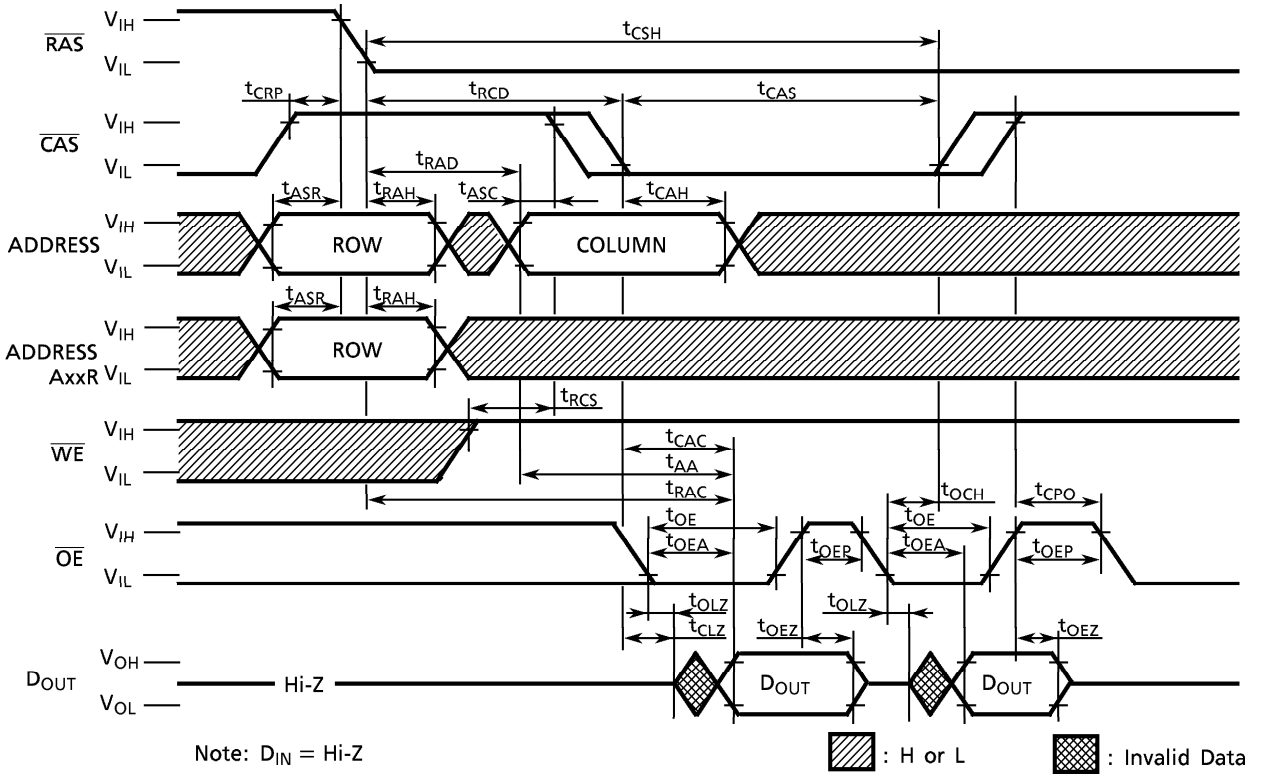
TIMING DIAGRAMS

READ CYCLE



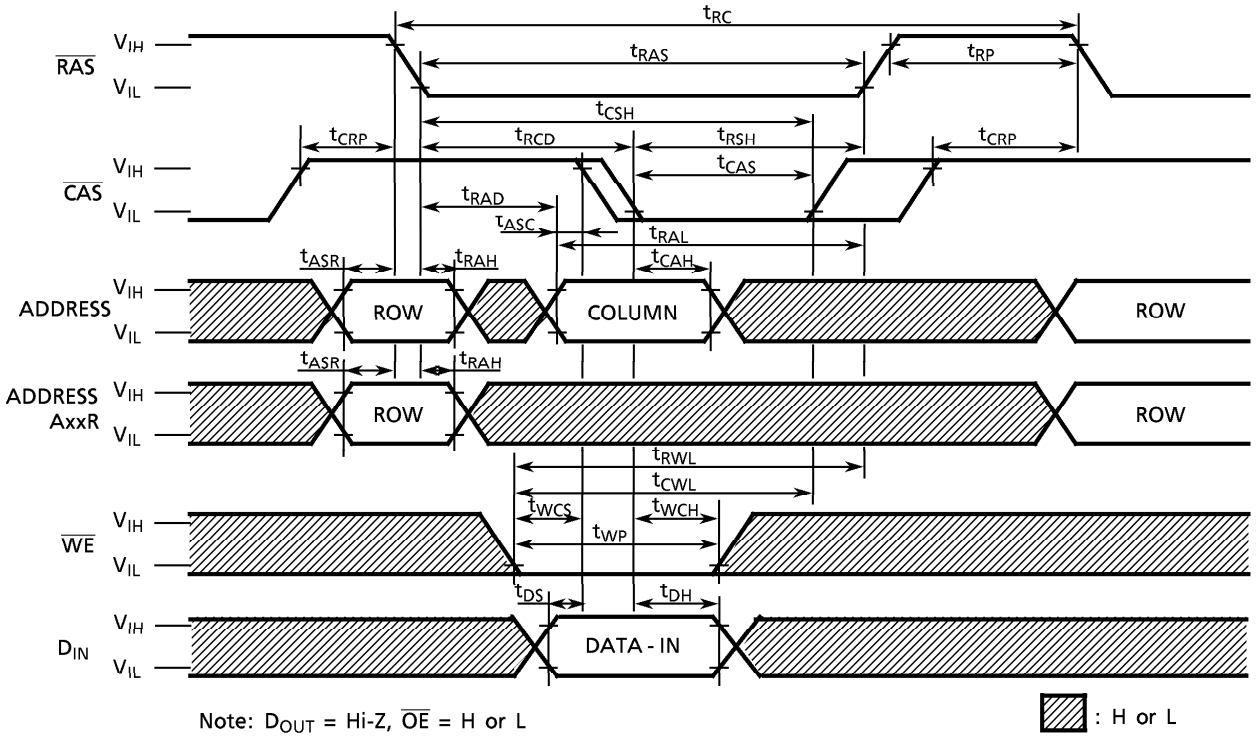
Note: D_{IN} = Hi-Z : H or L : Invalid Data

$\overline{OE}$-CONTROLLED READ CYCLE



Note: D_{IN} = Hi-Z : H or L : Invalid Data

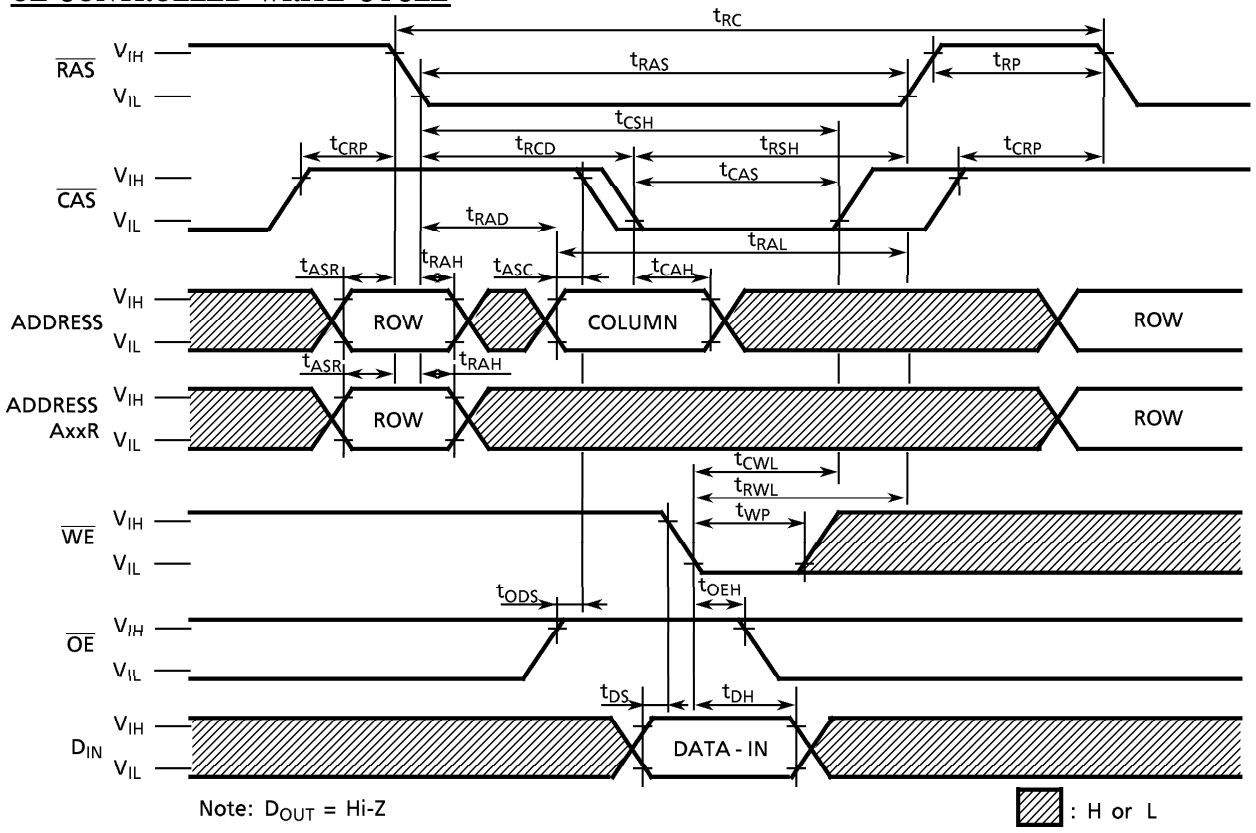
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z, $\overline{OE}$ = H or L

: H or L

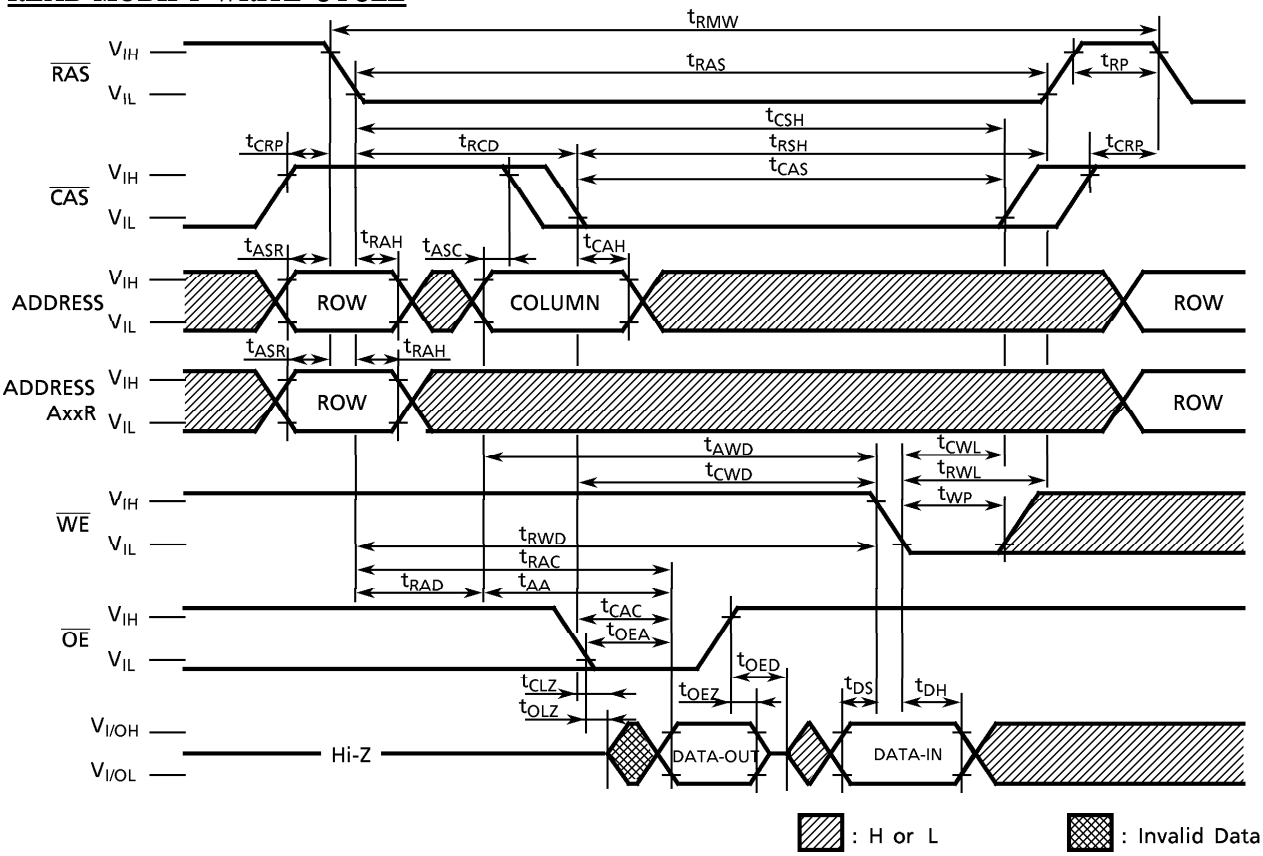
$\overline{OE}$-CONTROLLED WRITE CYCLE



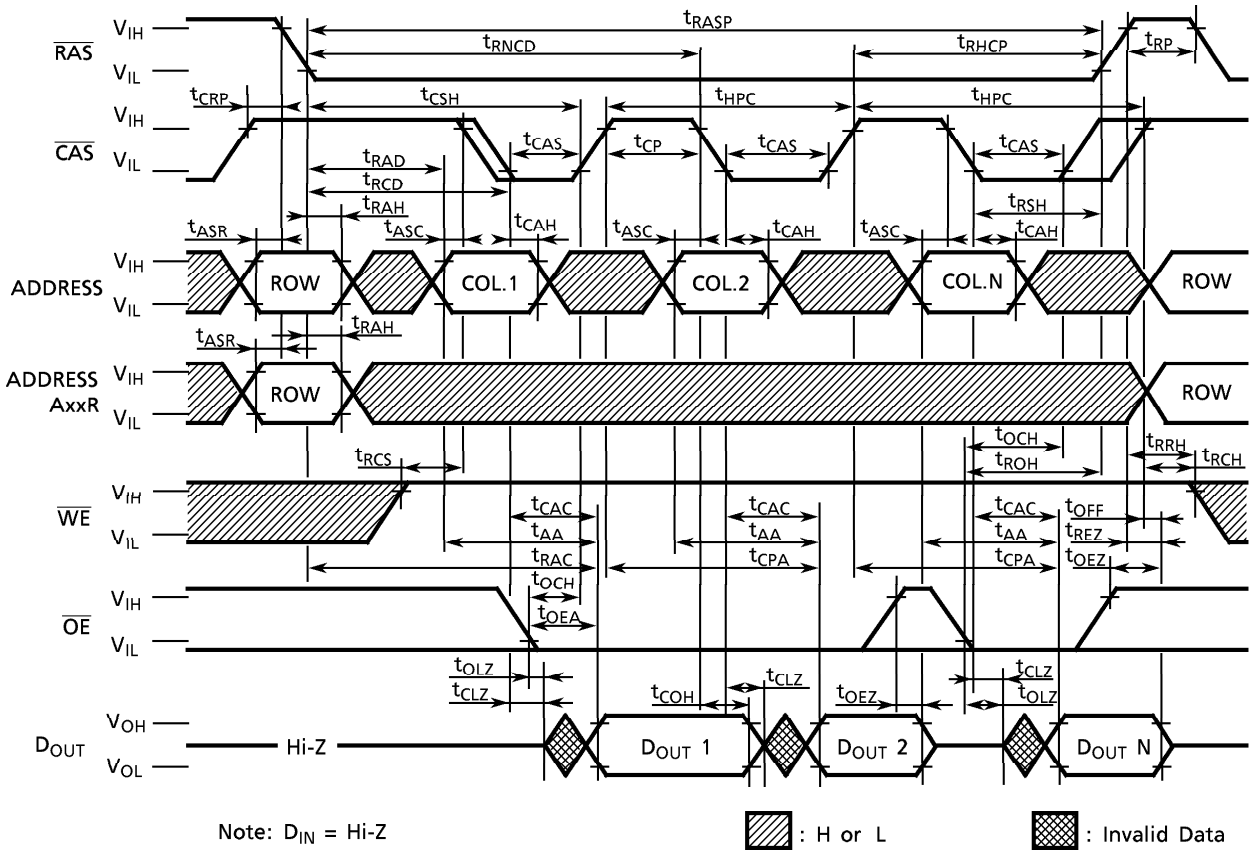
Note: D_{OUT} = Hi-Z

: H or L

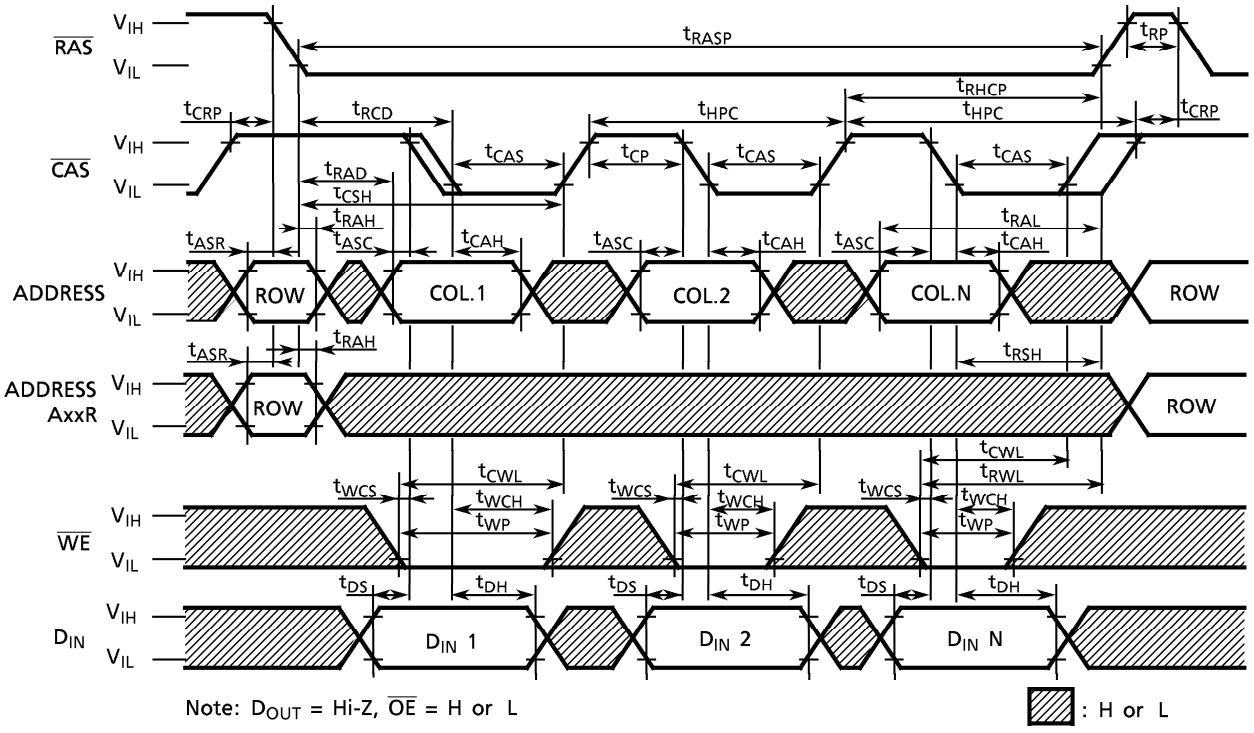
READ-MODIFY-WRITE CYCLE



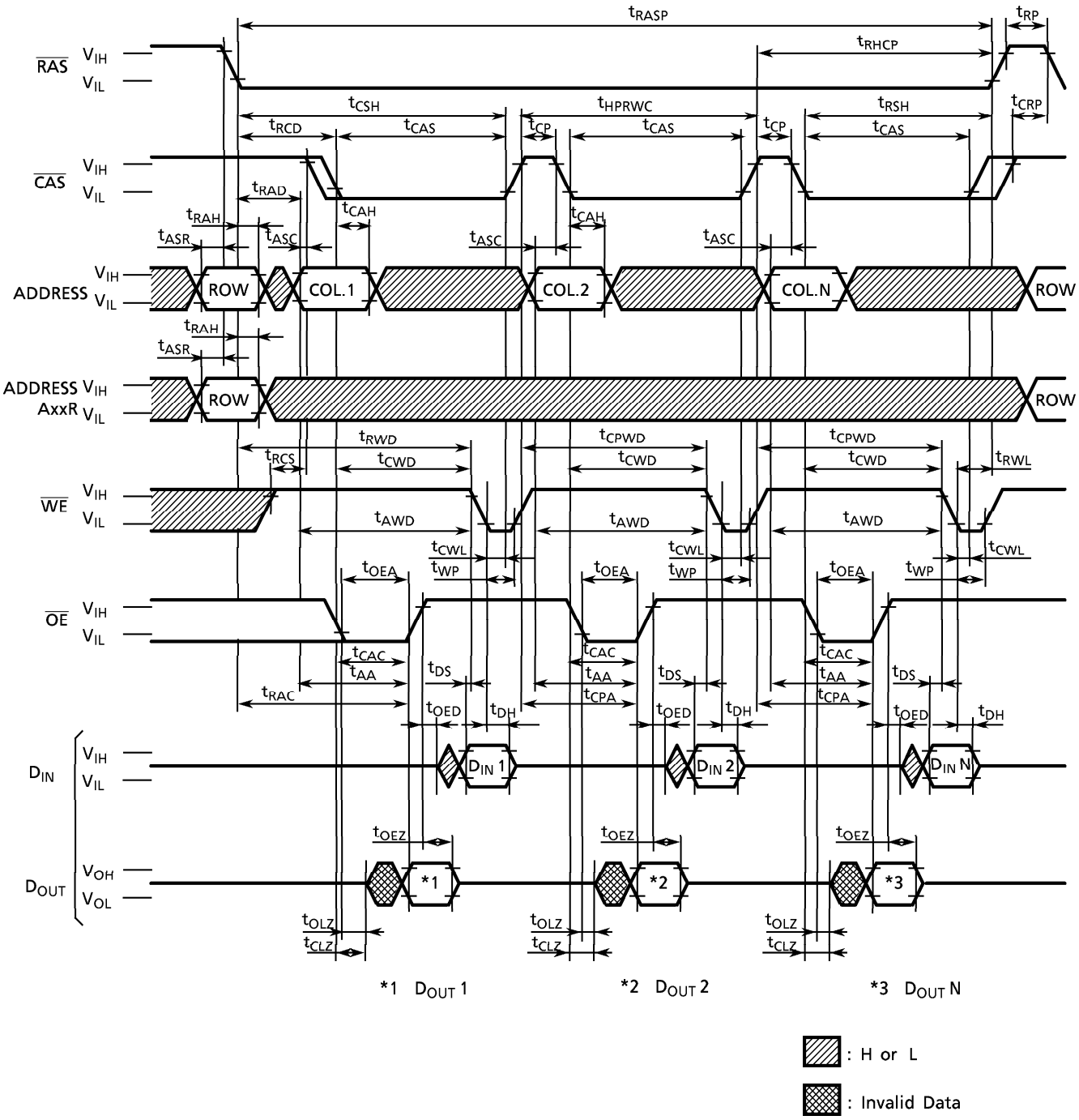
HYPER PAGE MODE READ CYCLE



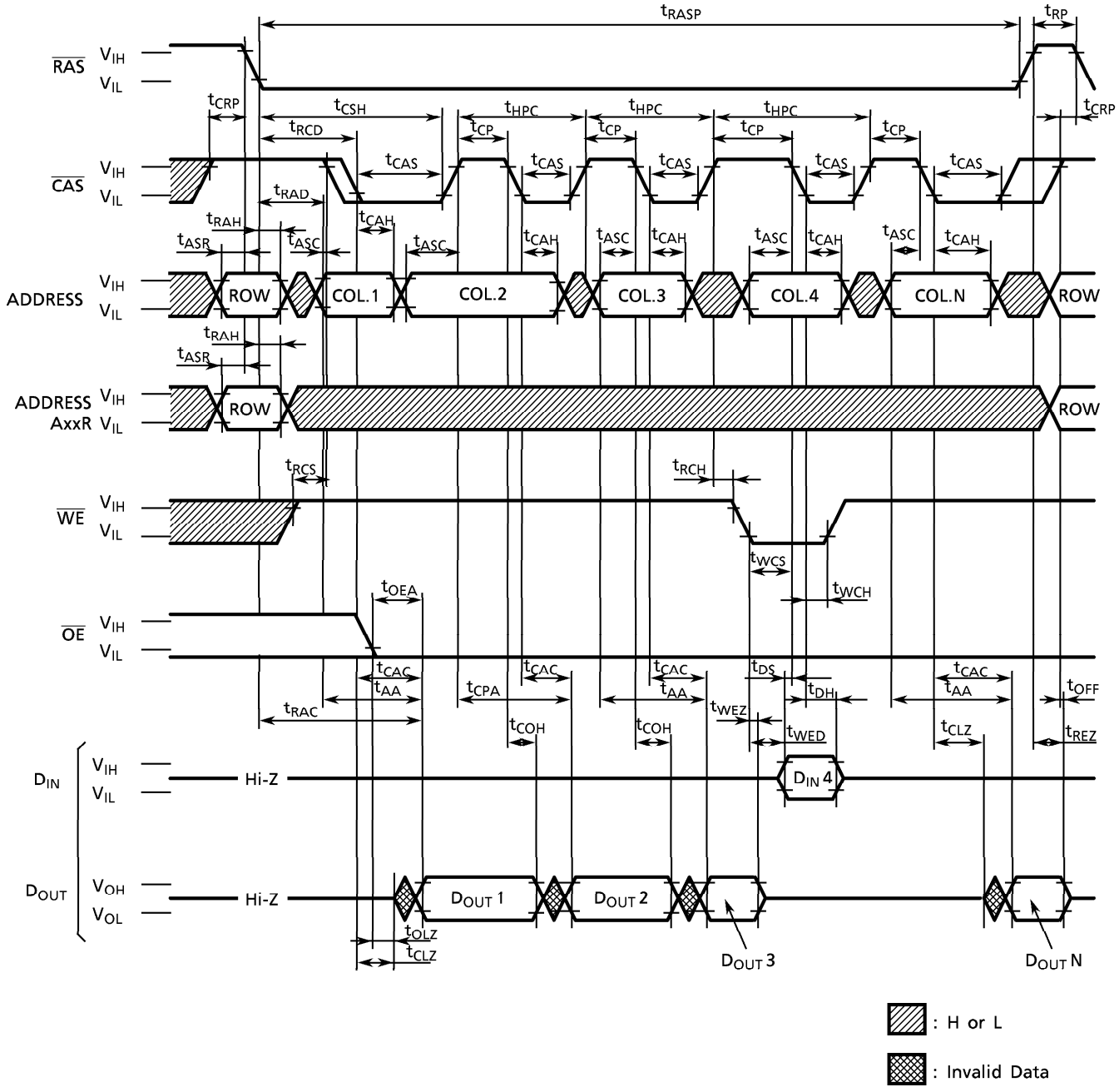
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



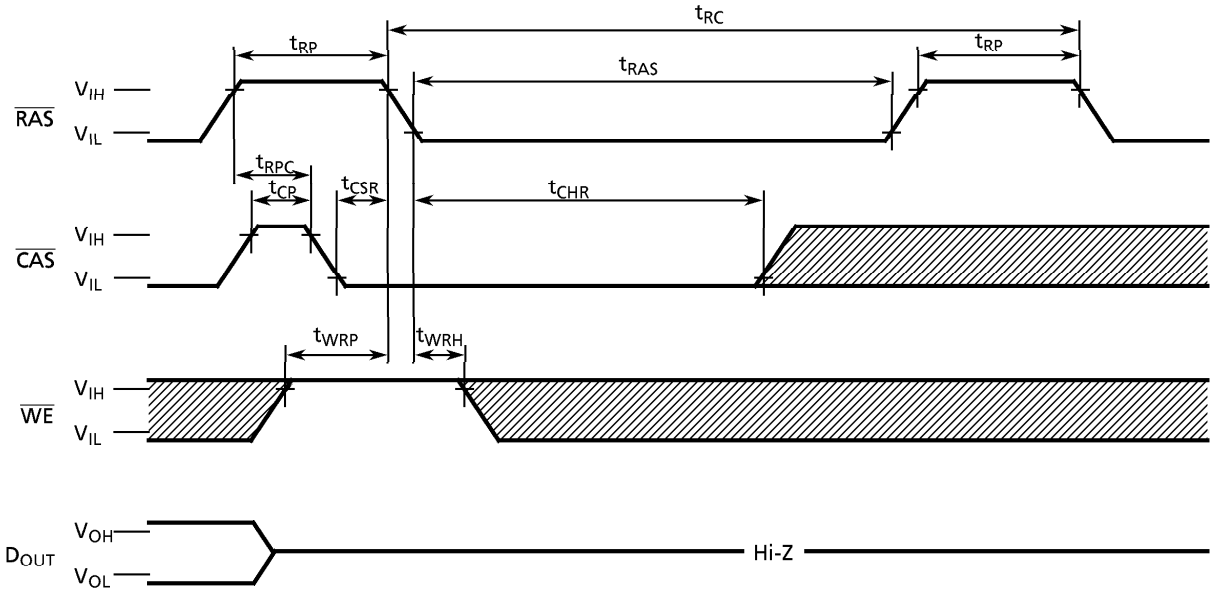
HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE READ-WRITE MIXED CYCLE



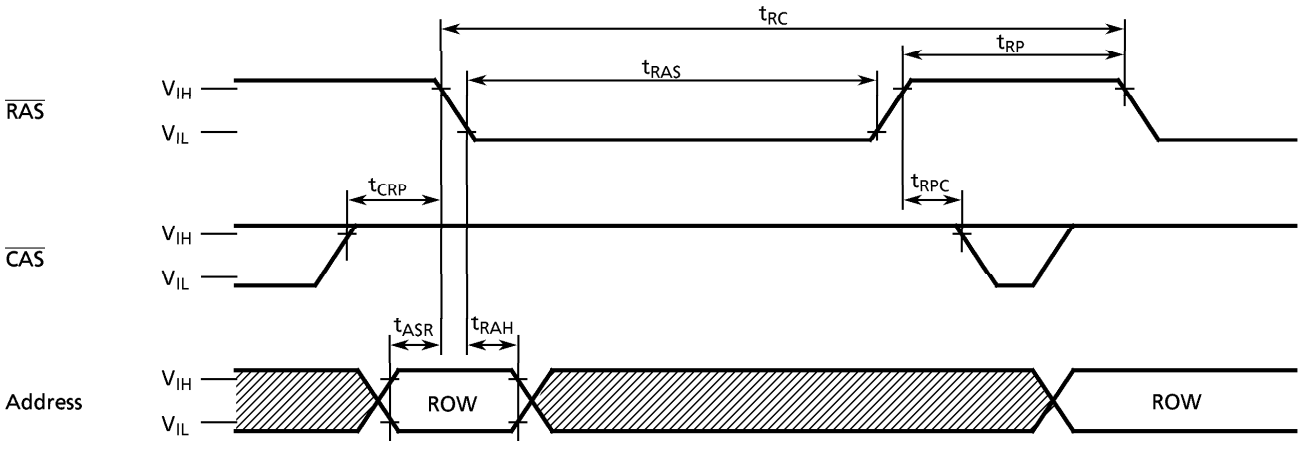
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, ADDRESS = H or L

▨ : H or L

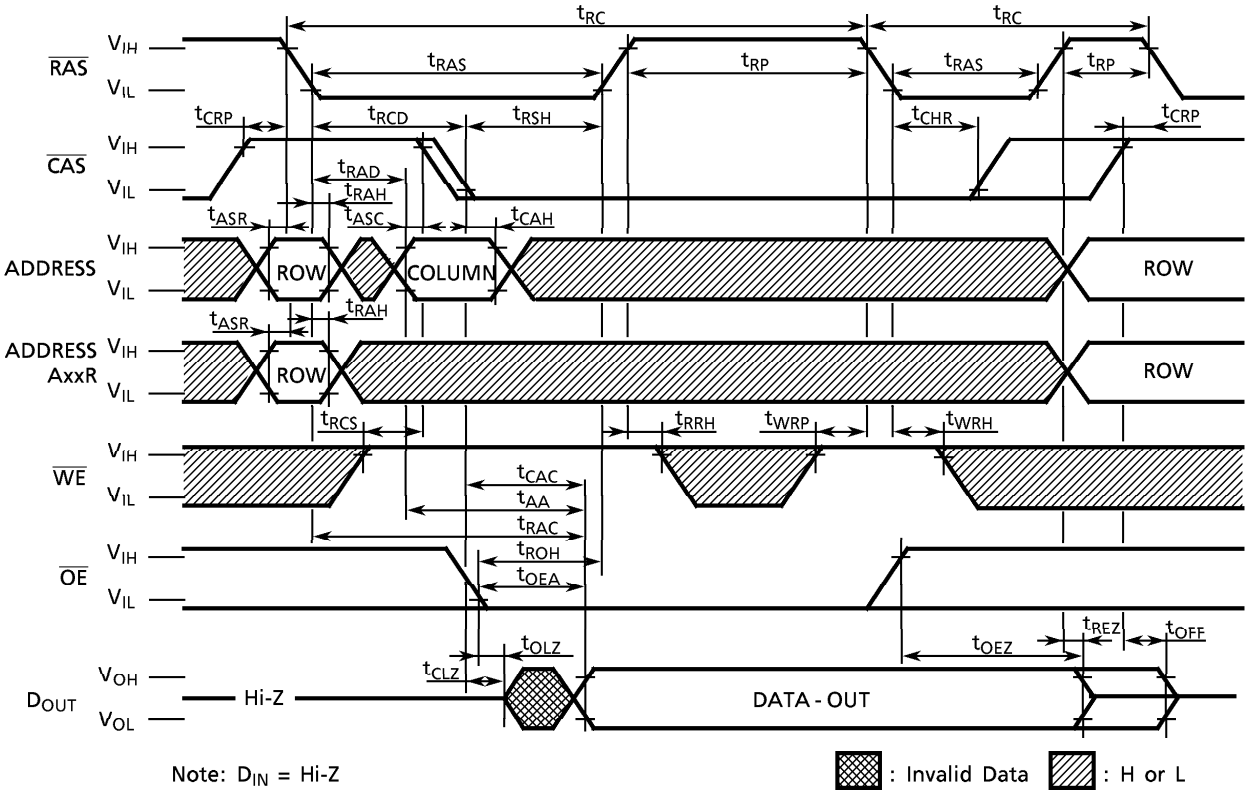
$\overline{RAS}$-ONLY REFRESH CYCLE



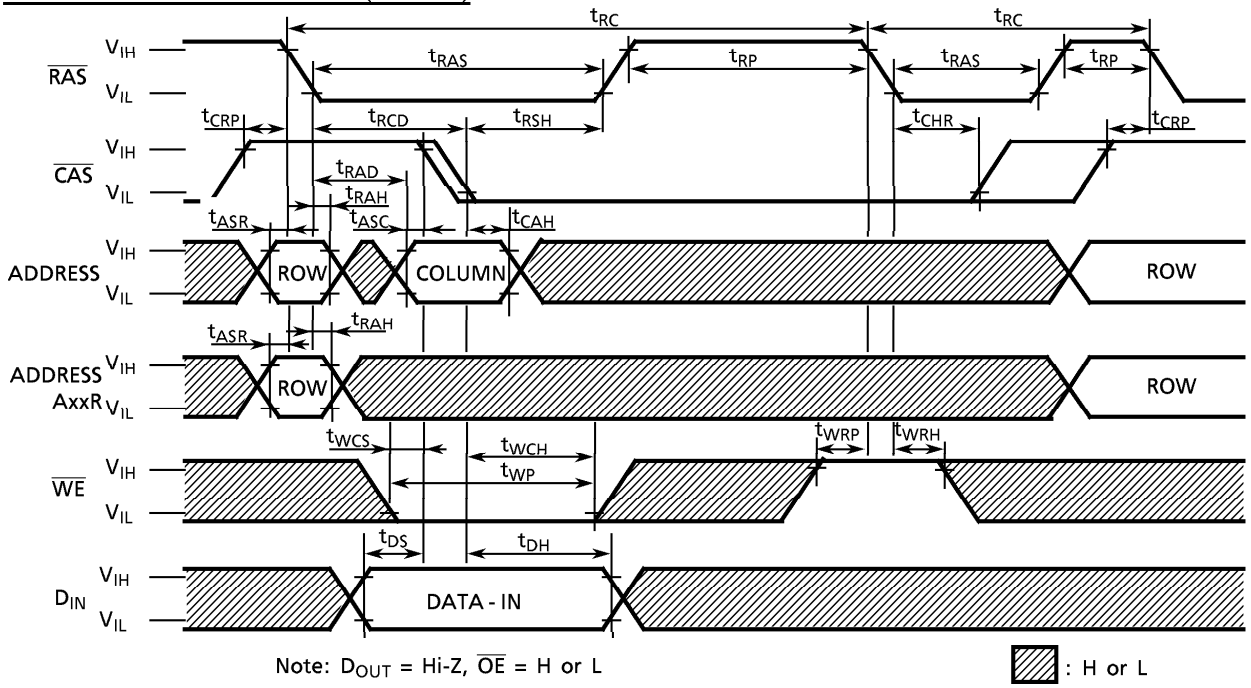
Note: $\overline{WE}$, $\overline{OE}$ and D_{IN} = H or L

▨ : H or L

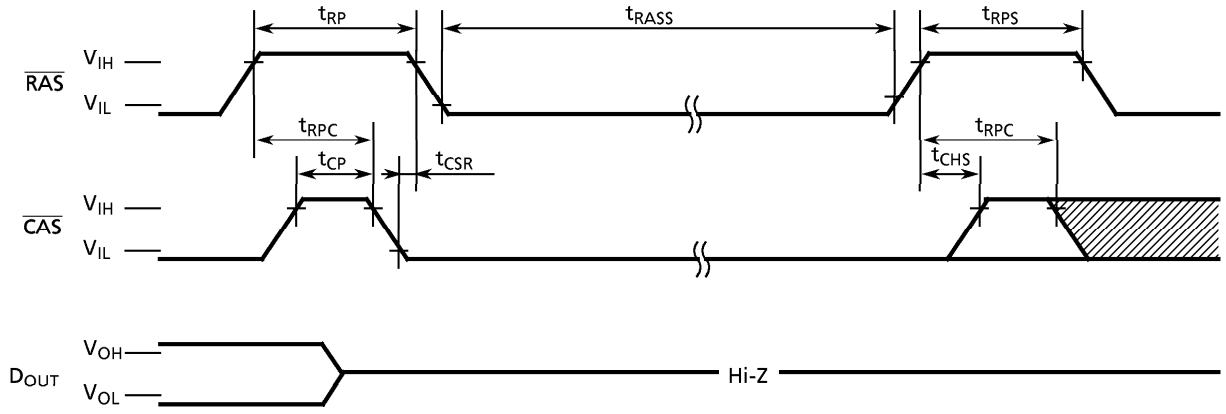
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF-REFRESH CYCLE (THL64VxxxxBTG-xS only)



Note: D_{IN}, $\overline{WE}$, $\overline{OE}$, ADDRESS = H or L

: H or L

SERIAL PRESENCE DETECT AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.100

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ± 0.15 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{IH}	Input High Voltage	V_{CC} × 0.7	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage	–0.3	V_{CC} × 0.3	V	
V_{OL}	Output Low Voltage (I_{OL} = 200 μA)	–	0.4	V	1

Note:

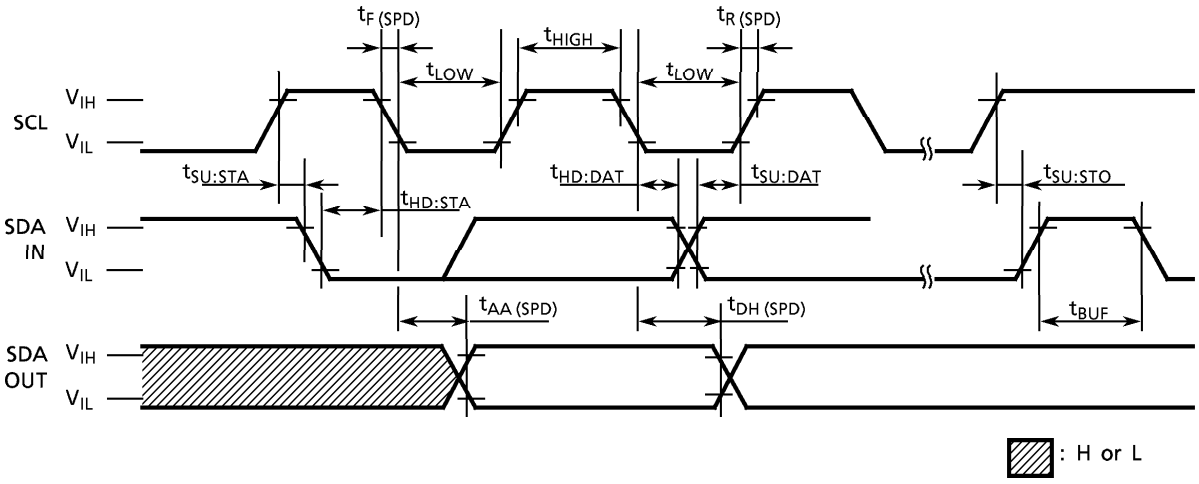
1. Output Load: 1TTL Gate and C_L = 100 pF

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

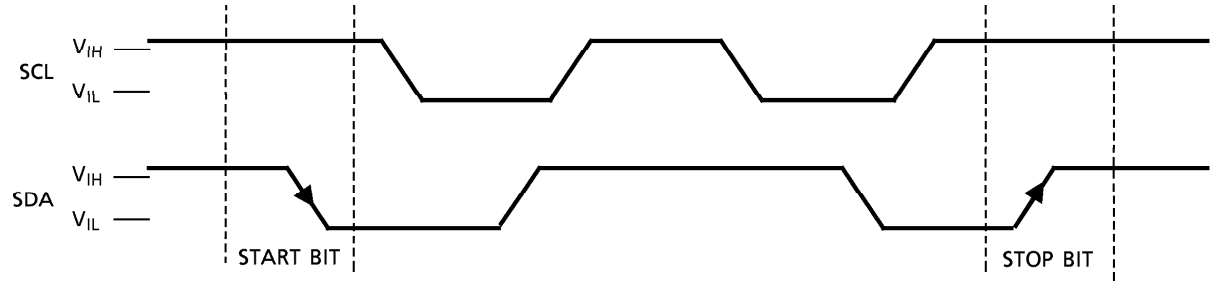
SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{SCL}	SCL Clock Frequency	–	80	KH_Z	
t_{LOW}	Clock Low Period	6.7	–	μs	
t_{HIGH}	Clock High Period	4.5	–	μs	
$t_{AA\ (SPD)}$	SCL Low to SDA Data Out Valid	0.3	7.0	μs	
$t_{HD\ :\ STA}$	Start Condition Hold Time	4.5	–	μs	
$t_{SU\ :\ STA}$	Start Condition Set-up Time (for a Repeated Start Condition)	6.7	–	μs	
$t_{SU\ :\ STO}$	Stop Condition Set-up Time	6.7	–	μs	
$t_{HD\ :\ DAT}$	Data-in Hold Time	0	–	μs	
$t_{SU\ :\ DAT}$	Data-in Set-up Time	500	–	ns	
$t_{DH\ (SPD)}$	Data-out Hold Time	300	–	ns	
$t_{R\ (SPD)}$	SDA and SCL Rise Time	–	1	μs	
$t_{F\ (SPD)}$	SDA and SCL Fall Time	–	300	ns	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7	–	μs	

TIMING DIAGRAMS

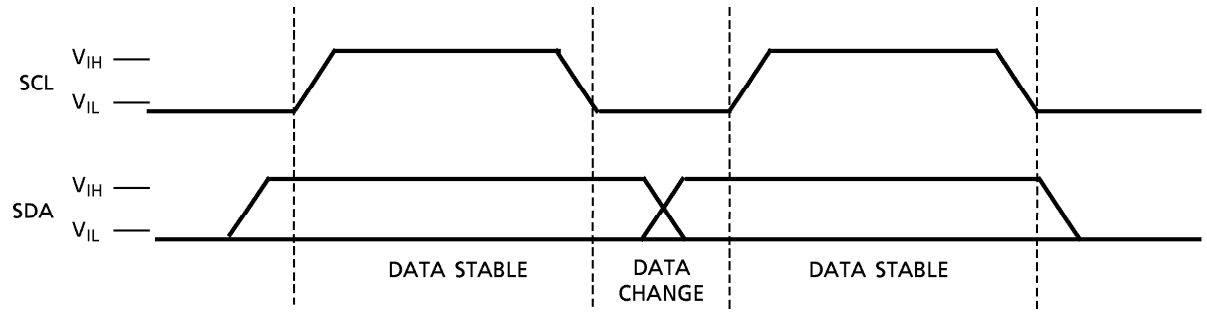
BUS TIMING



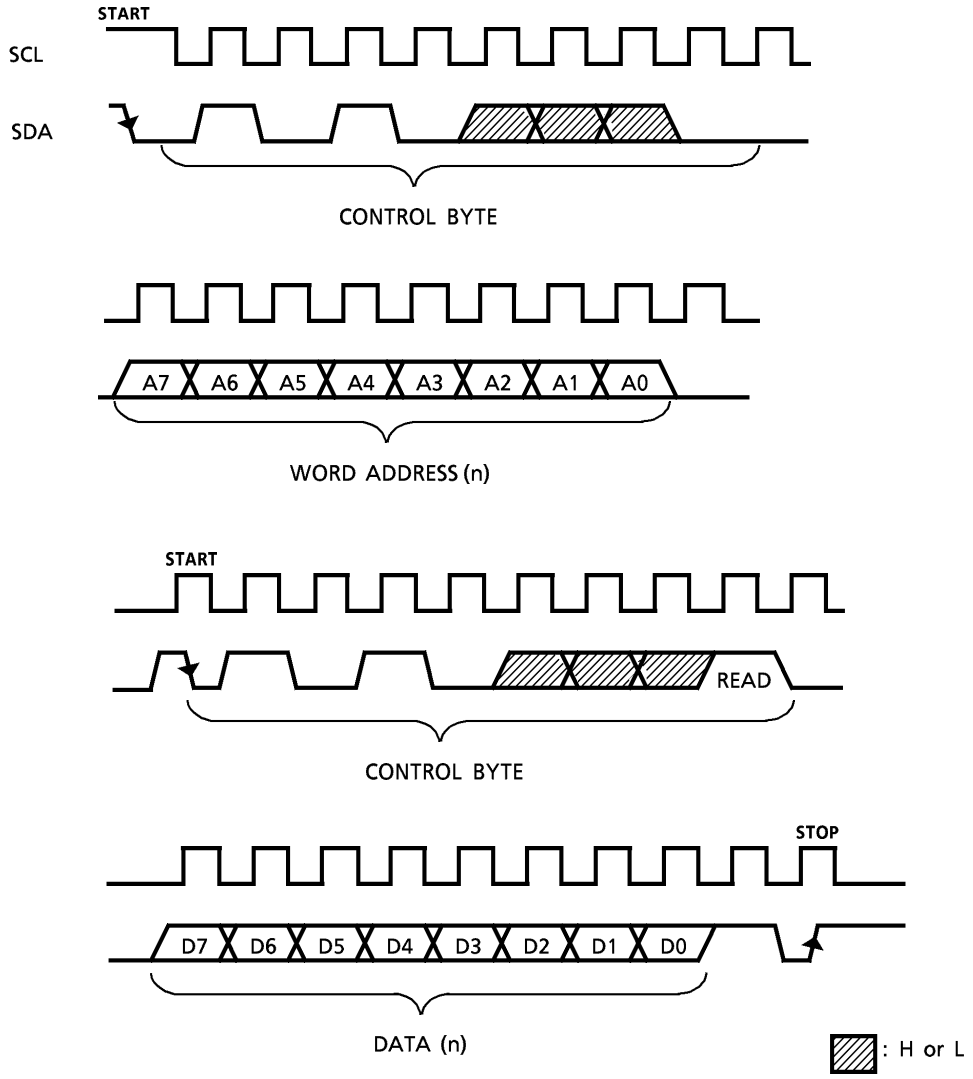
DEFINITION OF START AND STOP



DATA VALIDITY

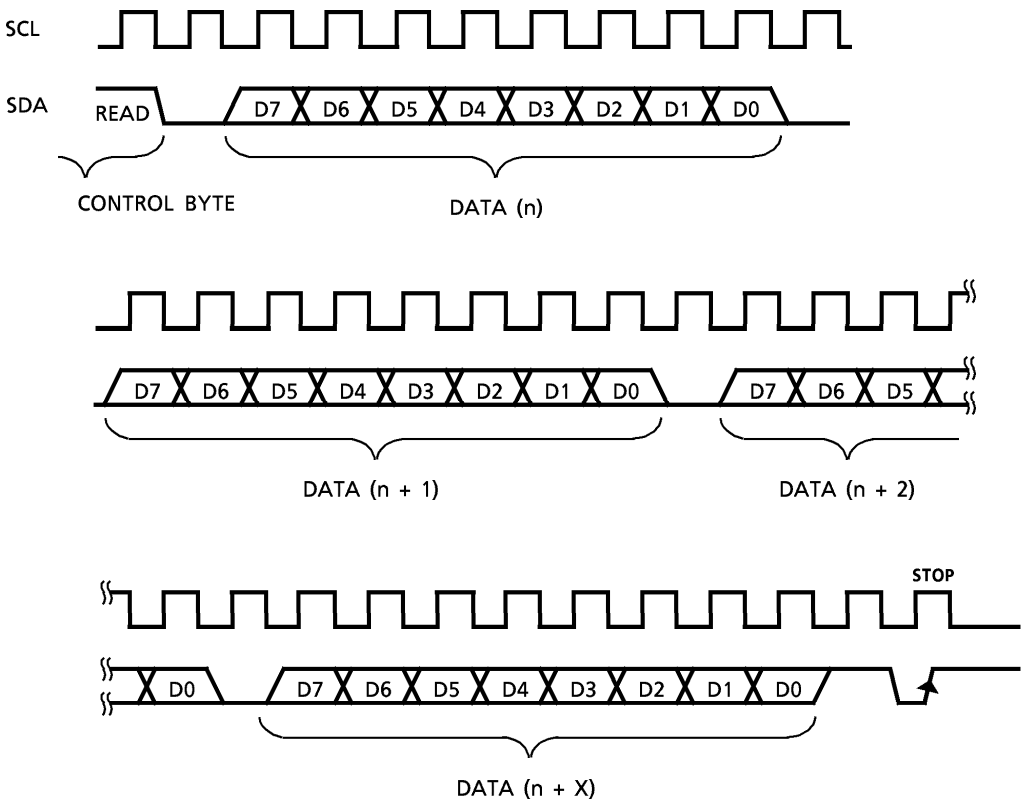


RANDOM READ



NOTE: Random read operations allow the master to access Serial PD DATA in a random manner.
To perform this type of read operation, first the word address must be set. (Dummy Write Operation)
After the word address is sent, the master generates a start condition following the acknowledge.
Then the master issues the control byte again but with READ bit set to a one.
E^2PROM will then issue an acknowledge and transmits the eight bit data word.

SEQUENTIAL READ



NOTE: Sequential reads can be initiated as random access read. The first word is transmitted in the same manner as the other read mode; however, the master now responds with an acknowledge, indicating it requires additional data.
E^2PROM continues to output data for each acknowledge received.
The read operation is terminated by generating a stop condition.