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FUJITSU

DATA SHEET

MB87085
ANALOG PROCESSOR LSI

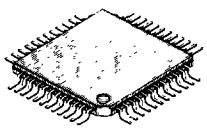
AUDIO PROCESSOR LSI

The Fujitsu MB87085 is an audio processor LSI for cellular radio application, fabricated in Fujitsu Advanced CMOS Technology.

The MB87085 contains filter, electronic volume and limiter circuit.

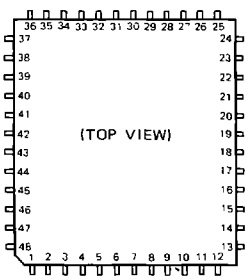
The MB87085 is designed for AMPS (U.S.), TACS (U.K.) and NMT (Scandinavia) systems and is used with the Fujitsu MB87084 Analog Processor LSI.

- AMPS, TACS or NMT mode is selected by select pin.
- Limiter circuit suppresses an instantaneous frequency deviation in FM modulation.
- Differential input structure prevents input noise of transmit section.
- Not required external parts of filter because filter consists of SCF is on chip. This enables stable performance.
- Electronic volume gain is digitally controlled for precision.
- Mute control of transmit/reception circuits are achieved respectively.
- Output pins for compressor and expander are provided.
- Power down mode is achieved by stand-by control function.
- Filter characteristics, electronic volume and stand-by mode are easily set by serial data input.
- I/O's are TTL compatible.



PLASTIC PACKAGE
FPT-48P-M02

PIN ASSIGNMENT



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ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Pin Name	Value	Unit
Supply Voltage	V_{DD}	V_{DD}	-0.3 to 7	V
Input Voltage	V_{IN}	All input pins	-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	All output pins	-0.3 to V_{DD}+0.3	V
Output Current	I_{OUT}	All output pins	-10 to 10	mA
Storage Temperature	T_{STG}		-40 to 85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I	TAM	17	I	DEM	33	I	TVDD/2
2	I	BYPASS	18	O	MSK	34		N.C.
3	I	RAM	19	P	V_{DD}	35	I	COMP2
4		N.C.	20	O	AFOUT	36		N.C.
5	I	DATA	21	I	TONE	37	O	RT1
6	I	CLK	22	O	RR3	38	I	RT2
7	I	STB	23	I	RR2	39	O	RT3
8	I	$\overline{\text{RESET}}$	24	O	RR1	40		N.C.
9	I	CLOCK	25	I	EXP2	41	O	C1
10	P	DG	26	O	EXP1	42	I	C2
11		N.C.	27	O	RE3	43	P	V_{DD}
12	O	TVDD2	28	I	RE2	44	I	AFIN (−)
13	O	TREF	29	O	RE1	45	I	AFIN (+)
14	O	RREF	30	I	RVDD/2	46		N.C.
15	O	RVDD2	31	P	AG	47	O	MOD
16		N.C.	32	O	COMP1	48	I	AN

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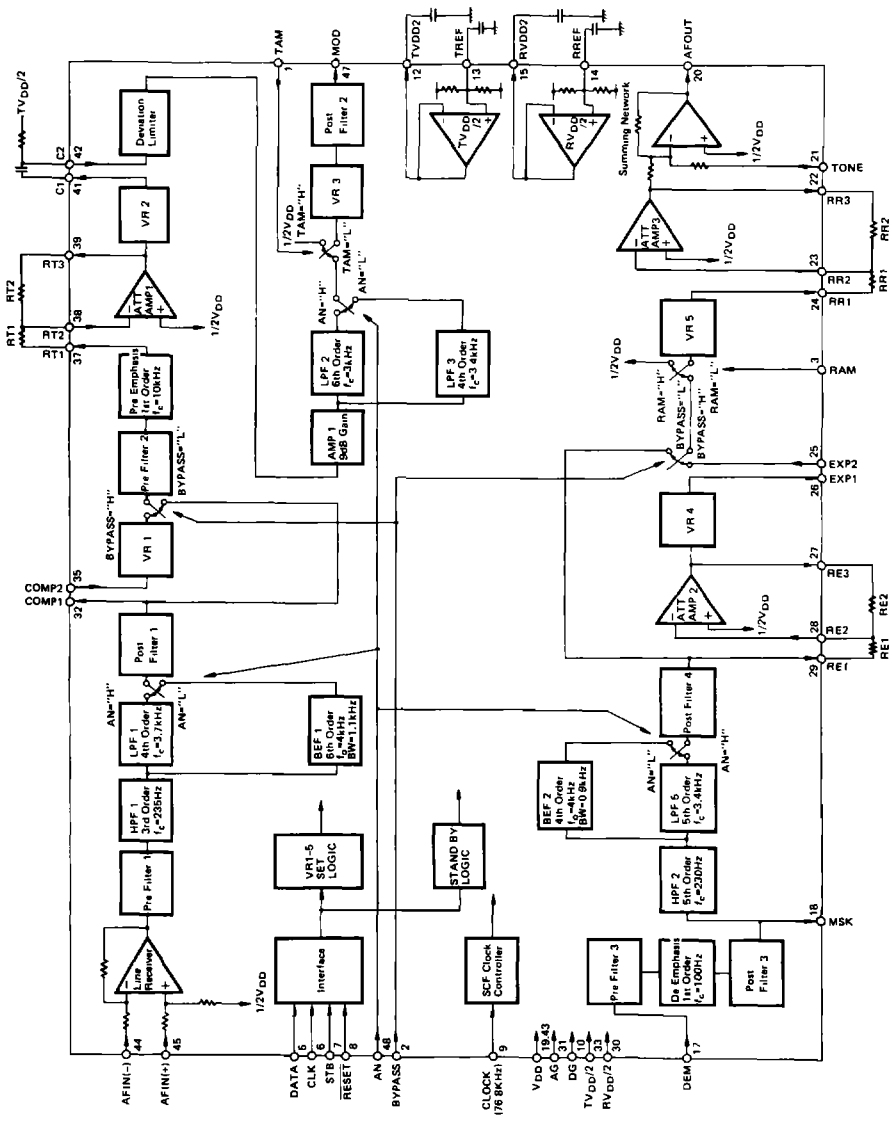
Fig. 1 – MB87085 BLOCK DIAGRAM



PIN DESCRIPTIONS

<table>
<tr><th>I/O</th><th>Pin No.</th><th>Pin Name</th><th>Descriptions</th></tr>
<tr><td rowspan="15">Input Pins</td><td>19, 43</td><td>V_{DD}</td><td>Power supply voltage input. (V_{DD} = 5V±10%)</td></tr>
<tr><td>31</td><td>AG</td><td>Ground for analog circuit.</td></tr>
<tr><td>10</td><td>DG</td><td>Ground for digital circuit.</td></tr>
<tr><td>45</td><td>AFIN (+)</td><td>Differential input (+) to transmit section.</td></tr>
<tr><td>44</td><td>AFIN (–)</td><td>Differential input (–) to transmit section.</td></tr>
<tr><td>48</td><td>AN</td><td>Filter characteristics select input.
When low, NMT filter is selected. When high, AMPS and TACS filter is selected.</td></tr>
<tr><td>2</td><td>BYPASS</td><td>Internal circuit bypass control signal input.
When low, transmit VR1 (external compressor) and reception VR4, ATTAMP2 (external expander) are bypassed.</td></tr>
<tr><td>1</td><td>TAM</td><td>Transmit mute control signal input.
When high, transmit filter output signal is muted.</td></tr>
<tr><td>3</td><td>RAM</td><td>Reception mute control signal input.
When high, reception filter output signal is muted.</td></tr>
<tr><td>5</td><td>DATA</td><td>The 25-bit of serial data input.</td></tr>
<tr><td>6</td><td>CLK</td><td>Clock input for 25-bit serial shift register.
On rising edge of CLK signal, one bit of serial data is shifted into the serial shift register.</td></tr>
<tr><td>7</td><td>STB</td><td>Strobe signal input.
On rising edge of STB signal, the data is stored in buffer register.</td></tr>
<tr><td>8</td><td>$\overline{RESET}$</td><td>Reset signal input.
When low, the data stored in the buffer register is reset as follows. When high, stored data is kept.
<table>
<tr><th></th><th>S5</th><th>S4</th><th>S3</th><th>S2</th><th>S1</th><th>Gain</th><th>SB1</th><th>SB2</th></tr>
<tr><td>VR1, 4</td><td>–</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0dB</td><td rowspan="3">H</td><td rowspan="3">H</td></tr>
<tr><td>VR2, 3</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0dB</td></tr>
<tr><td>VR5</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0dB</td></tr>
</table></td></tr>
<tr><td>9</td><td>CLOCK</td><td>Reference clock (768kHz) input for switched capacitor filter (SCF).</td></tr>
<tr><td>17</td><td>DEM</td><td>Reception signal input.
Input for pre filter 3.</td></tr>
<tr><td>35</td><td>COMP2</td><td>Signal input from an external compressor.
When BYPASS pin is set low, this input signal is ignored.</td></tr>
</table>

PIN DESCRIPTIONS (continued)

I/O	Pin No.	Pin Name	Descriptions
Input Pins	25	EXP2	Signal input from an external expander. When BYPASS pin is set low, this input signal is ingored.
	21	TONE	Reception adder input. After filtering an input signal from DEM pin, output the signal added with TONE signal to AFOUT pin.
	42	C2	Limiter circuit input. After cutting DC level signal by a condenser placed between C1 and C2 pins is input.
	38	RT2	Transmit gain control signal input. External resistor RT1 and RT2 at pins RT1, RT2 and RT3 set the gain of ATTAMP1 (−15dB to +5dB) given by: Gain $G = -\frac{R_{T2}}{R_{T1}}$
	28	RE2	Reception gain control signal input. External resistor RE1 and RE2 at pins RE1, RE2 and RE3 set the gain of ATTAMP2 (0dB to +20dB) given by: Gain $G = -\frac{R_{E2}}{R_{E1}}$
	23	RR2	Reception gain control signal input. External resistor RR1 and RR2 at pins RR1, RR2 and RR3 set the gain of ATTAMP3 (−10dB to +10dB) given by: Gain $G = -\frac{R_{R2}}{R_{R1}}$
	33	TVDD/2	Transmit reference level $(1/2 \cdot V_{DD})$ input. Please connect this pin and TVDD2 pin together externally. Transmit analog circuit operates referenced to this input level.
	30	RVDD/2	Reception reference level $(1/2 \cdot V_{DD})$ input. Please connect this pin and RVDD2 pin together externally. Reception analog circuit operates referenced to this input level.
Output Pins	32	COMP1	Output for an external compressor.
	26	EXP1	Output for an external expander.
	18	MSK	Output of reception de emphasis circuit. After De Emphasising, an input signal from DEM pin is output.
	47	MOD	Output of transmit section.
	20	AFOUT	Output of reception section.

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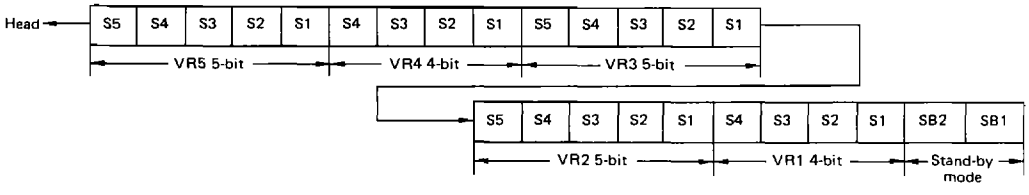
PIN DESCRIPTIONS (continued)

I/O	Pin No.	Pin Name	Descriptions
Output Pins	37	RT1	Transmit gain control signal output. Transmit gain of ATTAMP1 (−15dB to +5dB) is controlled by external resistors. Gain $G = -\frac{R_{T2}}{R_{T1}}$
	39	RT3	Transmit gain control signal output. Transmit gain of ATTAMP1 (−15dB to +5dB) is controlled by external resistors. Gain $G = -\frac{R_{T2}}{R_{T1}}$
	29	RE1	Reception gain control signal output. Reception gain of ATTAMP2 (0dB to +20dB) is controlled by external resistors. Gain $G = -\frac{R_{E2}}{R_{E1}}$
	27	RE3	Reception gain control signal output. Reception gain of ATTAMP2 (0dB to +20dB) is cotrolled by external resistors. Gain $G = -\frac{R_{E2}}{R_{E1}}$
	24	RR1	Reception gain control signal output. Reception gain of ATTAMP3 (−10dB to +10dB) is controlled by external resistors. Gain $G = -\frac{R_{R2}}{R_{R1}}$
	22	RR3	Reception gain control signal output. Reception gain of ATTAMP3 (−10dB to +10dB) is controlled by external resistors. Gain $G = -\frac{R_{R2}}{R_{R1}}$
	41	C1	Output for DC level cutting. Please cut DC level by a capacitor connected between C1 and C2 pins.
	12	TVDD2	Reference voltage output for transmit section.
	13	TREF	REF output voltage pin.
	15	RVDD2	Reference voltage output for reception section.
	14	RREF	REF output voltage pin.

FUNCTIONAL DESCRIPTIONS

ELECTRONIC VOLUME GAIN SETTING

Electronic volume gain and stand-by mode are set by 25-bit of serial data. The 25-bit of serial data format is shown below.



On each rising edge of CLK shifts one bit of serial data into internal shift register. On each rising edge of STB, the data stored in shift register is transferred into the buffer register. Read data is cleard by $\overline{\text{RESET}}$ signal.

Gain of volume VR1 to VR5 are set depending upon S1 to S5 data.

S5	S4	S3	S2	S1	VR1, VR4	VR2, VR3	VR5
1	1	1	1	1	1.4dB	3.0dB	10.5dB
1	1	1	1	0	1.2dB	2.8dB	9.8dB
1	1	1	0	1	1.0dB	2.6dB	9.1dB
1	1	1	0	0	0.8dB	2.4dB	8.4dB
1	1	0	1	1	0.6dB	2.2dB	7.7dB
1	1	0	1	0	0.4dB	2.0dB	7.0dB
1	1	0	0	1	0.2dB	1.8dB	6.3dB
1	1	0	0	0	0.0dB	1.6dB	5.6dB
1	0	1	1	1	-0.2dB	1.4dB	4.9dB
1	0	1	1	0	-0.4dB	1.2dB	4.2dB
1	0	1	0	1	-0.6dB	1.0dB	3.5dB
1	0	1	0	0	-0.8dB	0.8dB	2.8dB
1	0	0	1	1	-1.0dB	0.6dB	2.1dB
1	0	0	1	0	-1.2dB	0.4dB	1.4dB
1	0	0	0	1	-1.4dB	0.2dB	0.7dB
1	0	0	0	0	-1.6dB	0.0dB	0.0dB
0	1	1	1	1	–	-0.2dB	-0.7dB
0	1	1	1	0	–	-0.4dB	-1.4dB
0	1	1	0	1	–	-0.6dB	-2.1dB
0	1	1	0	0	–	-0.8dB	-2.8dB
0	1	0	1	1	–	-1.0dB	-3.5dB
0	1	0	1	0	–	-1.2dB	-4.2dB
0	1	0	0	1	–	-1.4dB	-4.9dB
0	1	0	0	0	–	-1.6dB	-5.6dB
0	0	1	1	1	–	-1.8dB	-6.3dB
0	0	1	1	0	–	-2.0dB	-7.0dB
0	0	1	0	1	–	-2.2dB	-7.7dB
0	0	1	0	0	–	-2.4dB	-8.4dB
0	0	0	1	1	–	-2.6dB	-9.1dB
0	0	0	1	0	–	-2.8dB	-9.8dB
0	0	0	0	1	–	-3.0dB	-10.5dB
0	0	0	0	0	–	-3.2dB	-11.2dB

STAND-BY MODE SETTING

Stand-by mode is set depending upon SB1 and SB2 data.

SB1		H	L	L	L
SB2		H	L	H	L
Transmit system block		0	x	x	x
Reception system block	Pre filter 3	0	x	0	0
	De emphasis	0	x	0	0
	Post filter 3	0	x	0	0
	Summing network	0	0	x	0
	RVDD/2	0	0	0	0
	Others reception block	0	x	x	x
SW, control block		0	0	0	0

Notes: 0 : Operating mode
x : Stand-by mode
When $\overline{\text{RESET}}$ signal is low, SB1 and SB2 are set high.

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OUTPUT PINS CONDITION AT STAND-BY MODE

Pin No.	SB1	H	H	L	L
	SB2	H	L	H	L
32	COMP1	ST	HZ	HZ	HZ
26	EXP1	ST	RVDD/2	RVDD/2	RVDD/2
18	MSK	ST	HZ	ST	ST
47	MOD	ST	HZ	HZ	HZ
20	AFOUT	ST	ST	RVDD/2	ST
37	RT1	ST	HZ	HZ	HZ
39	RT3	ST	TVDD/2 *1	TVDD/2 *1	TVDD/2 *1
29	RE1	ST	RVDD/2	RVDD/2	RVDD/2
27	RE3	ST	RVDD/2	RVDD/2	RVDD/2
24	RR1	ST	ST	RVDD/2	ST
22	RR3	ST	ST	RVDD/2	ST
41	C1	ST	TVDD/2	TVDD/2	TVDD/2
12	TVDD2	ST	HZ	HZ	HZ
13	TREF	ST	ST	ST	ST
15	RVDD2	ST	ST	ST	ST
14	RREF	ST	ST	ST	ST

Notes: HZ : High impedance.
ST : Standard output level.
*1 : *Pulled up by a high resistor.*

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Supply Voltage	V_{DD}	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	All input pins	0		V_{DD}	V
Analog Output Load Resistance 1	R_{L1}	RT1, RT3, RE1, RE3, RR1, RR3	30			kΩ
Analog Output Load Resistance 2	R_{L2}	COMP1, MOD, MSK, EXP1, AFOUT, TVDD2, RVDD2	10			kΩ
Analog Output Load Capacitance 1	C_{L1}	TREF, RREF		1.0		μF
Analog Output Load Capacitance 2	C_{L2}	TVDD2, RVDD2			100	pF
Operating Temperature	T_A		-30		60	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V±10%, T_A = -30 to 60°C, 0dBV = 1.0Vrms)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Supply Current 1	I_{DD}	V_{DD}	MOD, MSK, AFOUT are open. SB1 = H SB2 = H			14	mA
Supply Current 2	I_{DST1}	V_{DD}	MOD, MSK, AFOUT are open. SB1 = L SB2 = L			2.0	mA
Supply Current 3	I_{DST2}	V_{DD}	MOD, MSK, AFOUT are open. SB1 = H SB2 = L			1.5	mA
Digital Input Low Voltage	V_{IL}	DATA, CLK, STB, $\overline{\text{RESET}}$, AN, BYPASS, CLOCK, TAM, RAM		0		0.8	V
Digital Input High Voltage	V_{IH}	DATA, CLK, STB, $\overline{\text{RESET}}$, AN, BYPASS, CLOCK, TAM, RAM		2.2		V_{DD}	V
Digital Input Low Current	I_{IL}	DATA, CLK, STB, $\overline{\text{RESET}}$, AN, BYPASS, CLOCK, TAM, RAM	V_{IN} = GND	-10		10	μA
Digital Input High Current	I_{IH}	DATA, CLK, STB, $\overline{\text{RESET}}$, AN, BYPASS, CLOCK, TAM, RAM	V_{IN} = V_{DD}	-10		10	μA

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Analog Input Voltage	V_{IA}	COMP2, RT2, C2, DEM, RE2, EXP2, RR2, TONE		$1/5V_{DD}$		$4/5V_{DD}$	V
Analog Common-mode Input Voltage	V_{IAC}	AFIN (+) AFIN (–)		$1/5V_{DD}$		$4/5V_{DD}$	V
Analog Differential Input Voltage	V_{IAD}	AFIN (+) AFIN (–)	V_{IAD} = AFIN (+) –AFIN (–)	$-2/5V_{DD}$		$2/5V_{DD}$	V
Analog Input Resistance 1	R_{AIN1}	COMP2, RT2, C2, DEM, RE2, EXP2, RR2, TONE	Between input pins and $1/2 \cdot V_{DD}$ pin.	100			kΩ
Analog Input Resistance 2	R_{AIN2}	AFIN (+) AFIN (–)	$\left\lvert \frac{V_{IAFIN}(+) - V_{IAFIN}(-)}{I_{IAFIN}(+) - I_{IAFIN}(-)} \right\rvert$	30			kΩ
Analog Output Load Resistance 1	R_{LA1}	COMP1, MOD, MSK, EXP1, AFOUT	Between output pins and $1/2 \cdot V_{DD}$.	10			kΩ
Analog Output Load Resistance 2	R_{LA2}	RT1, RT2, RE1, RE3, RR1, RR3		30			kΩ
Analog Output Load Capacitance 1	C_{LA1}	TVDD2 RVDD2	Between output pins and AG pin.			100	pF
Analog Output Load Capacitance 2	C_{LA2}	TREF RREF	Between output pins and AG pin.		1.0		μF
Analog Output Voltage	V_{OA}	COMP1, C1, MOD, MSK, EXP1, AFOUT, RT1, RT3, RE1, RE3, RR1, RR3		1.5		3.5	V
Transmit Gain	T_{GAIN}	AFIN-MOD	Input: –27dBV 1kHz VR1~3: 0dB R_{T1}=R_{T2}=100kΩ COMP1 and COMP2 are shorted.	7.0	9.0	11.0	dB
Transmit Mute Attenuation	T_{MUTE}	AFIN-MOD	Input: –27dBV 1kHz VR1~VR3: 0dB R_{T1}=R_{T2}=100kΩ COMP1 and COMP2 are shorted.	45			dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Transmit S/N Ratio	$T_{S/N}$	AFIN-MOD	Input: -27dBV 1kHz VR1~VR3: 0dB $R_{T1}=R_{T2}=100k\Omega$ COMP1 and COMP2 are shorted. BW=50Hz~20kHz	40			dB
Transmit Distortion	$T_{S/D}$	AFIN-MOD	Input: -27dBV 1kHz VR1~VR3: 0dB $R_{T1}=R_{T2}=100k\Omega$ COMP1 and COMP2 are shorted. BW=50Hz~20kHz			-40	dB
Reception Gain	R_{GAIN}	DEM-AFOUT	Input: -26dBV 1kHz VR4, 5: 0dB $R_{R1}=R_{R2}=100k\Omega$ $R_{E1}=R_{E2}=100k\Omega$ EXP1 and EXP2 are shorted. TONE=1/2·V_{DD}	-1.0	0	1.0	dB
Reception Adder Gain	R_{GSUM}	TONE-AFOUT	Input: -26dBV 1kHz R_{R2}: 1/2·V_{DD}	-1.0	0	1.0	dB
Reception MSK Gain	R_{GMSK}	DEM-MSK	Input: -26dBV 1kHz	-1.0	0	1.0	dB
Reception Mute Attenuation	R_{MUTE}	DEM-AFOUT	Input: -18dBV 1kHz VR4, 5: 0dB $R_{R1}=R_{R2}=100k\Omega$ $R_{E1}=R_{E2}=100k\Omega$ EXP1 and EXP2 are shorted. TONE=1/2·V_{DD}	45			dB
Reception S/N Ratio	$R_{S/N}$	DEM-AFOUT	Input: -18dBV 1kHz VR4, 5: 0dB $R_{R1}=R_{R2}=100k\Omega$ $R_{E1}=R_{E2}=100k\Omega$ EXP1 and EXP2 are shorted. TONE=1/2·V_{DD} BW=50Hz~20kHz	45			dB

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Reception Distortion	$R_{S/D}$	DEM-AFOUT	Input: -18dBV 1kHz VR4, 5: 0dB $R_{R1}=R_{R2}=100k\Omega$ $R_{E1}=R_{E2}\approx100k\Omega$ EXP1 and EXP2 are shorted. TONE=1/2·V_{DD} BW=50Hz~20kHz			-40	dB
Deviation Limit High Voltage	V_{DLH}	C2-MOD	VR3 = 0dB V_{C2} = 4/5·V_{DD} TAM = L	1/2V_{DD} +0.050V_{DD}	1/2V_{DD} +0.053V_{DD}	1/2V_{DD} +0.056V_{DD}	V
Deviation Limit Low Voltage	V_{DLL}	C2-MOD	VR3 = 0dB V_{C2} = 1/5·V_{DD} TAM = L	1/2V_{DD} -0.056V_{DD}	1/2V_{DD} -0.053V_{DD}	1/2V_{DD} -0.050V_{DD}	V
Electronic Volume Minimum Step Voltage 1	V_{STEP1}	COMP2-RT1 RT3-C1 C2-MOD RE3-EXP1	Min. step of volume VR1~VR4	0.1	0.2	0.3	dB
Electronic Volume Minimum Step Voltage 2	V_{STEP2}	EXP2-RR1	Min. step of VR5	0.4	0.7	1.0	dB
Electronic Volume Maximum Variable Width 1	V_{VR1}	COMP2-RT1 RE3-EXP1	Max. variable width of VR1, VR4	2.6	3.0	3.4	dB
Electronic Volume Maximum Variable Width 2	V_{VR2}	RT3-C1 C2-MOD	Max. variable width of VR2, VR3	5.4	6.2	7.0	dB
Electronic Volume Maximum Variable Width 3	V_{VR3}	EXP2-RR1	Max. variable width of VR5	20.9	21.7	22.5	dB
Clock Duty	D_{CLK}	CLOCK		38	50	62	%

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AC CHARACTERISTICS

(V_{DD} = 5.0V±10%, T_A = −30 to 60°C)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Clock High-level Width	t_{WHCK}	CLK		1.0			μs
Clock Low-level Width	t_{WLCK}	CLK		1.0			μs
Data Setup Time	t_{SD}	DATA, CLK		1.0			μs
Data Hold Time	t_{HD}	DATA, CLK		1.0			μs
Strobe Signal High-level Width	t_{WHSB}	STB		1.0			μs
Strobe-Signal Low-level Width	t_{WLSB}	STB		1.0			μs
Strobe Signal Setup Time	t_{SS}	STB, CLK		1.0			μs
Strobe Signal Hold Time	t_{HS}	STB, CLK		1.0			μs
Rise Time	t_r	CLK, DATA, STB		0		100	ns
Fall Time	t_f	CLK, DATA, STB		0		100	ns

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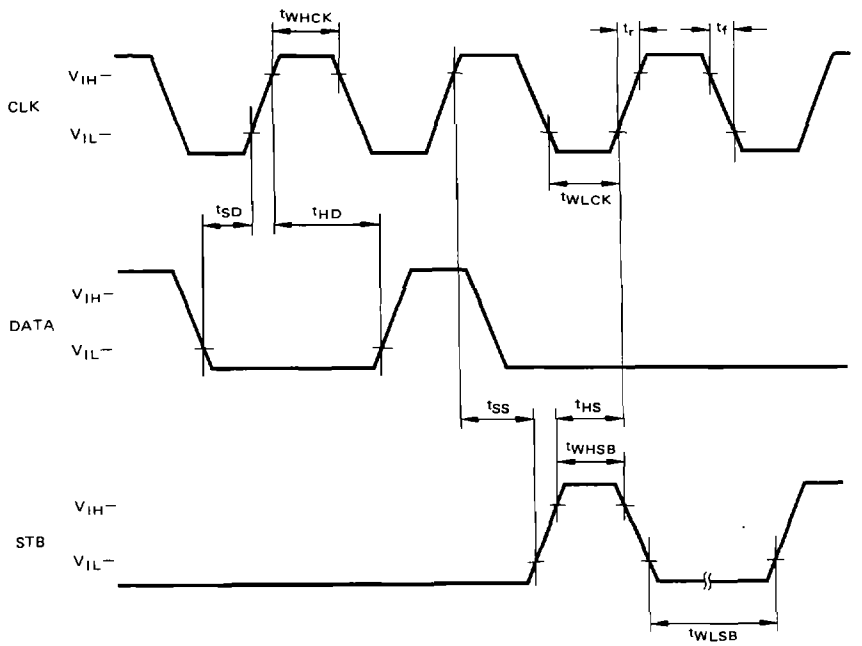
TRANSMISSION CHARACTERISTICS

(V_{DD} = 5.0V±10%, T_A = −30 to 60°C, 0dBV = 1.0Vrms)

Parameter	Symbol	Pin Name	Condition	Note
Transmission Characteristics	TFA	AFIN-MOD	VR1~3: 0dB COMP1 and COMP2 are shorted. AN =H, R_{T1} = R_{T2} = 100kΩ Input Level: −27dBV	Please see Fig.-2
	TFN	AFIN-MOD	VR1~3: 0dB COMP1 and COMP2 are shorted. AN = L, R_{T1} = R_{T2} = 100kΩ Input Level: −27dBV	Please see Fig.-3
Reception Characteristics	RFA	DEM-AFOUT	VR4, 5: 0dB EXP1 and EXP2 are shorted. AN = H, R_{E1} = R_{E2} = 100kΩ R_{R1} = R_{R2} = 100kΩ TONE: 1/2·V_{DD} Input Level: −26dBV	Please see Fig.-4
	RFN	DEM-AFOUT	VR4, 5: 0dB EXP1 and EXP2 are shorted. AN = L, R_{E1} = R_{E2} = 100kΩ R_{R1} = R_{R2} = 100kΩ TONE: 1/2·V_{DD} Input Level: −26dBV	Please see Fig.-5

TIMING CHART



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TRANSMISSION CHARACTERISTICS CURVES

Fig. 2 – TRANSMISSION AMPS STANDARD (AN=H)

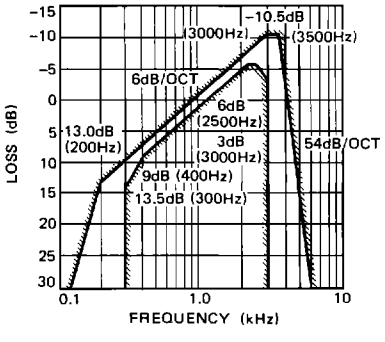


Fig. 3 – TRANSMISSION NMT STANDARD (AN=L)

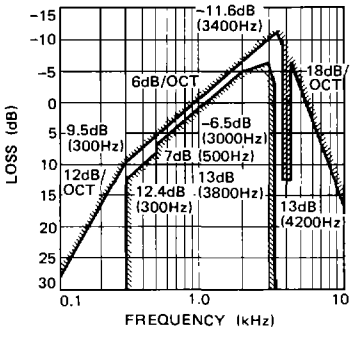


Fig. 4 – RECEPTION AMPS STANDARD (AN=H)

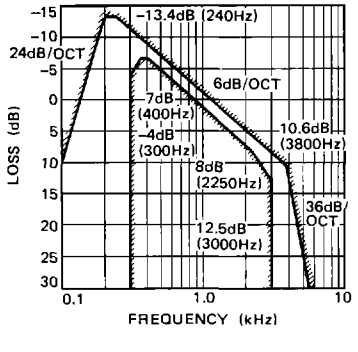
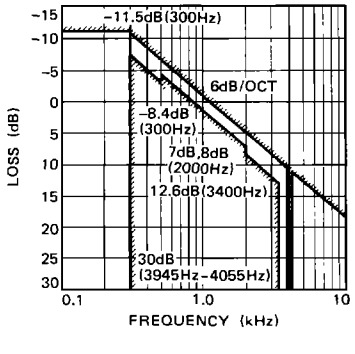


Fig. 5 – RECEPTION NMT STANDARD (AN=L)



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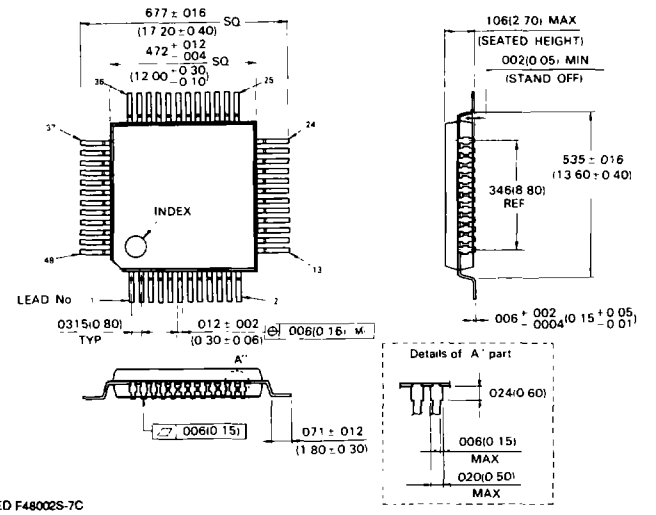
PACKAGE DIMENSIONS

48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M02)



Dimensions in inches (millimeters)

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