LOW-POWER OCTAL ECL/TTL BI-DIRECTIONAL TRANSLATOR WITH REGISTER

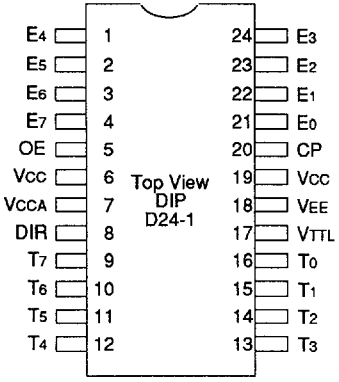
SYNERGY SEMICONDUCTOR

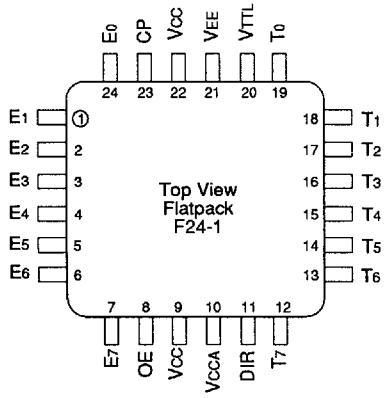
PRELIMINARY
SY100S329

FEATURES

- **Bi-directional translation**
- **ESD protection of 2000V**
- **ECL high impedance outputs**
- **Registered outputs**
- **Voltage compensated operating range: –4.2V to –5.7V**
- **Fast TTL outputs**
- **Three-state outputs**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP and CERPACK**

PIN CONFIGURATIONS





DESCRIPTION

The SY100S329 is an octal registered bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

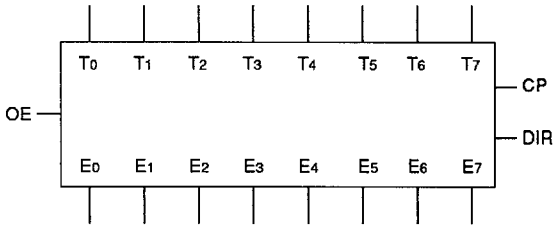
The SY100S329 is designed with fast TTL output buffers featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have internal 75KΩ pull-down resistors.

PIN NAMES(1)

Pin	Function
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input (Active Rising Edge)
DIR	Direction Control Input

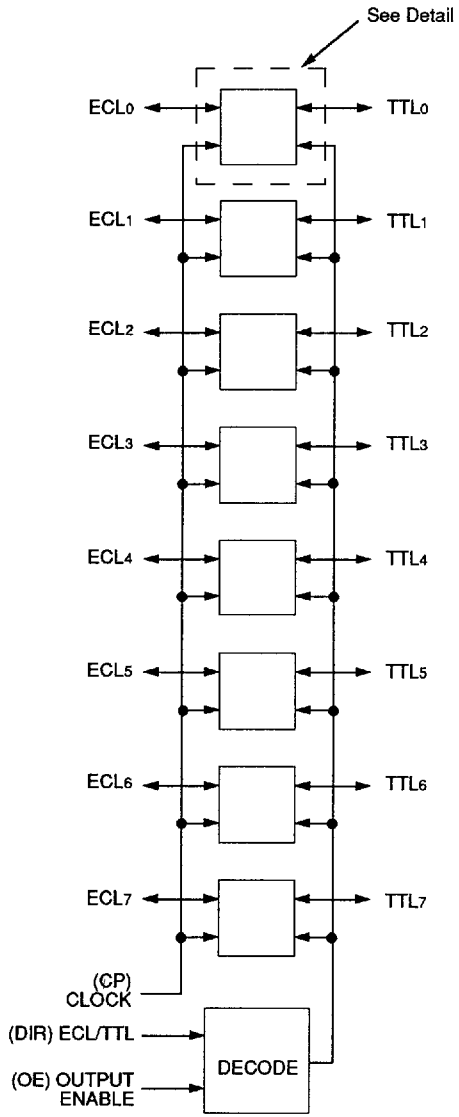
NOTE:
1. All pins function at 100K ECL levels except for T_0–T_7

LOGIC SYMBOL

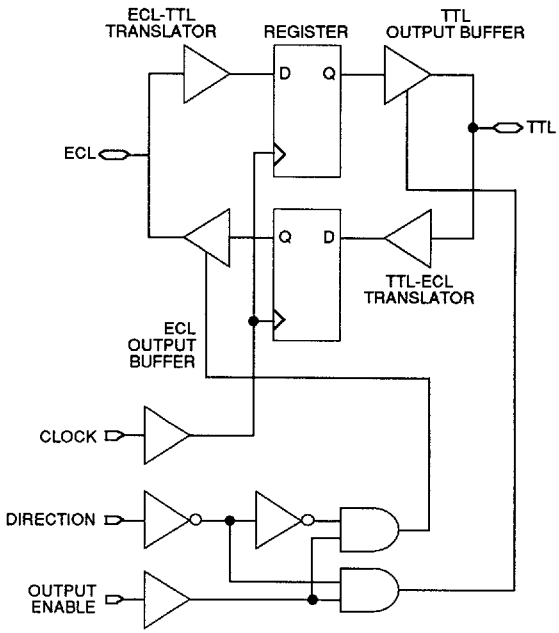


Rev.: B Amendment: /0
Issue Date: February, 1994

FUNCTIONAL BLOCK DIAGRAM



DETAIL



NOTE:

1. CP, DIR and OE use ECL logic levels.

TRUTH TABLE[1]

OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	2, 4
L	H	X	LOW (Cut-Off)	Input	3, 4
H	L	∫	L	L	2
H	L	∫	H	H	2
H	L	L	X	NC	2, 4
H	H	∫	L	L	3
H	H	∫	H	H	3
H	H	L	NC	X	3, 4

NOTES:

1 H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = High Impedance
2 ECL input to TTL output mode.
3. TTL input to ECL output mode.
4. Retains data present before CP.

GUARANTEED OPERATING CONDITIONS

Symbol	Rating	Value	Unit
V_{EE}	ECL Supply Voltage	–5.7 to –4.2	V
V_{TTL}	TTL Supply Voltage	+4.5 to +5.5	V
T_C	Case Temperature	0 to +85	°C

6

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_J	Maximum Junction Temperature Ceramic Plastic	 +175 +150	°C
V_{EE}	V_{EE} Pin Potential to Ground Pin	–7.0 to +0.5	V
V_{TTL}	V_{TTL} Pin Potential to Ground Pin	–0.5 to +6.0	V
—	ECL Input Voltage (DC)	V_{EE} to +0.5	V
—	ECL Output Current (DC Output HIGH)	–50	mA
—	TTL Input Voltage[2]	–0.5 to +6.0	V
—	TTL Input Current[2]	–30 to +5.0	mA
—	Voltage Applied to Output in HIGH State (Three-state Output)	–0.5 to +5.5	V
—	Current Applied to TTL Output in LOW State (Max.)	Twice the Rated I_{OL}	mA

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

TTL-TO-ECL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1025	–955	–870	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)
V_{OL}	Output LOW Voltage	–1830	–1705	–1620	mV	Loading with 50Ω to –2V
	Cutoff Voltage	—	–2000	–1950	mV	OE or DIR Low, V_{IN} = V_{IH} (Max.) or V_{IL} (Min.), Loading with 50Ω to –2V
V_{OHC}	Output HIGH Voltage Corner Point High	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.) Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage Corner Point Low	—	—	–1610	mV	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	—	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current	—	—	70	µA	V_{IN} = +2.7V
	Breakdown Test	—	—	1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	–700	—	—	µA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{EE}	V_{EE} Supply Current	–189 –199	— —	–94 –94	mA	LE Low, OE and DIR High, Inputs Open V_{EE} = –4.2V to –4.8V V_{EE} = –4.2V to –5.7V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions

ECL-TO-TTL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50pF, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9	— —	V	I_{OH} = –3mA, V_{TTL} = 4.75V I_{OH} = –3mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage	—	0.3	0.5	V	I_{OL} = 24mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	–1165	—	–870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	–1830	—	–1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.)
I_{IL}	Input LOW Current	0.50	—	—	µA	V_{IN} = V_{IL} (Min.)
I_{OZHT}	Three-State Current Output High	—	—	70	µA	V_{OUT} = +2.7V
I_{OZLT}	Three-State Current Output Low	–700	—	—	µA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	–150	—	–60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current	—	—	74	mA	V_{TTL} = +5.5V

NOTE:

1. The specified limits represent the "worst case" value for the parameter Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	350	—	350	—	350	—	MHz	—
t_{PLH} t_{PHL}	CP to En	1.7	3.6	1.7	3.7	1.9	3.9	ns	Figures 1 & 2
t_{PZH}	OE to En (Cutoff to HIGH)	1.3	4.2	1.5	4.4	1.7	4.8	ns	Figures 1 & 2
t_{PHZ}	OE to En (HIGH to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	Figures 1 & 2
t_{PHZ}	DIR to En (HIGH to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	Figures 1 & 2
t_{set}	Tn to CP	1.1	—	1.1	—	1.1	—	ns	Figures 1 & 2
t_{hold}	Tn to CP	1.7	—	1.7	—	1.9	—	ns	Figures 1 & 2
t_{pw}(H)	Pulse Width CP	2.1	—	2.1	—	2.1	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, C_L = 50pF[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	125	—	125	—	125	—	MHz	—
t_{PLH} t_{PHL}	CP to Tn	3.1	7.2	3.1	7.2	3.3	7.7	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	Figures 3 & 6
t_{set}	En to CP	1.1	—	1.1	—	1.1	—	ns	Figures 3 & 4
t_{hold}	En to CP	2.1	—	2.1	—	2.6	—	ns	Figures 3 & 4
t_{PW} (H)	Pulse Width CP	4.1	—	4.1	—	4.1	—	ns	Figures 3 & 4

NOTE:

1. The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

6

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	350	—	350	—	350	—	MHz	—
t_{PLH} t_{PHL}	CP to En	1.7	3.4	1.7	3.5	1.9	3.7	ns	Figures 1 & 2
t_{PZH}	OE to En (Cutoff to HIGH)	1.3	4.0	1.5	4.2	1.7	4.6	ns	Figures 1 & 2
t_{PHZ}	OE to En (HIGH to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	Figures 1 & 2
t_{PHZ}	DIR to En (HIGH to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	Figures 1 & 2
t_{set}	Tn to CP	1.0	—	1.0	—	1.0	—	ns	Figures 1 & 2
t_{hold}	Tn to CP	1.7	—	1.7	—	1.7	—	ns	Figures 1 & 2
t_{pw} (H)	Pulse Width CP	2.0	—	2.0	—	2.0	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	—
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	—
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	650	—	650	—	650	ps	—
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	650	—	650	—	650	ps	—

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

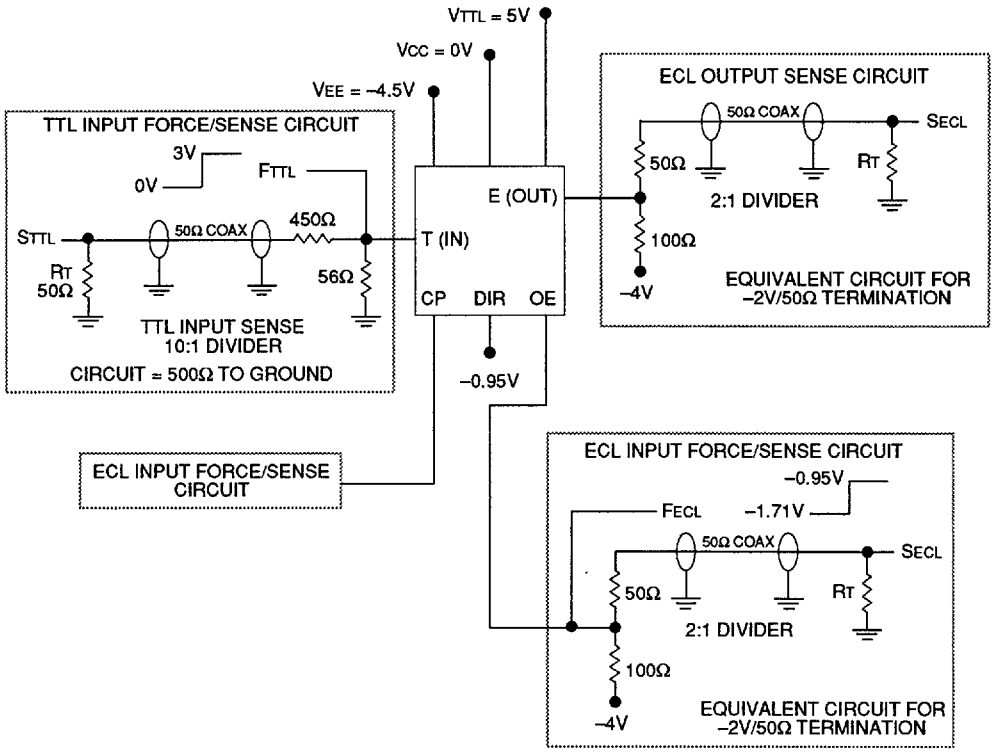
FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50pF

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	125	—	125	—	125	—	MHz	—
t_{PLH} t_{PHL}	CP to Tn	3.1	7.0	3.1	7.0	3.3	7.5	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	Figures 3 & 6
t_{set}	En to CP	1.0	—	1.0	—	1.0	—	ns	Figures 3 & 4
t_{hold}	En to CP	2.0	—	2.0	—	2.5	—	ns	Figures 3 & 4
t_{pw} (H)	Pulse Width CP	4.0	—	4.0	—	4.0	—	ns	Figures 3 & 4
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	600	—	600	—	600	ps	—
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	850	—	850	—	850	ps	—
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	1350	—	1350	—	1350	ps	—
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	950	—	950	—	950	ps	—

6

TEST CIRCUITRY (TTL-TO-ECL)



NOTES:

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. For ECL input pins, the equivalent force/sense circuitry is optional.

Figure 1. TTL-to-ECL AC Test Circuit

SWITCHING WAVEFORMS (TTL-TO-ECL)

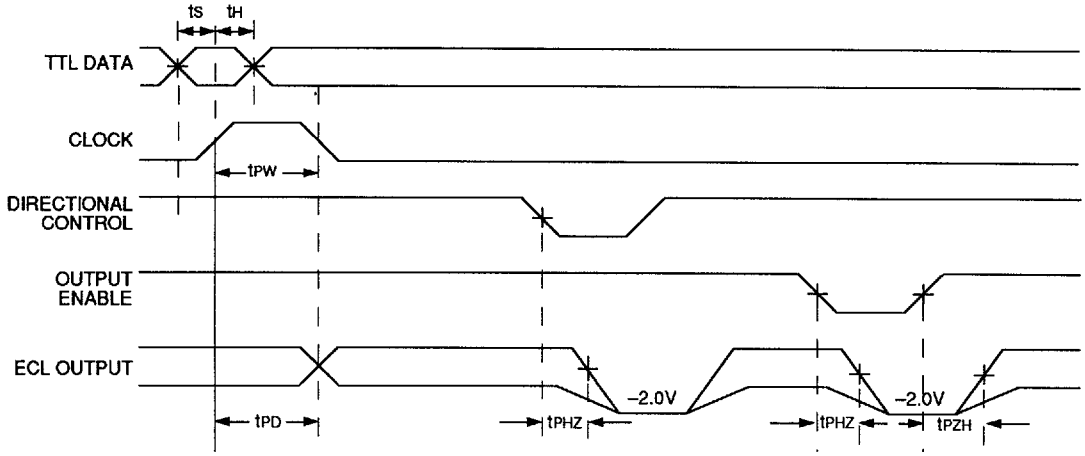
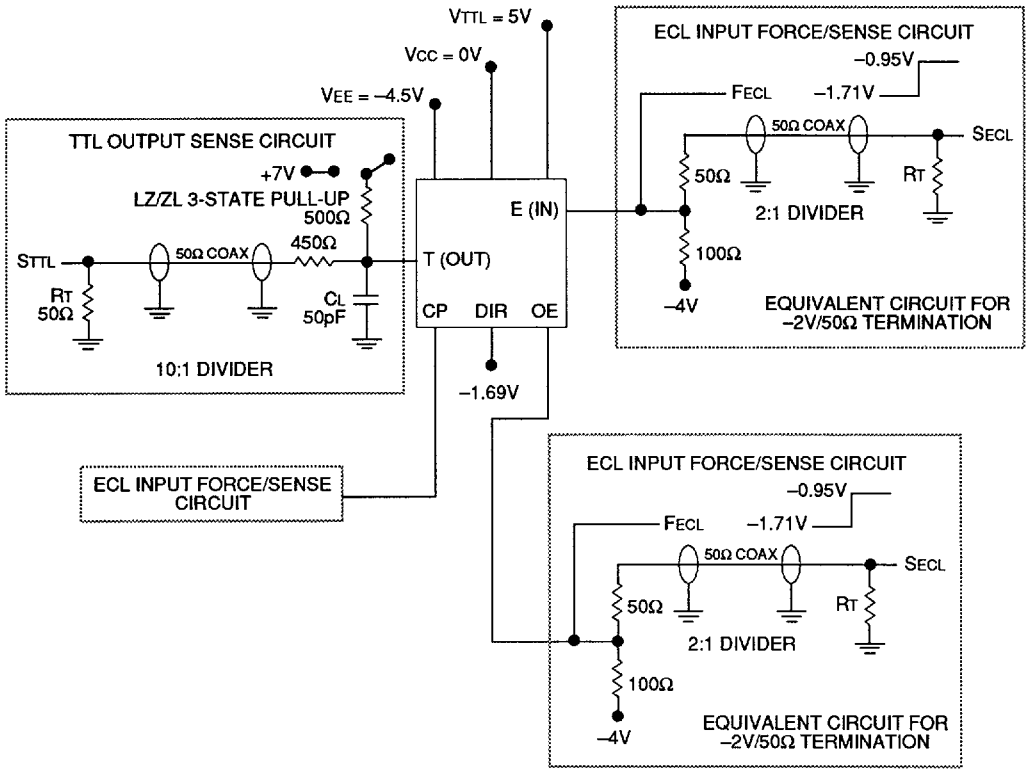


Figure 2. TTL-to-ECL Propagation Delay and Transition Times

6

TEST CIRCUITRY (ECL-TO-TTL)

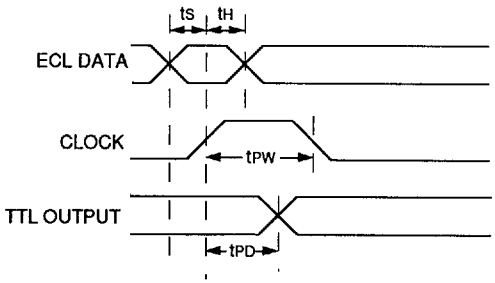


NOTES;

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is *not* being monitored, an external 50Ω resistance must be applied to serve as R_t.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. The TTL three-state pull-up switch is connected to +7V only for ZL and LZ tests.

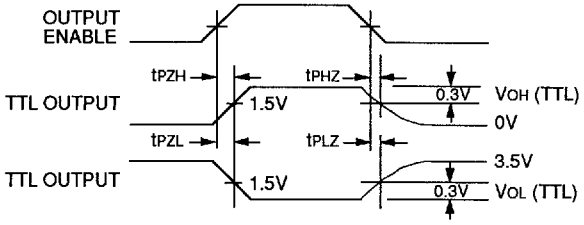
Figure 3. ECL-to-TTL AC Test Circuit

SWITCHING WAVEFORMS (ECL-TO-TTL)



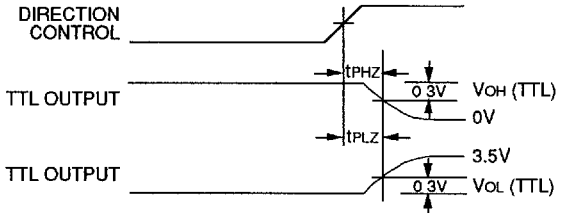
NOTE:
1. DIR is LOW and OE is HIGH

Figure 4. ECL-to-TTL Transition, Propagation Delay and Transition Times



NOTE:
1 DIR is LOW and LE is HIGH.

Figure 5. ECL-to-TTL Transition, OE to TTL Output Enable and Disable Times



NOTE:
1. OE is HIGH and LE is HIGH.

Figure 6. ECL-to-TTL Transition, DIR to TTL Output Disable Time

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S329DC	D24-1	Commercial
SY100S329FC	F24-1	Commercial

6