54F/74F85

4-Bit Magnitude Comparator

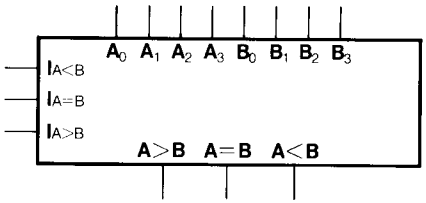
Description

The 'F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0-A_3) and (B_0-B_3), where A_3 and B_3 are the most significant bits.

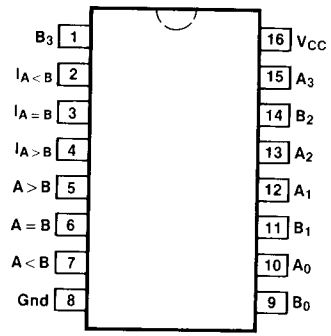
- **Magnitude Comparison of Any Binary Words**
- **Serial or Parallel Expansion Without Extra Gating**

Ordering Code: See Section 5

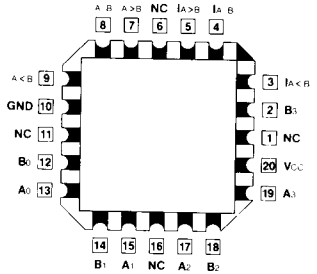
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	A Inputs	0.5/0.375
B_0-B_3	B Inputs	0.5/0.375
$I_{A<B}$	Expansion Input, Less Than	0.5/0.375
$I_{A=B}$	Expansion Input, Equal To	0.5/0.375
$I_{A>B}$	Expansion Input, Greater Than	0.5/0.375
A>B	Greater Than Output	25/12.5
A=B	Equal To Output	25/12.5
A<B	Less Than Output	25/12.5

Functional Description

The operation of the 'F85 is described in the Function Table, which shows all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = LOW, $I_{A=B}$ = HIGH, and $I_{A<B}$ = LOW.

The parallel expansion scheme shown in Figure a demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position, except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A<B}$ as an 'A' input, $I_{A<B}$ as a 'B' input and setting $I_{A=B}$ LOW. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1

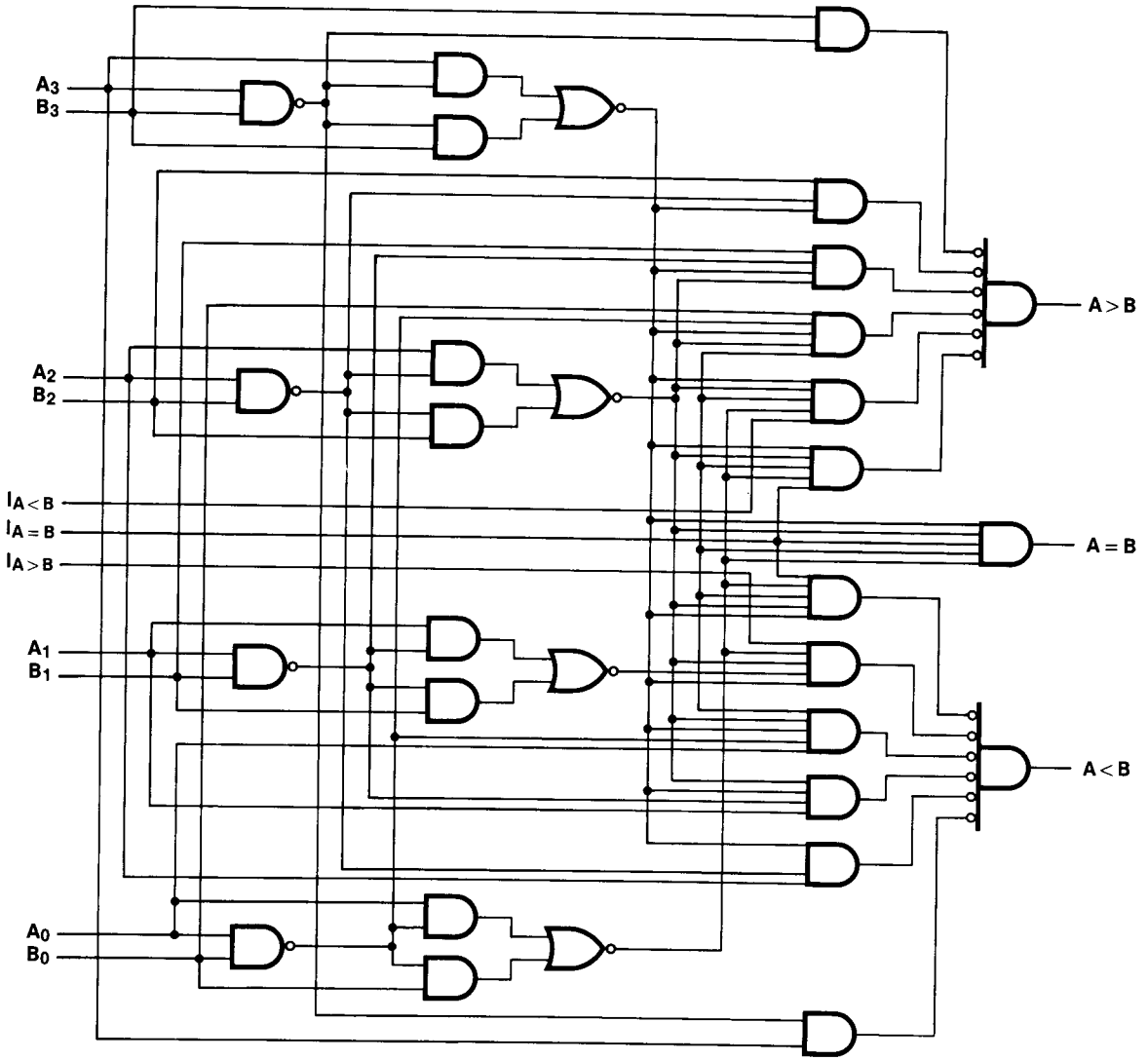
Word Length	Number of Packages	Typical Speeds 54F/74F
1-4 Bits	1	12 ns
5-25 Bits	2-6	22 ns
25-120 Bits	8-31	34 ns

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		32	47	mA	Outputs = OPEN, Inputs = Gnd, V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A or B to A<B or A>B		14.0 14.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay A or B to A=B		14.0 11.5						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $I_{A<B}$ or $I_{A=B}$ to A>B		8.0 7.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $I_{A=B}$ to A=B		7.0 7.0						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $I_{A>B}$ or $I_{A=B}$ to A<B		8.0 7.0						ns	3-1 3-3

Comparison of Two 24-Bit Words