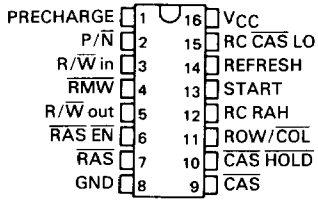
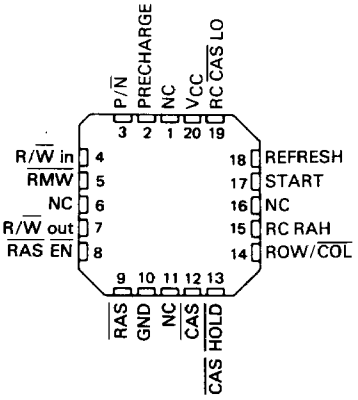
D2548, JANUARY 1981 – REVISED DECEMBER 1981

- **Provides Correct Timing for Memory Cycles**
  - **Read Cycle**
  - **Write Cycle**
  - **Read-Modify-Write Cycle**
  - **RAS-Only Refresh Cycle**
- **Page or Normal Modes**
- **Stand-Alone Controller for CPU-to-Memory Interface**
- **Also Designed to be Part of a Three-Chip Set Consisting of 'LS600 thru 'LS603, 'LS604 thru 'LS607, and 'LS608**
- **$\overline{RAS}$ Output is 3-State to Share Bus With 'LS600 thru 'LS603**
- **Critical Times Are User RC-Programmable to Optimize System Performance**

SN54LS608 . . . J PACKAGE
SN74LS608 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS608 . . . FK PACKAGE
SN74LS608 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flip-flops, and more than 50 miscellaneous gates on a single chip. The 'LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

The 'LS608 can operate as a stand-alone interface but it is also designed to be part of a three-chip memory controller set. The user must select one of the 'LS600 thru 'LS603 refresh controllers and one of the 'LS604 thru 'LS607 multiplexers to use along with the 'LS608 memory cycle controller for complete dynamic RAM control.

After the user has selected and attached RC networks to pins 1, 12, and 15, the 'LS608 will deliver proper $\overline{RAS}$, $\overline{CAS}$, and READ/$\overline{WRITE}$ output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady-state input conditions of the 'LS608 as indicated in the table below.

MEMORY CYCLE	MODE	INPUT CONDITIONS						
		P/$\overline{N}$ IN	R/$\overline{W}$ IN	$\overline{RMW}$ IN	$\overline{RAS}$ ENABLE IN	$\overline{CAS}$ HOLD IN	START IN	REFRESH IN
READ	PAGE	H	H	H	L	H	↑	L
WRITE		H	L	H	L	H	↑	L
READ-MODIFY-WRITE		H	H	L	L	H	↑	L
READ	NORMAL	L	H	H	L	H	↑	L
WRITE		L	L	H	L	H	↑	L
READ-MODIFY-WRITE		L	H	L	L	H	↑	L
REFRESH	REFRESH	x	x	x	L	H	↑	H
EXTERNAL REFRESH		x	x	x	H	H	x	L

H = High, L= Low, x = irrelevant, ↑ = low-to-high transition

PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	RC PRECHARGE	User-programmable timing node* for precharge ($\overline{CAS}$ high and $\overline{RAS}$ high).
2	P/$\overline{N}$ IN	When high, initiates a ready cycle (holds R/W OUT high) and, when low, page mode read or write cycle holds $\overline{RAS}$ continuously low while $\overline{CAS}$ and column addresses are sequenced.
3	R/$\overline{W}$ IN	When high, initiates a ready cycle (holds R/$\overline{W}$ OUT high) and, when low, initiates a write cycle (holds R/$\overline{W}$ OUT low) if pin 4 is high and pin 14 is low.
4	$\overline{RMW}$ IN	When low, enables read-modify-write cycle. R/$\overline{W}$ IN must be high at the start of the RMW cycle.
5	R/$\overline{W}$ OUT	When high, indicates a read cycle is in progress. When low, indicates a write cycle is in progress. Normally ties to a $\overline{W}$ memory input in a system.
6	$\overline{RAS}$ $\overline{ENABLE}$ IN	When low, enables $\overline{RAS}$ output. When high, $\overline{RAS}$ is in the high-impedance or third state.
7	$\overline{RAS}$ OUT	3-state row-address-strobe output controlled by $\overline{RAS}$ $\overline{ENABLE}$ IN. In the three-chip controller set, the $\overline{RAS}$ output of the 'LS608 ties to the $\overline{RAS}$ output of the refresh controller ('LS600 thru 'LS603).
8	GND	Device and substrate ground.
9	$\overline{CAS}$ OUT	Column-address-strobe output.
10	$\overline{CAS}$ $\overline{HOLD}$ IN	When low, allows $\overline{CAS}$ to latch in low state. When high, latch is removed. Can be used to improve data retrieval during read cycle.
11	ROW/$\overline{COL}$ (or $\overline{MEMBSY}$) OUT	In a system where the 'LS608 is a stand-alone controller, this output indicates a memory-busy condition to the microprocessor. When the 'LS608 is used as a part of a three-chip controller set, this pin ties to the SELECT A/$\overline{B}$ input of the multiplexer ('LS604 thru 'LS607) for selecting row and column in addition to indicating a memory-busy condition to the microprocessor.
12	RC RAH	User-programmable timing node* for row address hold time. (high level at ROW/$\overline{COL}$ OUT).
13	START IN	When changed from low to high, initiates a memory cycle.
14	REFRESH IN	When high, enables $\overline{RAS}$-only refresh cycle.
15	RC $\overline{CAS}$ LO	User-programmable timing node* for column-address-strobe low time.
16	V_{CC}	5-volt power supply terminal.

*All timing nodes require a resistor to V_{CC} and a capacitor to ground. Programmed time is approximately 0.29 RC.

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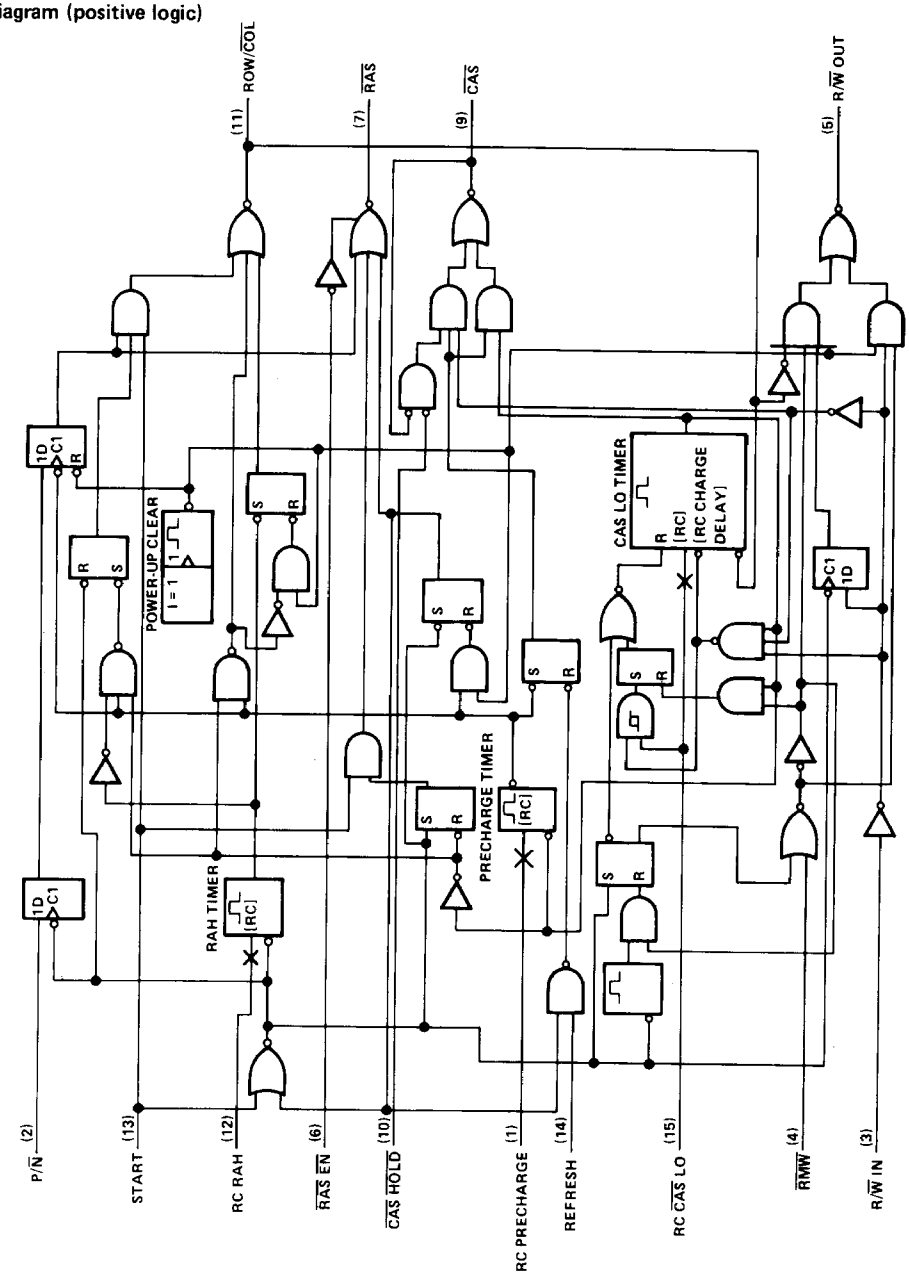
logic diagram (positive logic)

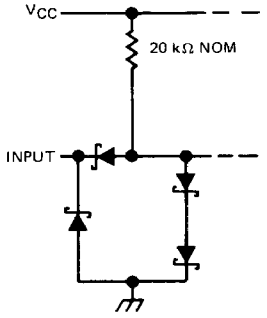


Pin numbers shown on logic notation are for D, J or N packages.

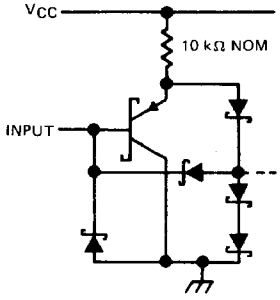
3 TTL DEVICES

schematics of inputs and outputs

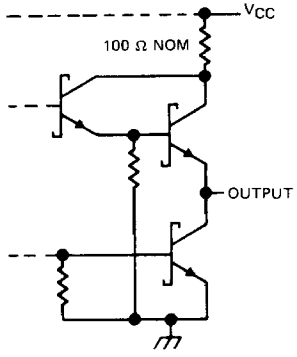
EQUIVALENT OF REFRESH, R/$\overline{W}$, AND $\overline{RMW}$ INPUTS



EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF ALL OUTPUTS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS608 . . . . . −55°C to 125°C
SN74LS608 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS608			SN74LS608			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	ROW/$\overline{\text{COL}}$			−0.4			−0.4	mA
		$\overline{\text{RAS}}$			−1			−2.6	
		All others			−1.2			−1.2	
I_{OL}	Low-level output current	ROW/$\overline{\text{COL}}$			4			8	mA
		All others			12			24	
t_{su}	Setup time	R/$\overline{\text{W}}$, $\overline{\text{RMW}}$, P/$\overline{\text{N}}$, or REFRESH to START↑	20			20			ns
		$\overline{\text{CAS}}$ HOLD to $\overline{\text{CAS}}$↓	20			20			
t_h	Hold time		0			0			ns
R_{ext}	External timing resistor	RC RAH	0.1		2	0.1		2	kΩ
		RC $\overline{\text{CAS}}$ LO, RC PRECHARGE	1		6	1		6	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS608			SN74LS608			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	ROW/$\overline{\text{COL}}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
	$\overline{\text{RAS}}$		I_{OH} = MAX	2.4	3.2		2.4	3.1		
	Others		I_{OH} = −1.2 mA	2.4	3.2		2.4	3.2		
V_{OL}	ROW/$\overline{\text{COL}}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
	Others		I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	$\overline{\text{RAS}}$	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V	V_{IL} = MAX,			20			20	μA
I_{OZL}	$\overline{\text{RAS}}$	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V	V_{IL} = MAX,			−20			−20	μA
I_I		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	REFRESH, R/$\overline{\text{W}}$, $\overline{\text{RMW}}$	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	Others					−0.2			−0.2	
I_O	ROW/$\overline{\text{COL}}$	V_{CC} = MAX	V_O = 2.25 V	−10		−50	−10		−50	mA
	Others		V_O = 0 V§	−30		−130	−30		−130	
I_{CC}		V_{CC} = MAX, Outputs open, All inputs at GND			38	65		38	65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND (see waveforms for more detail)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MODE	MIN	TYP	MAX	UNIT
t_{PHL}	START ↑	$\overline{RAS}$	R_L = 667 Ω to V_{CC}	NORMAL READ		8	15	ns
t_{PLH}†	START ↑	$\overline{RAS}$			290	363	435	ns
t_{PHL}‡	START ↑	$\overline{CAS}$			100	126	150	ns
t_{PLH}†	START ↑	$\overline{CAS}$			275	342	410	ns
t_{PHL}‡	START ↑	R/$\overline{W}$		NORMAL WRITE	90	113	135	ns
t_{PLH}†	START ↑	R/$\overline{W}$			303	383	460	ns
t_{PLH}	$\overline{CAS}$ HOLD ↑	$\overline{CAS}$		NORMAL READ		10	15	ns
t_{PHL}‡	START ↑	ROW/$\overline{COL}$	R_L = 2 kΩ to V_{CC}		75	100	125	ns
t_{PLH}§	START ↑	ROW/$\overline{COL}$			485	609	730	ns
t_{PHL}	R/$\overline{W}$ ↓	R/$\overline{W}$	R_L = 667 Ω to V_{CC}	NORMAL RMW		13	20	ns
t_{PLH}	ROW/$\overline{COL}$ ↑	R/$\overline{W}$				10	15	ns
t_{PLH}	$\overline{RMW}$ ↑	$\overline{CAS}$				34	50	ns
t_{PLH}♦	$\overline{RMW}$ ↑	ROW/$\overline{COL}$			240	300	360	ns
t_{PZH}	$\overline{RAS}$ $\overline{EN}$ ↓	$\overline{RAS}$	R_L = 667 Ω to GND	NORMAL READ		13	20	ns
t_{PZL}	$\overline{RAS}$ $\overline{EN}$ ↓	$\overline{RAS}$	R_L = 667 Ω to V_{CC}			14	25	ns
t_{PHZ}	$\overline{RAS}$ $\overline{EN}$ ↑	$\overline{RAS}$	R_L = 667 Ω to GND			7	15	ns
t_{PLZ}	$\overline{RAS}$ $\overline{EN}$ ↑	$\overline{RAS}$	R_L = 667 Ω to V_{CC}			16	25	ns

† Depends on RC network at pin 12 (2 kΩ, 180 pF used for testing) and the RC network at pin 15 (5 kΩ, 180 pF).
‡ Depends on RC network at pin 12 (2 kΩ, 180 pF).
§ Depends on RC networks at pin 12 (2 kΩ, 180 pF), pin 15 (5 kΩ, 180 pF), and pin 1 (5 kΩ, 180 pF).
♦ Depends on RC network at pin 1 (5 kΩ, 180 pF).
NOTE 2: Measurement point for all t_{PHZ} output pulses is 2.9 V. Measurement point for all t_{PLZ} output pulses is 0.8 V. All other measurement points are 1.3 V.

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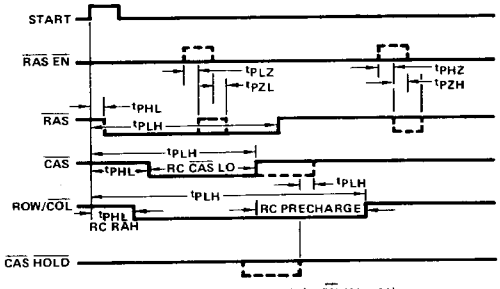
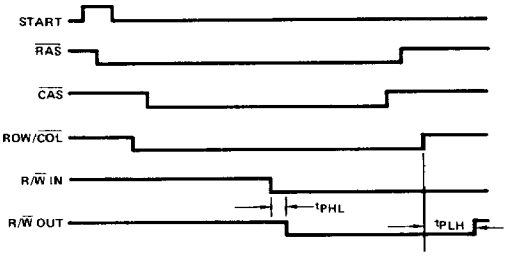
TTL DEVICES

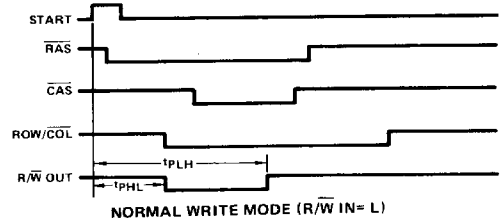
PARAMETER MEASUREMENT INFORMATION



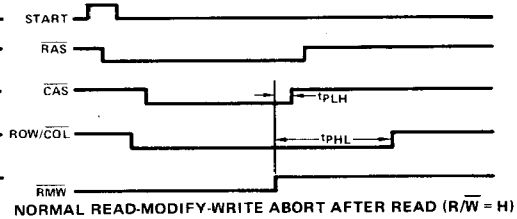
NORMAL READ MODE (R/$\overline{W}$ IN = H)



NORMAL READ-MODIFY-WRITE MODE ($\overline{RMW}$ = L)



NORMAL WRITE MODE (R/$\overline{W}$ IN= L)



NORMAL READ-MODIFY-WRITE ABORT AFTER READ (R/$\overline{W}$ = H)

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