SA572

Programmable analog compandor

Rev. 03 — 3 November 1998 Product data

1. Description

The SA572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The SA572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

2. Features

- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110 dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6 μV typical
- Wide supply voltage range—6 to 22 μV
- System level adjustable with external components

3. Applications

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

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4. Ordering information

Table 1: Ordering information

Type number	Package			
	Name	Description	Version	Temperature range (°C)
SA572D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1	–40 to +85
SA572N	DIP16	plastic dual in- line package; 16 leads (300 mil)	SOT38-4	–40 to +85

5. Block diagram

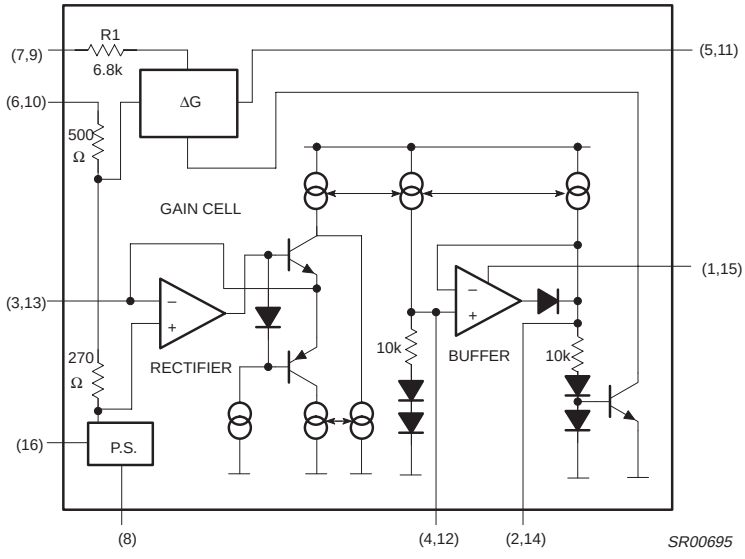

Fig 1. Block diagram.

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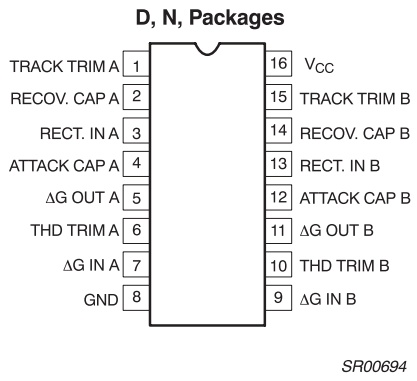
6. Pinning information

6.1 Pinning



(1) D package released in large SO (SOL) package only.

Fig 2. Pin configuration.

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
TRACK TRIM A	1	Track trim A
RECOV. CAP A	2	Recovery time capacitor A
RECT. IN A	3	Full-wave rectifier input A
ATTACK CAP A	4	Attack capacitor A
ΔG OUT A	5	Linearized temperature-compensated, gain cell OUT A
THD TRIM A	6	THD trim terminal A
ΔG IN A	7	Linearized temperature-compensated gain cell IN A
GND	8	Ground
ΔG IN B	9	Linearized temperature-compensated gain cell IN B
THD TRIM B	10	THD trim terminal B
ΔG OUT B	11	Linearized temperature-compensated gain cell OUT B
ATTACK CAP B	12	Attack capacitor B
RECT. IN B	13	Full-wave rectifier input B
RECOV. CAP B	14	Recovery time capacitor B
TRACK TRIM B	15	Track trim B
V_{CC}	16	Supply voltage

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7. Functional description

7.1 Audio signal processing IC combines VCA and fast attack/slow recovery level sensor

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Philips SA572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The SA572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10 kΩ resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10 kΩ resistor R_R. Typical attack time of 4 ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1 μF and 1.0 μF attack capacitors, respectively. Recovery time of 200 ms can be obtained with a 4.7 μF recovery capacitor for a 100 Hz signal, the third harmonic distortion is improved by more than 10 dB over the simple RC ripple filter with a single 1.0 μF attack and recovery capacitor, while the attack time remains the same.

The SA572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6 V to 22 V. Supply current is less than 6 mA. The SA572 is designed for applications from –40 °C to +85 °C.

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–	22	V_{DC}
T_{amb}	operating temperature range		–40	+85	°C
P_D	power dissipation		–	500	mW

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9. Static characteristics

Table 4: DC electrical characteristics

Standard test conditions (unless otherwise noted) V_{CC} = 15 V, T_{amb} = 25 °C; Expandor mode (see Section 10 "Test circuit"). Input signals at unity gain level (0 dB) = 100 mV_{RMS} at 1 kHz; $V_1 = V_2$; R_2 = 3.3 kΩ; R_3 = 17.3 kΩ.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		6	–	22	V_{DC}
I_{CC}	supply current	No signal	–	–	6.3	mA
V_R	internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	total harmonic distortion (untrimmed)	1 kHz C_A = 1.0 µF	–	0.2	1.0	%
THD	total harmonic distortion (trimmed)	1 kHz C_R = 10 µF	–	0.05	–	%
THD	total harmonic distortion (trimmed)	100 Hz	–	0.25	–	%
	no signal output noise	Input to V_1 and V_2 grounded (20–20 kHz)	–	6	25	µV
	DC level shift (untrimmed)	Input change from no signal to 100 mV_{RMS}	–	±20	±50	mV
	unity gain level		–1.5	0	+1.5	dB
	large-signal distortion	$V_1 = V_2$ = 400 mV	–	0.7	3	%
	tracking error (measured relative to value at unity gain) = [V_O–V_O (unity gain)]dB –V_2dB	Rectifier input				
		V_2 = +6 dB V_1 = 0 dB	–	±0.2	–	dB
		V_2 = –30 dB V_1 = 0 dB	–	±0.5	–2.5, +1.6	dB
	channel crosstalk	200 mV_{RMS} into channel A, measured output on channel B	60	–	–	dB
PSRR	power supply rejection ratio	120 Hz	–	70	–	dB

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10. Test circuit

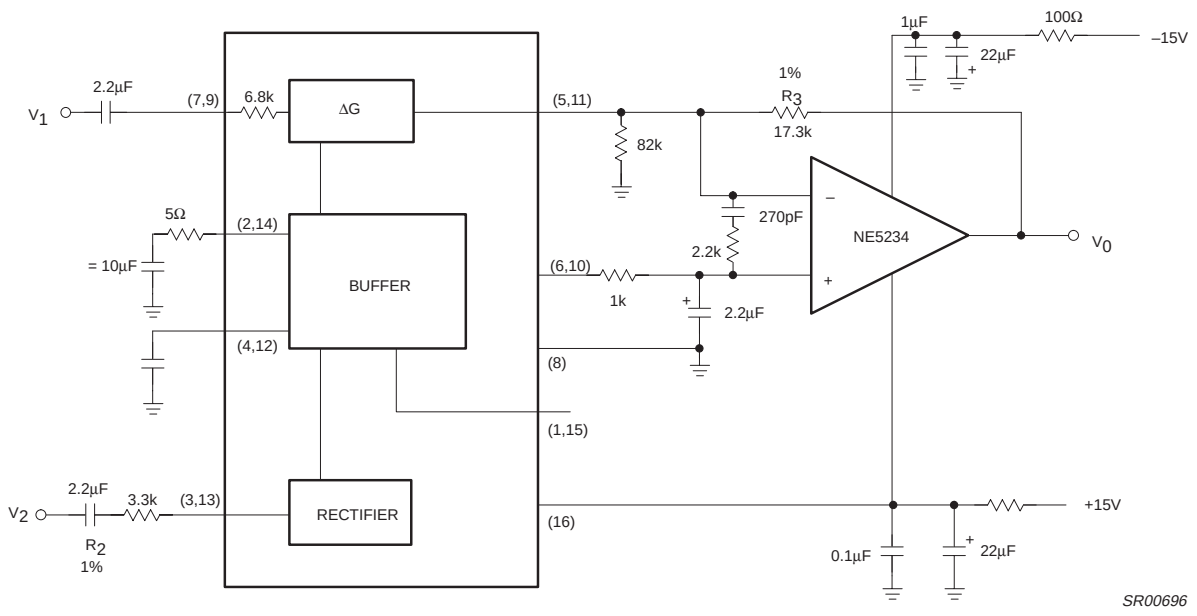

Fig 3. Test circuit.

11. Application information

11.1 SA572 Basic applications

11.1.1 Description

The SA572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5 V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

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11.1.2 Gain cell

Figure 4 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1-Q_2 and Q_3-Q_4 are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of Q_1-Q_2 and the V_{BE} of Q_3-Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta_{BE_{Q1Q2}} \tag{1}$$

$$(V_{BE} = V_T I_{IN} IC/IS)$$

$$V_T I_n \left(\frac{\frac{1}{2} I_G + \frac{1}{2} I_O}{I_S} \right) - V_T I_n \left(\frac{\frac{1}{2} I_G - \frac{1}{2} I_O}{I_S} \right) = \left(V_T I_n \left(\frac{I_1 + I_{IN}}{I_S} \right) - V_T I_n \left(\frac{I_2 - I_1 - I_{IN}}{I_S} \right) \right) \tag{2}$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

R_1 = 6.8 kΩ

I_1 = 140 μA

I_2 = 280 μA

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, Equation 2 can be simplified to:

$$I_O = \frac{2}{I_2} \times I_{IN} \times I_G - \frac{1}{I_2}(I_2 - 2I_1) \times I_G \tag{3}$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25 μA into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100 mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6 μV in the audio spectrum (10 Hz to 20 kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

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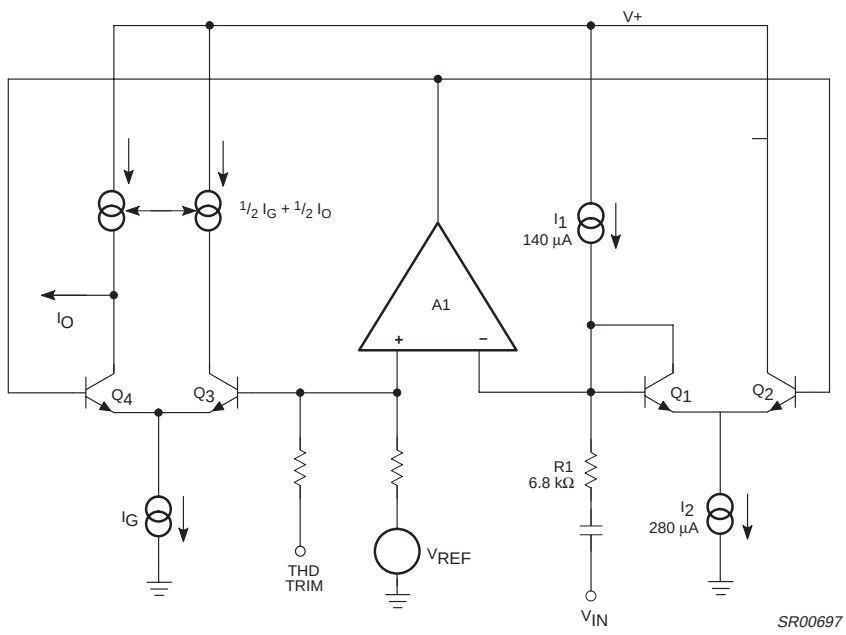

Fig 4. Basic gain cell schematic.

11.1.3 Rectifier

The rectifier is a full-wave design as shown in Figure 5. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70 nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to: $I_{RAC} = \frac{V_{IN}(AVG)}{R_2}$

The internal bias scheme limits the maximum output current I_R to be around 300 µA. Within a ±1 dB error band the input range of the rectifier is about 52 dB.

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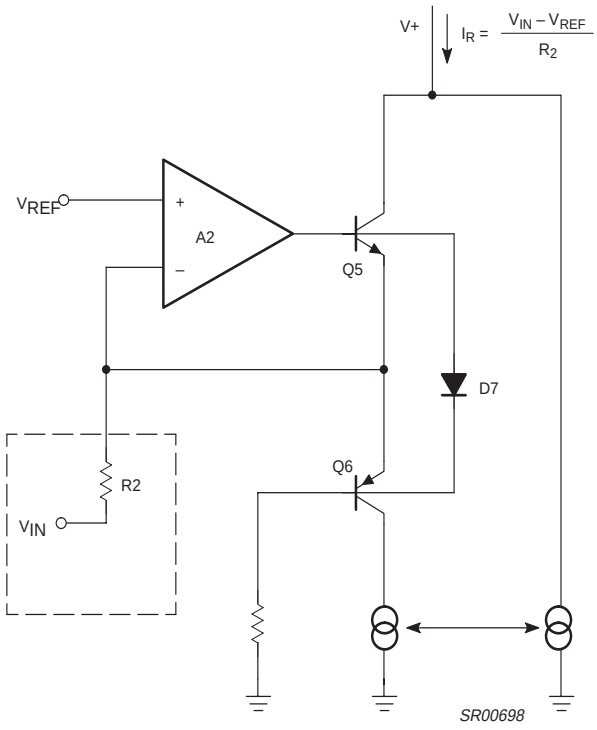

Fig 5. Simplified rectifier schematic.

11.1.4 Buffer amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 6, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\, e^{\frac{-t}{\tau_A}} + Ga_{FNL} \quad (5)$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \times CA = 10\ k\Omega \times CA$

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where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR $\times$ R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{RINT} - G_{RFNL})e^{\frac{-t}{\tau_R}} + G_{RFNL} \quad (6)$$

$$\tau R = R_R \times CR = 10k\Omega \times CR$$

where τR is the recovery time constant and R_R is a 10 kΩ internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ± 3 μA.

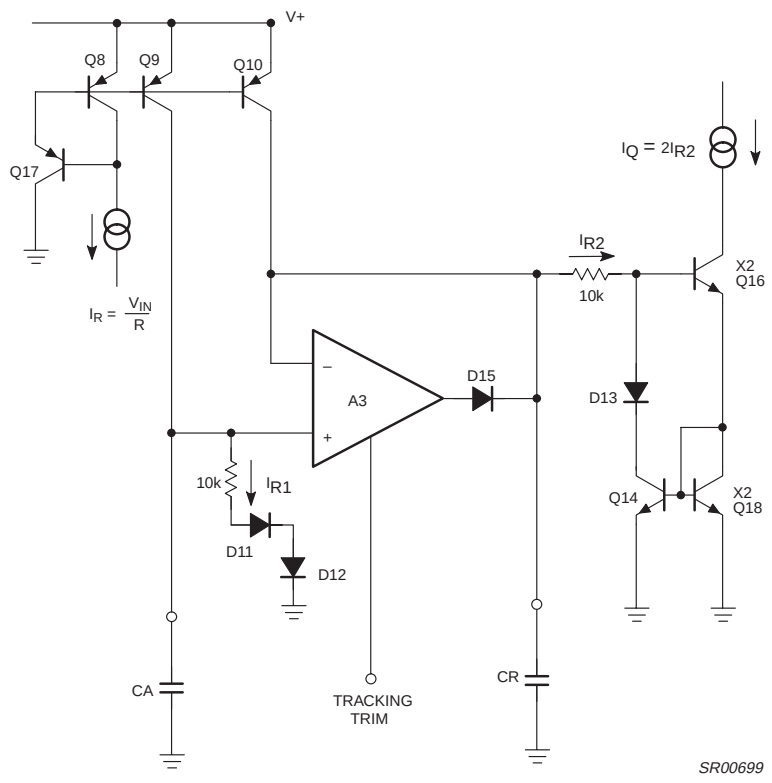

Fig 6. Buffer amplifier schematic.

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11.1.5 Basic expandor

Figure 7 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \times \frac{R_3 \times V_{IN(AVG)}}{R_2 \times R_1} \quad (7)$$

(I_1 = 140μA)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8 kΩ internal resistor. The maximum input current into the gain cell can be as large as 140 mA. This corresponds to a voltage level of 140 μA × 6.8k = 952 mV peak. The input peak current into the rectifier is limited to 300 μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \quad (8)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

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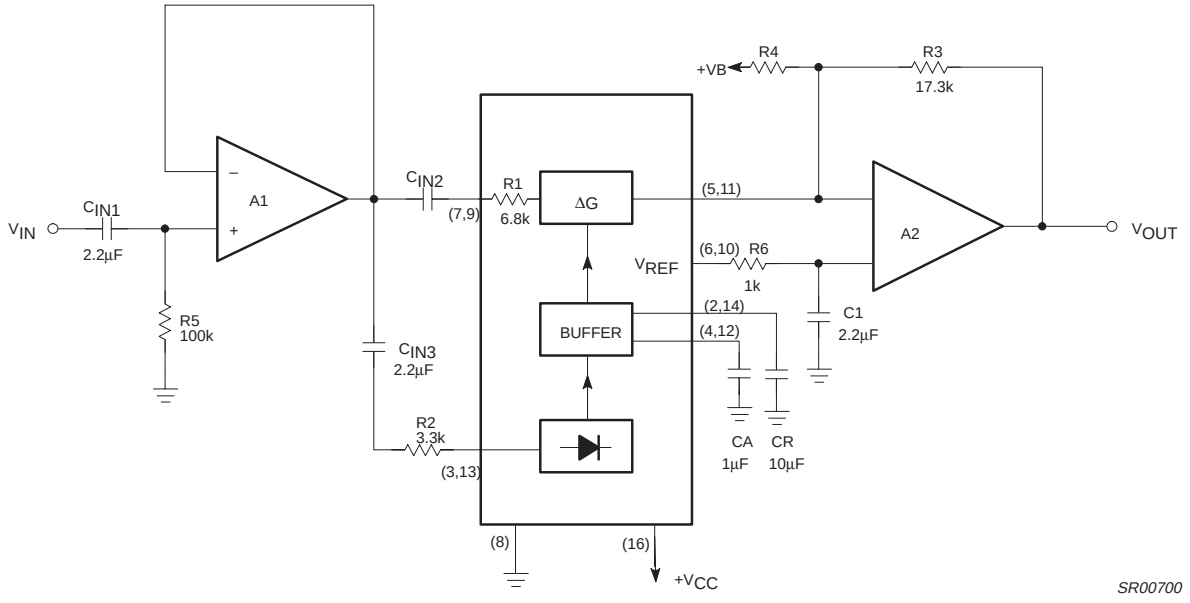

Fig 7. Basic expandor schematic.

11.1.6 Basic compressor

Figure 8 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \sqrt{\left(\frac{I_1}{2} \times \frac{R_2 \times R_1}{R_3 \times V_{IN(AVG)}}\right)} \tag{9}$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \times \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \tag{10}$$

The zener diodes D_1 and D_2 are used for channel overload protection.

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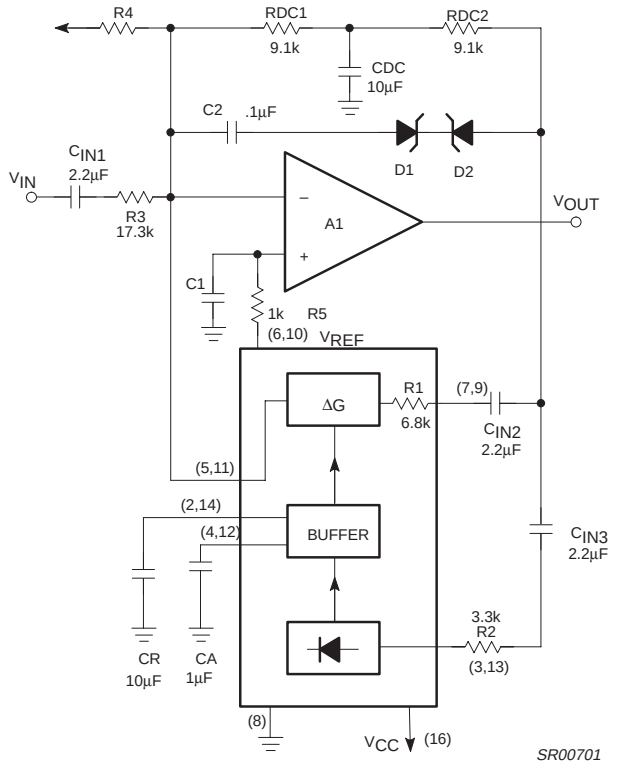

Fig 8. Basic compressor schematic.

11.1.7 Basic compandor system

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 9 shows the system level diagram for reference.

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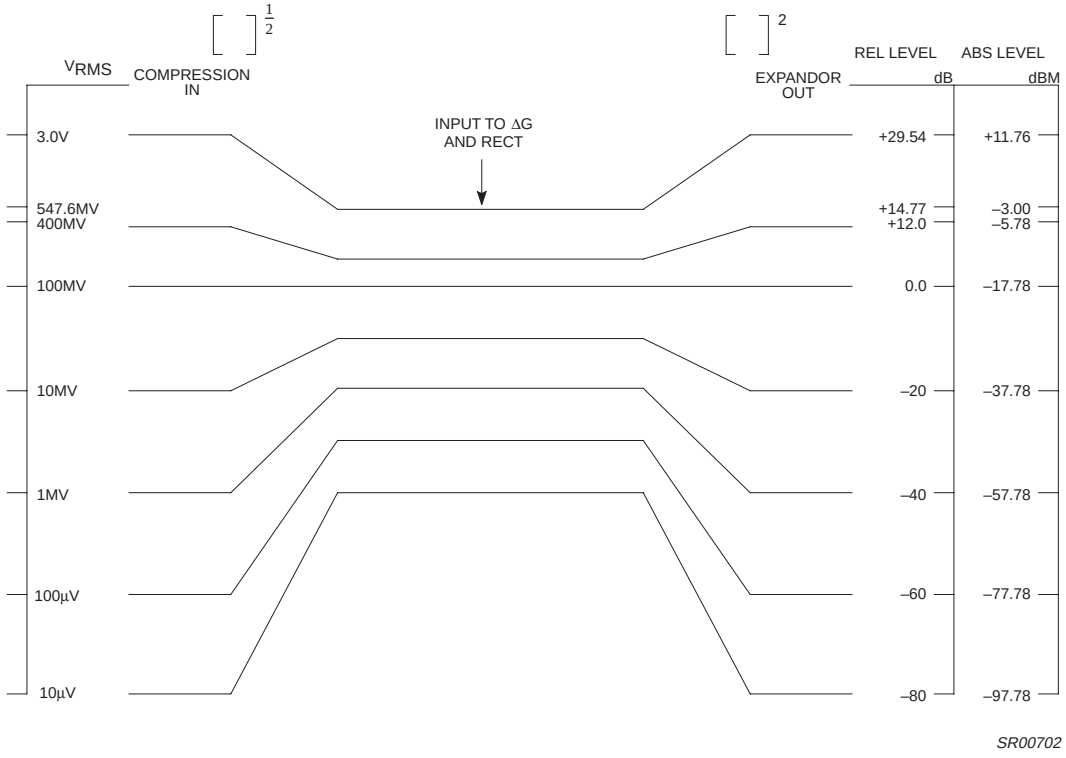

Fig 9. SA572 system level.

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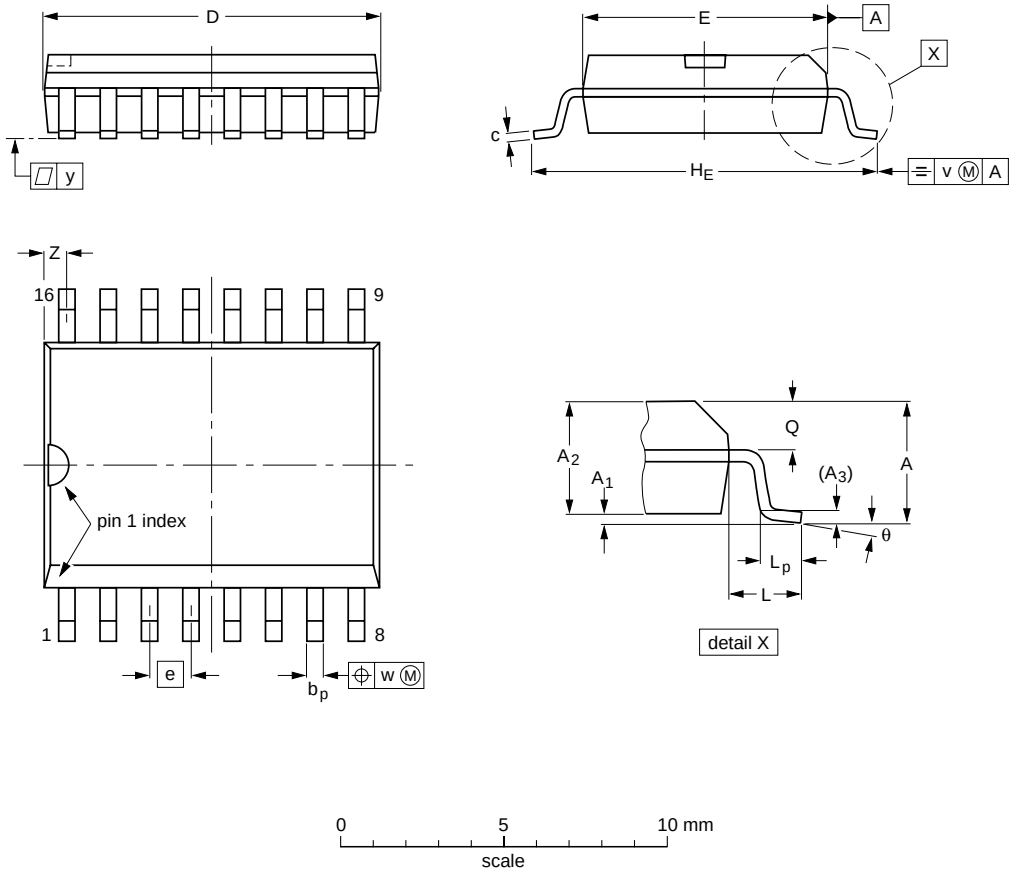
12. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				~~97-05-22~~ 99-12-27

Fig 10. SOT162-1.

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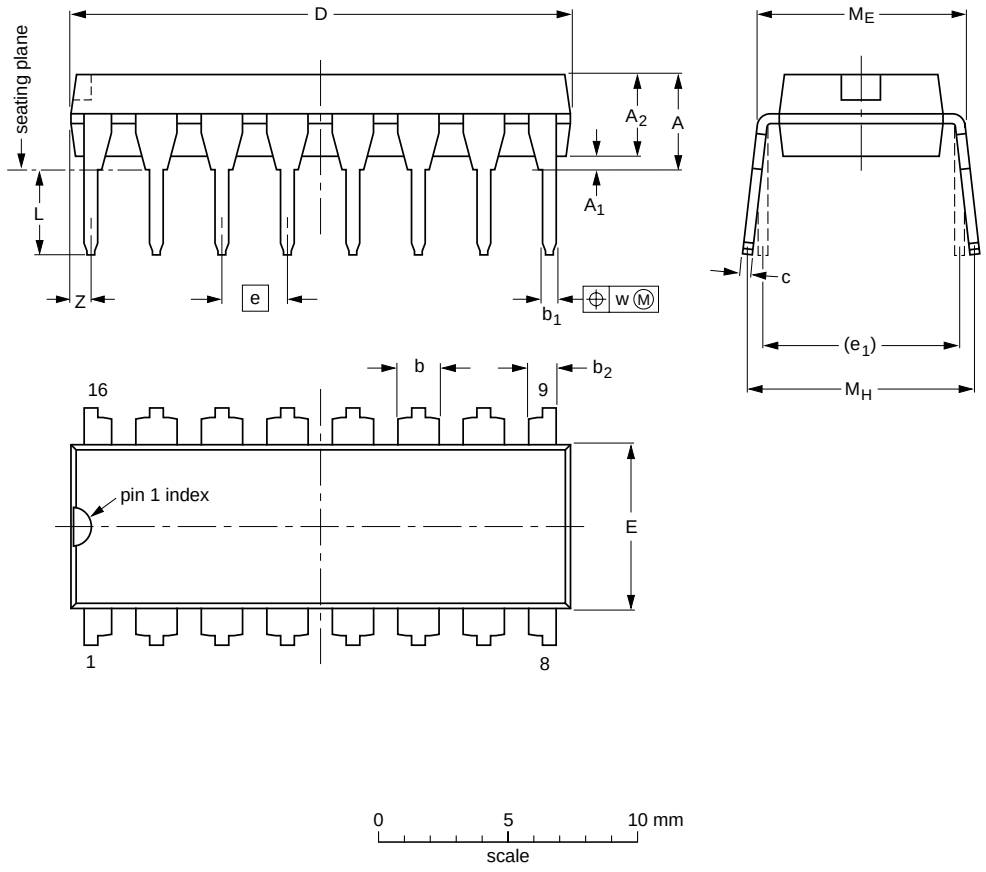
DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Fig 11. SOT38-4.

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13. Soldering

13.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Surface mount packages

13.2.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

13.2.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

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- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.2.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.3 Through-hole mount packages

13.3.1 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

13.3.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

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13.4 Package related soldering information

Table 5: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package	Soldering method		
		Wave	Reflow [1]	Dipping
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable [2]	–	suitable
Surface mount	BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable [3]	suitable	–
	PLCC [4], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended [4] [5]	suitable	–
	SSOP, TSSOP, VSO	not recommended [6]	suitable	–

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[3] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	**19981103**	**853-0813 20294**	**Product specification; third version; supersedes second version SA572_2 of 1998 Nov 03 (9397 750 04749). Modifications:** The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard.
02	**19981103**	**853-0813 20294**	**Product specification; second version; supersedes first version SA572_1 of 1987 Oct 07. Modifications:** Changed prefix from NE to SA.
01	**19871007**	**853-0813 90829**	**Product specification; initial version.**

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15. Data sheet status

Data sheet status [1]	Product status [2]	Definition
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