Floppy Disk Read/Write

GENERAL DESCRIPTION

The XR-3448 Floppy Disk Read/Write is a single 28 Pin monolithic solution for double-sided floppy disk drives. The device is compatible with 8", 5¼", and 3½" drives, providing all read and write functions and offering improved performance over industry standard dual chip sets, with lower external parts count. Schmitt trigger inputs and separate analog and power grounds aid noise and crosstalk immunity. Both pre and post amplifiers, plus an AGC, allow reliable operation with input signals ranging from 0.5 mV to 25mV.

The XR-3448 is available in a standard 28 pin package as well as a 32 pin quad surface mount package. Control, write inputs, and read outputs are TTL compatible. The device operates from +12 V and +5 V supplies.

FEATURES

All Read/Write Functions on a Single Chip
Schmitt Trigger Inputs for Noise Immunity
TTL Compatible
Power Up and Low Voltage Inhibit
Low Peak Shift – No Trimming Necessary
On Board AGC
Wide Read Dynamic Range
Low External Parts Count
All Delays RC Programmable
Separate Power and Signal Ground
Tunnel or Straddle Erase Compatibility
Erase Timers May Be Externally Overridden

APPLICATIONS

Single or Dual Head Floppy Disk Drive Systems

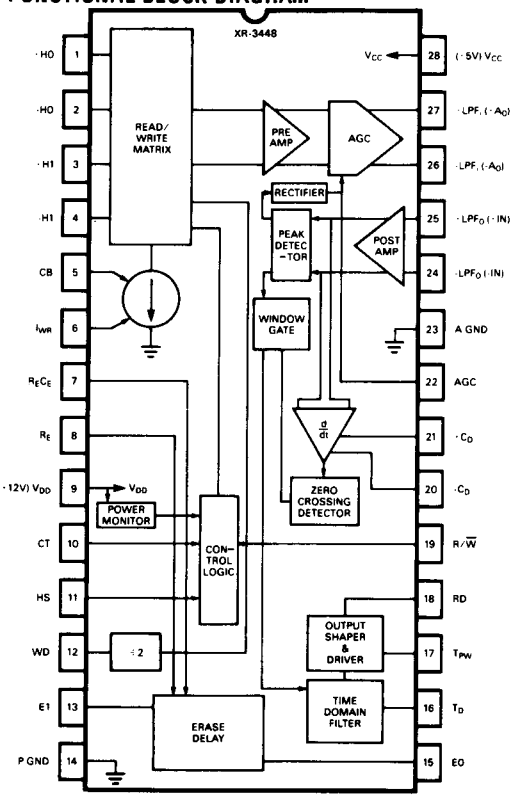
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
Pin 28 (5 V)	7 V
Pin 9 (12 V)	15 V
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	150°C
Power Dissipation (28 Pin DIP)	800 mW
Derate Above 25°C	6.5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3448CP	Plastic	0°C to +70°C
XR-3448CN	Ceramic	0°C to +70°C
XR-3448CQ	Surface Mount Quad	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-3448 Floppy Disk Read/Write is a high performance single chip solution for all standard floppy disk drives. TTL compatible control and interface levels, and +12 V and +5 V operation allows easy system implementation with standard components. An on-board voltage monitor, with hysteresis, supervises device voltage and disables all operation during power up and down. Dual grounds, one for the digital levels, the other for low level signals, and the use of ECL processing logic eliminates digital crosstalk and jittering coupled back into the read heads.

Read error reduction performance is greatly enhanced by the window gating logic that qualifies data pulse and eliminates errors generated by noise or discontinuities during shouldering. A time domain filter further reduces errors caused by nonlinearities about data peaks. Together, these systems allow improved performance margins over simpler floppy disk read devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 12 V, V_{CC} = 5 V, R_{ED} = 10k, C_E = 0.05μF, R_{EH} = 10kΩ, C_D = 1500 pF, R_D = 100Ω, C_{TD} = 100 pF, R_{TD} = 10kΩ, C_{PW} = 330 pF, R_{PW} = 10kΩ, Output Load = 1kΩ to V_{CC}, V_{IN} (preamp) = DC coupled 10 mVp-p sine wave, V_{IN} (postamp) = AC coupled 400 mVp-p sine wave, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	Recommended Power Supply Voltage	4.5	5	5.5	V	
V_{DD}	Recommended Power Supply Voltage	10.8	12	13.2	V	
I_{CC}	Power Supply Current (5 V)		35 37	45 47	mA mA	Read Mode Write Mode
I_{DD}	Power Supply Current (12 V)		19 19	25 25	mA mA	Read Mode Write Mode, I_E = 0
POWER SUPPLY MONITOR						
V_{CC}	Power Up Threshold Power Down Threshold	2.5 2.0	3.5 2.8	4.3 3.8	V V	
V_{DD}	Power Up Threshold Power Down Threshold	7.0 6.5	8.8 8.0	10.3 9.5	V V	
LOGIC INPUTS						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current			−400	μA	V_{IL} = 0.4 V
I_{IH}	Input High Current			20	μA	V_{IH} = 2.4 V
DATA OUTPUT						
T_D	Time Domain Filter Accuracy	−15	±5	15	%	R_{TD} = 10k, C_{TD} = 100 pF, f_{in} = 125kHz
T_{PW}	Output Pulse Width Accuracy	−20		20	%	R_{PW} = 10kΩ, C_{PW} = 300 pF, f_{in} = 125kHz
V_{OL}	Output Low Voltage		0.3	0.5	V	R_L = 1kΩ
V_{OH}	Output High Voltage	2.7	4.6		V	I_{OH} = 400μA
t_r	Output Rise Time		60		nS	R_L = 1kΩ
TIMERS						
	Erase Delay Accuracy	−15	±5	15	%	Error from $T_{ED} = R_{ED} C_E$
	Erase Hold Accuracy	−15		15	%	Error from $T_{EH} = 0.87 (R_{ED}+R_{EH})C_E$
	Time Domain Filter Accuracy	−15		15	%	R_{TD} = 10k, C_{TD} = 100 pF

4

READ MODE						
PREAMPLIFIER						
A_V	Differential Voltage Gain	400	500	600	V/V	f = 250 kHz, V_{CT} = 1.5V, Pin 22 Shorted to Ground
BW	Bandwidth	12.5	25		MHz	-3 dB Point
	Gain Flatness	−1.0		1.0	dB	f = 0 to 1.5 MHz
Z_{IN}	Differential Input Impedance	10	20		kΩ	f = 250 kHz
V_{CT}	Center Tap Voltage		1.5		V	Read Mode
	AGC Dynamic Range		12		dB	For 3 dB Output Variation
POSTAMPLIFIER & DIFFERENTIATOR						
A_V	Differential Voltage Gain	3.0	4.0	5.0	V/V	f = 250 kHz
BW	Bandwidth	12.5	25		MHz	−3 dB Point
	Gain Flatness	−1.0		1.0	dB	f = 0 to 5 MHz
PS	Peak Shift		0.5		%	
WRITE MODE						
V_{CT}	Center Tap Output ON Voltage	V_{DD} −2.5	V_{DD} −1.8	V_{DD} −0.5	V	R_E = 150Ω
	Unselected Head Erase Leakage		0.1	100	μA	V_{E0}, V_{E1} = 12V, R_E = 150Ω
I_W	Recommended Write Current Range	3		10	mA	R_W = 680Ω to 240Ω
	Write Current Accuracy	−5	±0.2	5	%	CB = 0, Error from $I_W = \frac{2.38}{R_W}$
	Write Current Unbalance	−1	±0.01	1	%	Head 0 to Head 1
CB	Current Boost Factor	1.25	1.30	1.35		CB = 1
V_E	Erase Output ON Voltage		0.3	1.0	V	R_E = 150Ω
	Erase Override Voltage		4		V	Pin 7, Voltage to Force Erase ON. R/W = 0.
			0.8		V	Pin 7. Voltage to Force Erase OFF. R/W = 0.

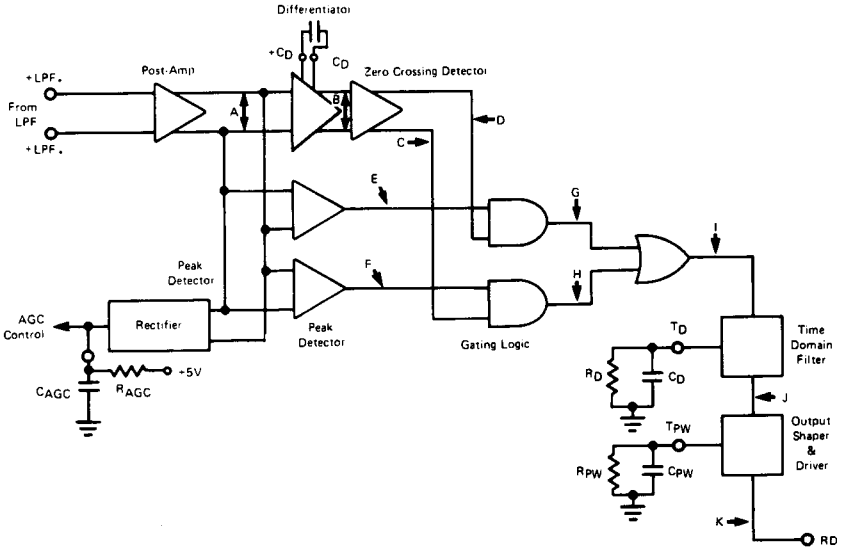


Figure 1. Read Error Reduction Circuitry

PRINCIPLES OF OPERATION

Write Mode

In the write mode, R/W (Pin 19) is held low. Data is applied to the input Schmitt trigger (Pin 12), goes through a toggle flip-flop, and into the write matrix. The proper magnetic head is selected by the matrix, depending on the level at HS (Pin 11). Both head center taps are connected to CT (Pin 10) which sources the current sunk by the proper transistor (Pin 1, 2, 3, or 4).

Write current is controlled by the resistor, R_{IW}, on I_{WR} (Pin 6); when CB (Pin 5) is pulled high, write current is boosted 30%. Tunnel erase delay and hold times are set by a capacitor and two resistors on $R_E C_E$ (Pin 7) and R_E (Pin 8). Straddle erase heads are accommodated by eliminating C_E.

Read Mode

Pulling R/W high selects data readback mode. The dual error reduction system employed by the XR-3448 greatly diminishes read error rates. The read signal is routed through a diode multiplexer into a low noise preamplifier. This output is fed to an automatic gain control (AGC) circuit which lowers peak shift: for most systems, external peak shift adjustment is unnecessary across an input dynamic range from 500 μV to 25 mV. The AGC compresses a 12 dB input variation down to a 3 dB output range. AGC response time is affected by the RC at the AGC pin (Pin 22). The compressed signal is applied to a low pass filter (LPF) which attenuates high frequency noise. A post-amplifier compensates for LPF insertion losses and drives both the Peak Detector and Active Differentiator (see Figure 1) with waveform A, shown in Figure 2. The Peak Detector is a comparator-like device that produces output whenever data input is above a threshold level (see Figure 2E, 2F). This output is employed as the Gating Logic enable. Rectified peak detector output is returned to the AGC as the control signal.

The Active Differentiator computes the first derivative of the input signal, producing waveform B of Figure 2. Zero Crossing Detector output toggles (Figure 2C, 2D) at zero crossings, which correspond to data peaks — one crossing per datum. Hysteresis in the detector aids noise immunity. The Window Gating Logic effectively provides an AND function: output (Figure 2I) appears only when (1) the Zero Crossing Detector sees a crossing, and (2) the Peak Detector sees a data peak. Spurious signals, therefore, do not cause output.

Noise and system nonlinearities however, occasionally produce closely spaced false outputs from the zero crossing detector. Further error reduction is provided by a time domain filter following the gating logic. Adjacent pulses, occurring before the minimum time delay set by a resistor and capacitor on T_d (Pin 16), are ignored (Figure 2J). Since nonlinearities occur in pairs, a valid data pulse mixed with two invalid pulses still provides one meaningful output — exactly as desired. Output pulse width is determined by an RC on T_{pw} (Pin 17), which feeds the output driver with TTL level constant width pulses. The data appears at RD (Pin 18), as shown in Figure 2K.

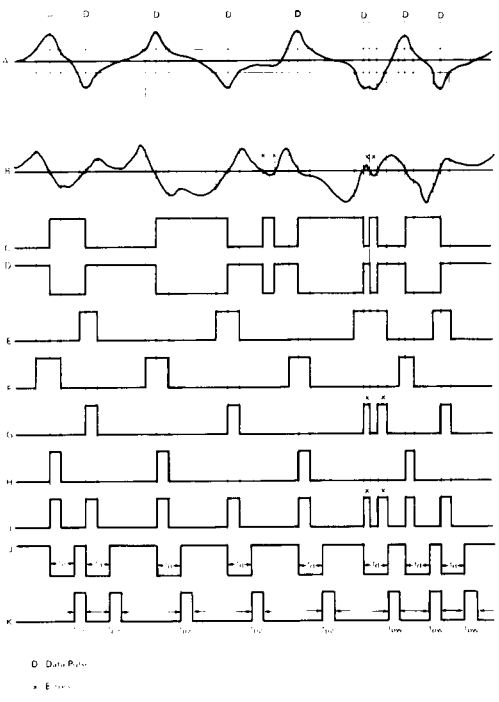


Figure 2. Read Waveforms

Figure 2 shows both common and uncommon error signals and how the XR-3448 corrects them. Basically, shouldering and noise errors are eliminated by the detection threshold of the gating logic. Non-linearity induced errors near signal peaks are removed by the time domain filter.

APPLICATIONS INFORMATION

The applications circuit of Figure 3 may be customized to match the available magnetic head, interface pulse widths, write currents, AGC times, data transfer rates, etc. Table 1 gives recommended component values and ranges. Table 2 shows digital control logic states.

DESIGN INSTRUCTIONS

AGC:

The AGC time constant is set by the resistor and capacitor on Pin 22. The time must be short enough that initial data does not overdrive the amplifiers, yet long enough that noise and offset levels between data bits do not register as output. Delay time is determined by:

$$T = R_{AGC}\, C_{AGC}$$

For most applications at 500 kB data rate, a time of 1 ms, using R_{AGC} = 10 kΩ and C_{AGC} = 0.1μF is recommended..

LPF

The LPF is strongly dependent on head type and other system and circuit considerations. Constant gain and phase to f = (baud rate/2) is tantamount to proper performance. Avoiding driver saturation requires that the filter current is less than 2.8 mA. The preamplifier inputs are DC biased internally. Blocking capacitors should isolate the DC level from the AGC output; optimum transient response characteristics occur when the capacitors are before the filter, directly after the AGC output.

Active Differentiator

The differentiation function requires a capacitor network across Pins 20 and 21. The dominant component, capacitor C_D, is optimum when its current slew rate is maximized. This occurs when

$$C_D = \frac{1\ mA}{(A_{VD})\,(E_P)\,(\omega_{max})\,(A_F)}$$

Where A_{VD} is the gain of the amplifier
E_P is the maximum expected input voltage
ω_{max} is the maximum operating frequency in radians/sec of the system
A_F is the gain of the filter network

If C_D is greater than the maximum value calculated above, peak shifting will occur.

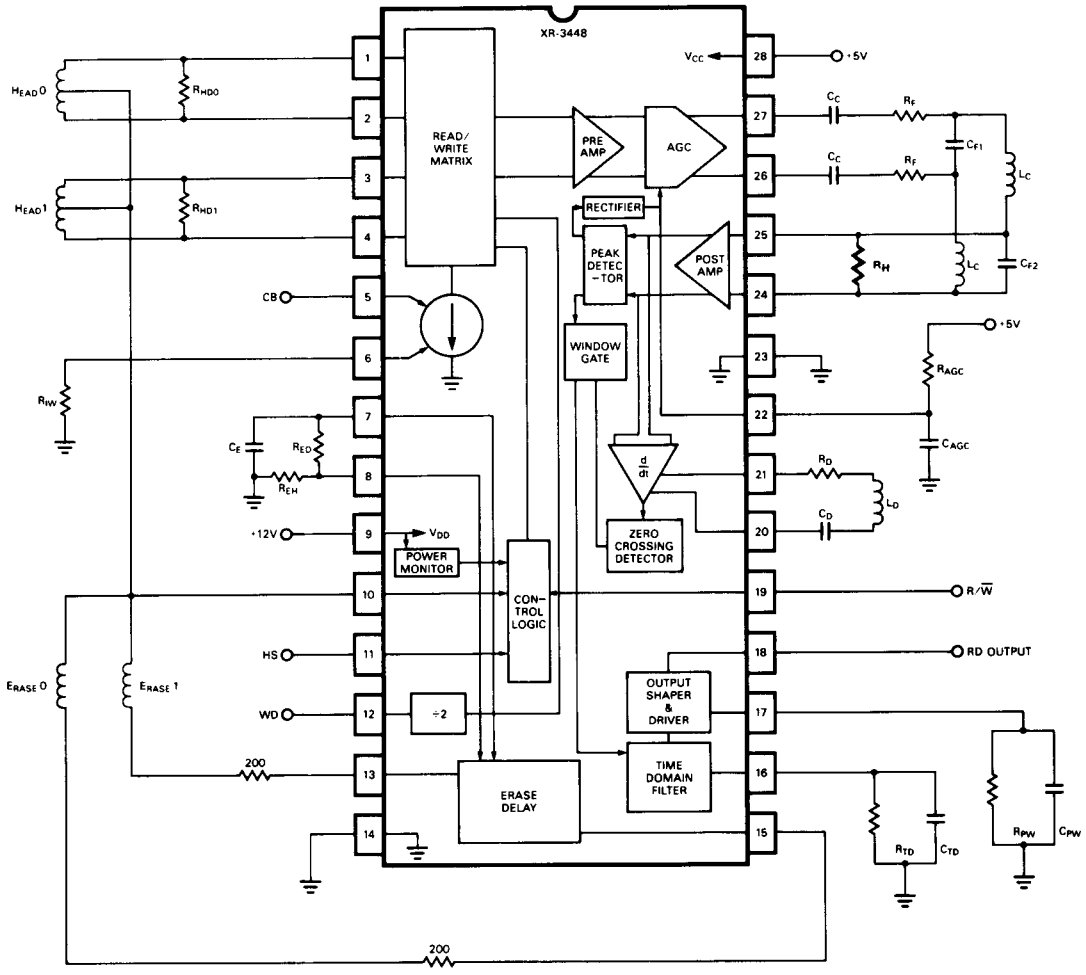


Figure 4. XR-3448 Typical Application

For maximum gain applications delete R_{AGC} and C_{AGC} and ground pin 22.

TABLE I

TYPICAL COMPONENT VALUES

Component	Typical Value	Recommended Range	Component	Typical Value
R_{IW}	560Ω	180 - 680Ω	C_C	.022μF
R_{E0}, R_{E1}	280Ω	100 - 680Ω	R_F	470Ω
R_{ED}, R_{EH}	10kΩ	5k - 30kΩ	C_{F1}	.001μF
C_E	.047μF	0.01 - 0.068μF	C_{F2}	470pF
R_{PW}	10kΩ	5k - 25kΩ	L_C	680μH
C_{PW}	100 pF	51 pF - 1000 pF	R_D	200Ω
R_{TD}	10kΩ	5k - 25kΩ	C_D	1000pF
C_{TD}	100pF	51 pF - 330 pF	L_D	56μH
R_{AGC}	6.8kΩ	3.3k - 25kΩ	R_H	1.5kΩ
C_{AGC}	.1μF	.01μF - 1μF		

TABLE II

CONTROL LOGIC STATES

Mode	Logic Level	
INPUT	0	1
HS	Head 0	Head 1
R/W	Write	Read
CB	Normal Write Current	30% Boost Write Current
$R_E C_E$	Erase Off	Forced Erase (Write Only)

When C_D is the only component employed, a pole is produced by C_D and the effective output resistance of Q1 and Q2 (See Figure 3), R_O. This pole lies at

$$\omega_p = \frac{1}{2R_O C_D}$$

where R_O is typically 40Ω.

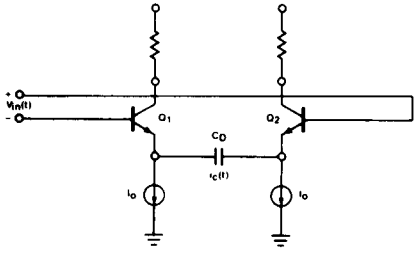


Figure 3. Simplified Active Differentiator Section

Perfect differentiation requires a phase shift of 90° This suggests ω_p should approach ∞ since

$$\theta = \arctan (\omega_p/\omega_O)$$

where ω_O = operating frequency.

A large ω_p, however, produces a large noise bandwidth; a reasonable compromise sets ω_p at 10 ω_{max}. This produces a phase shift of approximately 84° and limits the noise bandwidth. The design criteria is now given by

$$\omega_{max} = \frac{1}{20(R_O C_D)}$$

Active Differentiator

The differentiation function requires a capacitor network across Pins 20 and 21. The dominant component, capacitor C_D, is optimum when its current slew rate is maximized. This occurs when

Where A_{VD} is the gain of the amplifier
E_P is the maximum expected input voltage
ω_{max} is the maximum operating frequency in radians/sec of the system
A_F is the gain of the filter network

If C_D is greater than the maximum value calculated above, peak shifting will occur.

When C_D is the only component employed, a pole is produced by C_D and the effective output resistance of Q1 and Q2 (see Figure 4), R_O. This pole lies at

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Often, R_O is too low, creating a pole at a frequency greater than 10 ω_{max}. In this case, a resistor R_D, in series with C_D gives the equation:

$$\omega_{max} = \frac{1}{20(R_D + R_O) C_D}$$

This allows a degree of flexibility in selecting the noise bandwidth, as shown in Figure 5.

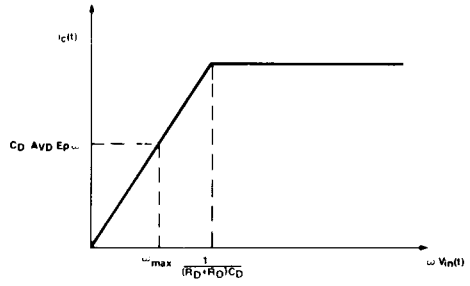


Figure 5: Differentiator Response for C_D and R

A series inductor, L_D, will further reduce noise bandwidth by introducing another pole. When selected for 10 ω_{max}, as shown in Figure 6, L_D is given by

$$L_D = \frac{1}{100(\omega_{max})^2 C_D}$$

The damping ratio, δ, should be between 0.3 and 1 where

$$\delta = \frac{(R_O + 0.5\ R_D)\ C_D}{2\sqrt{L_D C_D}}$$

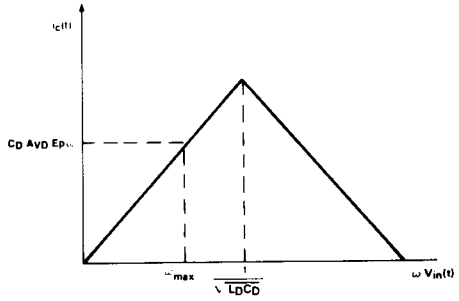


Figure 6: Differentiator Response with R_D, C_D, and L.

Often, L_D may be excluded due to the superior noise reduction characteristics of the XR-3448.

Time Doman Filter

Filter time, T_D, is determined by the maximum period at expected distortion and the maximum operating frequency.

Delay time is set by R_{TD} and C_{TD} on Pin 16, and is affected by differentiator capacitor, C_D.

$$T_D = 0.25\ R_{TD}\ C_{TD} + t_x$$

Where R_{TD}: 1kΩ ≤ R_{TD} ≤ 15kΩ, and C_{TD}: 51 pF ≤ C_{TD} ≤ 330 pF. Time t_x as a function of C_D is shown in Figure 7.

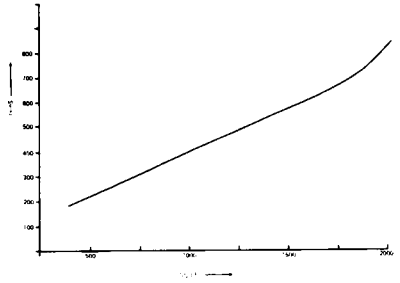


Figure 7. Additional Time Delay (t_x) introduced by C_D.

For values of C_D ≤ 1500 pF, the following approximation is valid:

$$t_x \approx 0.36\ C_D + 40$$

Where t_x is in nS and C_D is in pF.

Output Shaper

The output shaper determines the pulse width of the data signal. Pulse width is

$$t = 0.25\ R_{PW}\ C_{PW}$$

where R_{PW}: 5kΩ ≤ R ≤ 30kΩ, and C_{TD}: 100 pF ≤ C ≤ 620 pF.

Damping Resistors

Head damping resistors should be optimized for writing. Their value depends entirely on the head employed and the desired damping coefficient.

Write Current

A current mirror uses the internal voltage reference and a resistor from Pin 6 to ground for write current programming. The resistor value is determined by

$$R_{IW}\ (k\Omega) = \frac{2.35V}{I_{WR}\ (mA)}$$

Write current increases by 30% over this value when CB (Pin 5) is held at a high TTL logic level.

Additional write current steps, if necessary, are implemented as shown in Figure 8. In Figure 8(a), TTL logic lines and resistors vary current output. Figure 8(b) shows the resistive ladder method, with transistors selectively switching resistors. The varying resistance on Pin 6 causes varying write currents.

$$I_W\ (mA) = \frac{2.35V}{R_{IW}\ (total)\ (k\Omega)}$$

These method work for any number of control lines. CB (Pin 5) is still active, and will multiply current by 1.3 whenever held high.

Write Erase Resistors

Erase current is limited by series resistors from E0 and E1 to the respective erase heads. Resistor values may be approximated by:

$$R_E = \frac{V_{CT} - V_{SAT}}{I_{ERASE}}$$

For typical I_{ERASE} = 50 mA, V_{CT} = 10.5 V, and V_{SAT} = 500 mV, R_E = 200 Ω.

Erase Delay Time

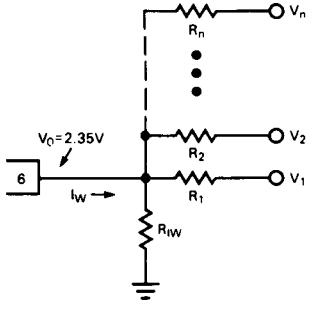
Tunnel erase delays are provided by the XR-3448. Both Erase Delay Time, T_{ED}, which controls erase initiation and Erase Hold Time, T_{EH}, which delays erase release, are controlled by a simple RC circuit. In the configuration of Figure 1, T_{ED} is calculated as:

$$T_{ED} = R_{ED} C_E$$

and T_{EH} is determined by

$$T_{EH} = 0.87 (R_{ED} + R_{EH}) C_E$$

Suggested resistor values range between 5kΩ and 30kΩ. C_E should range from 0.01μF to 0.068μF.

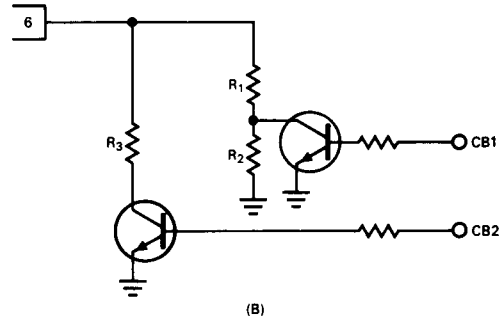


$$I_W = \frac{V_0}{R_{IW}} - \left(\frac{V_1 - V_0}{R_1}\right) - \left(\frac{V_2 - V_0}{R_2}\right) - \cdots - \left(\frac{V_n - V_0}{R_n}\right)$$

WHERE V_0 = 2.35V AND V_1 THROUGH V_n ARE LOGIC LEVELS.

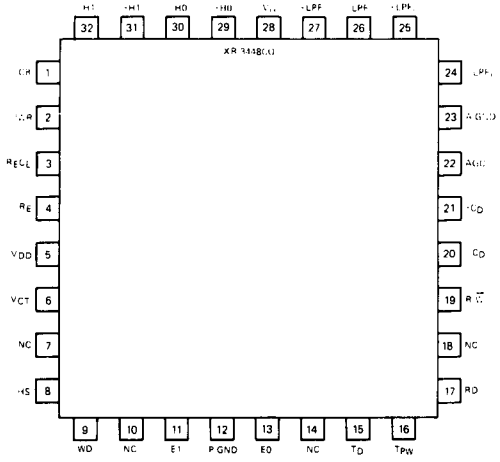
(A)

CB1	CB2	R_{IW} (eff)
0	0	$R_1 + R_2$
0	1	$R_3//R_1 + R_2$
1	0	R_1
1	1	$R_3//R_1$



(B)

Figure 8. Obtaining Additional Write Current Steps: (A) TTL Lines and Resistors Increase and Decrease I_W. (B) Transistors Switch Resistors to Increase I_W.



Quad Package Pinout

4

EXAR

XR-1488/1489A

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

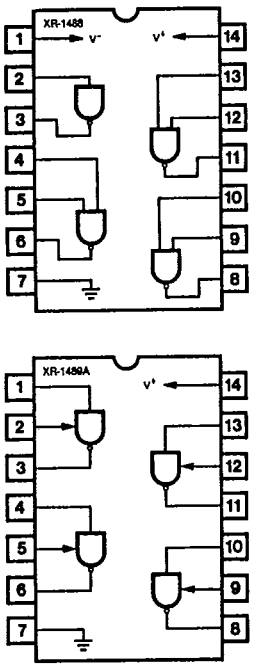
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.