DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Decoder/Demultiplexer On the basis of an applied instruction, channels of communication are selected which connect certain sources of information to certain destinations e.g., the distribution of timing signals; the interconnection between arithmetic registers.

$\overline{E}_0$, $\overline{E}_1$ Enable Inputs. The device is enabled when both the Enable inputs are LOW.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T²L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V.

$\overline{O}j$ Active LOW output of Demultiplexer/Decoder j = 0-15.

OPERATIONAL TERMS:

I_{OH} Output HIGH current forced out of output in V_{IH} test.

I_{OL} Output LOW current forced into the output in V_{IL} test.

I_{IH} Reverse input load current with V_{CC} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 7.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 7.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

$t_{pd+}(A\overline{O})$ The propagation delay from input address transition to the output LOW to HIGH transition.

$t_{pd-}(A\overline{O})$ The propagation delay from input address transition to the output HIGH to LOW transition.

$t_{pd+}(\overline{E}\overline{O})$ The propagation delay from input Enable LOW to HIGH transition to the output LOW to HIGH transition.

$t_{pd-}(\overline{E}\overline{O})$ The propagation delay from input Enable HIGH to LOW transition to the output HIGH to LOW transition.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L0859X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L0851X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

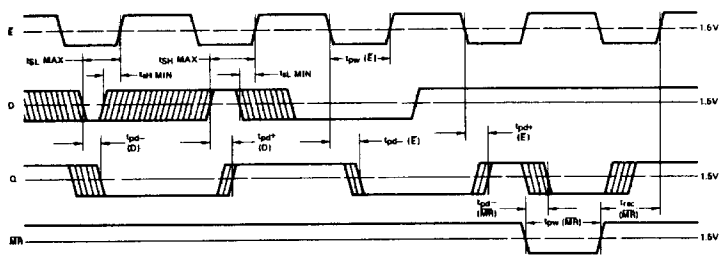
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		20	33	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\overline{E}$)	Enable to Output HIGH	V_{CC} = 5.0 V C_L = 15 pF	16	33	75	ns
t_{pd-} ($\overline{E}$)	Enable to Output LOW		15	30	60	
t_{pd+} (D)	Data to Output HIGH		12	25	55	ns
t_{pd-} (D)	Data to Output LOW		15	30	60	
t_s "H"	HIGH Data Set-up Time		2.0		20	ns
t_s "L"	LOW Data Set-up Time		3.0		35	
t_{pw} ($\overline{E}$)	Min. Enable Pulse Width			32	45	ns
t_{pw} ($\overline{MR}$)	Min. Master Reset Pulse Width			27	40	ns
t_{pd-} ($\overline{MR}$)	Master Reset to Output LOW		15	29	60	
t_{rec} ($\overline{MR}$)	Master Reset Recovery Time			20	30	ns

SWITCHING TIME WAVEFORMS



STORING A LOW. Data must be LOW by t_{SL} max and remain LOW until after t_{SH} min.

STORING A HIGH. Data must be HIGH by t_{SH} max and must remain HIGH until after t_{SL} min.

STORING A LOW. Enable pulse must be at least t_{pw} ($\overline{E}$) max.

STORING A HIGH.

RESET AND STORE HIGH. To reset, $\overline{MR}$ pulse width must be at least t_{pw} ($\overline{MR}$) max. To store data, the Enable must remain LOW at least t_{rec} ($\overline{MR}$) max after $\overline{MR}$ goes HIGH.

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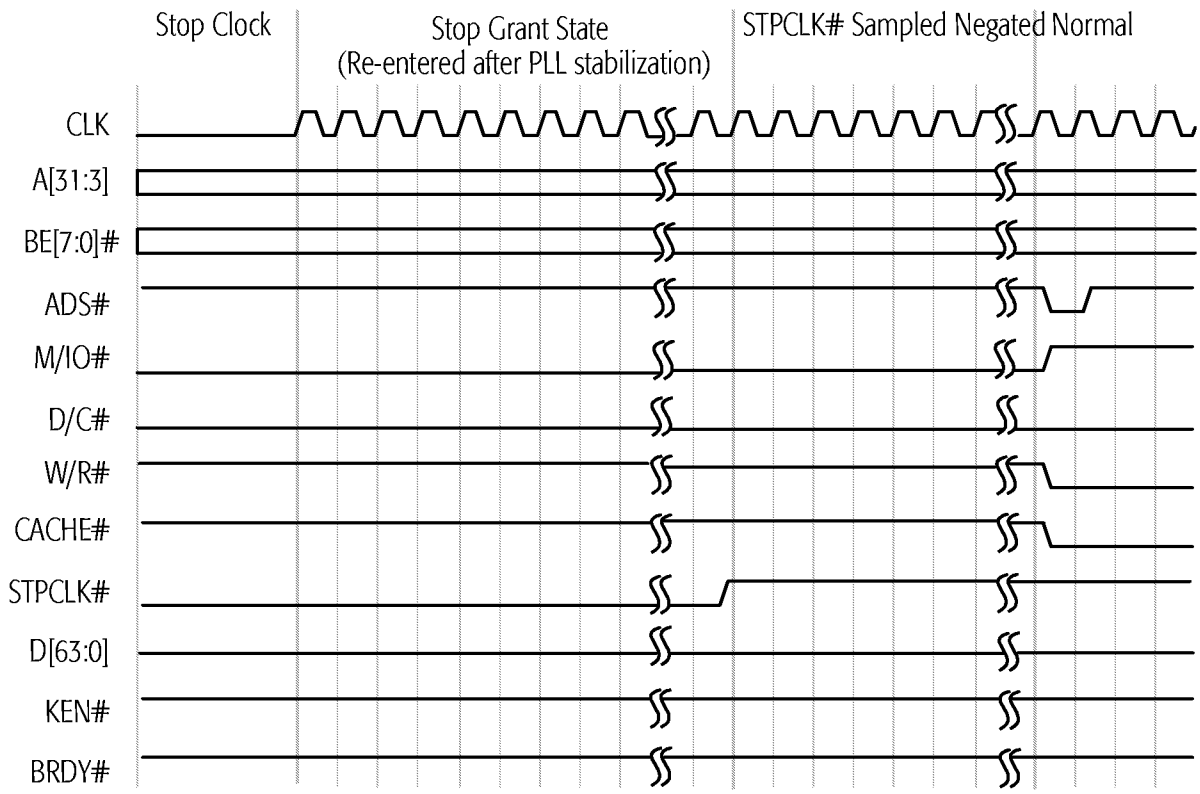

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

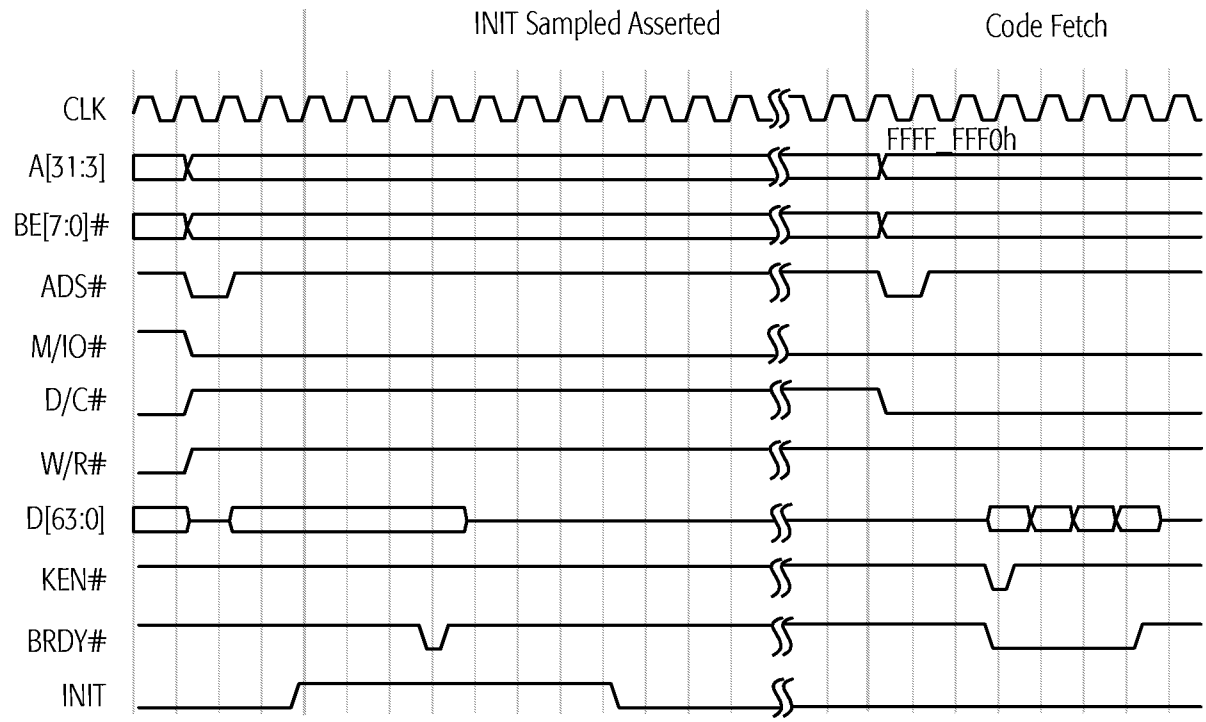

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.